ECE 3040B Microelectronic Circuits

Exam 3

November 29, 2001

Dr. W. Alan Doolittle

Print your name clearly and largely: Solution

Instructions:
Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

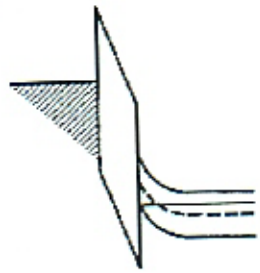
***First 15%* Multiple Choice and True/False (Select the most correct answer)**

1.) (3-points) "OP-amp" stands for :
   a.) Oh pooh!
   b.) Operating Amplifier
   c.) Operational Amplifier
   d.) Oh please help me!

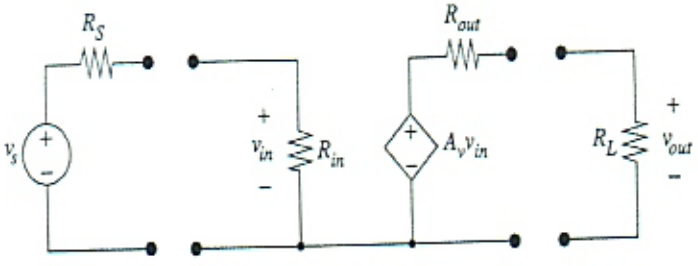
2.) (3-points) An enhancement mode NMOS transistors has a…
   a.) …p-type substrate.
   b.) …n-type substrate
   c.) n-type channel when biased into cutoff (either depletion or accumulation)
   d.) huge gate current.

3.) (3-points) True / False When a "real world" (Non-ideal) Op-Amp is used in a circuit that uses negative feedback (part of the output is fed back to the negative input terminal) it is possible that the input resistance of the circuit is higher than the input resistance of the Op-amp.

4.) (3-points) Which of the following is true about the figure to the right?
   a.) This is a NMOS capacitor biased into inversion.
   b.) This is a NMOS capacitor biased into depletion.
   c.) This is a NMOS capacitor biased into accumulation.
   d.) This is a PMOS capacitor biased into inversion.
   e.) This is a PMOS capacitor biased into depletion.
   f.) This is a PMOS capacitor biased into accumulation



5.) (3-points) For the following amplifier:
   a.) Is this a: Voltage, Current, Transconductance, or Transresistance Amplifier
   b.) Should this amplifier have an High or Low input impedance?
   c.) Should this amplifier have an High or Low output impedance?



Second 20% Short Answer:

6.) (10 points) A NMOS transistor at room temperature has a substrate doping of 1e15 cm^{-3} an oxide thickness of 2000 angstroms (10^{-8} cm), determine the threshold voltage of the transistor. Use the following:

Substrate relative Dielectric Constant, $\varepsilon_{r\text{-semiconductor}}=K_S=11.7$

Oxide relative Dielectric Constant, $\varepsilon_{ox}=K_{ox}=3.9$ $= \varepsilon_{r\text{-}ox}$

Dielectric Constant of free space, $\varepsilon_O=8.854\text{e-}14$ F/cm

Substrate intrinsic concentration, $n_i=1\text{e}10$ cm^{-3}

$$\phi_F = \begin{cases} \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) & \text{for a p - type semiconductor} = 0.0259\left(\ln\frac{10^{15}}{10^{10}}\right) = 0.298\ V \\ -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) & \text{for a n - type semiconductor} \end{cases}$$

$$V_T = 2\phi_F + \frac{\varepsilon_{Si}}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_S}(2\phi_F)} \quad \text{(for n - channel devices)}$$

$$V_T = 2\phi_F - \frac{\varepsilon_{Si}}{C_{ox}}\sqrt{\frac{2qN_D}{\varepsilon_S}(-2\phi_F)} \quad \text{(for p - channel devices)}$$

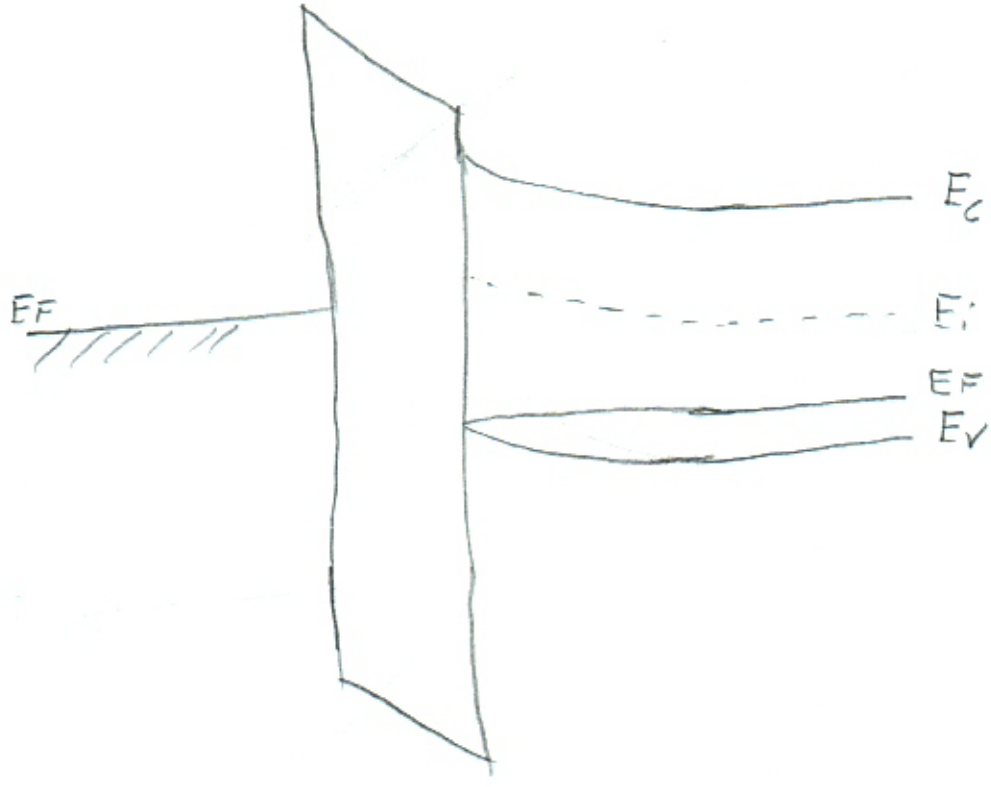
where,

$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}}$ is the oxide capacitance per unit area $= \frac{3.9\,(8.854\text{e-}14)\ F/cm}{2000 \times 10^{-8}\ cm} = 1.73\text{e-}8\ F/cm^2$

$$V_T = 2(0.298) + \frac{11.7(8.854\text{e-}14)}{1.73\text{e-}8\ F/cm^2}\sqrt{\frac{2(1.6\text{e-}19)(1\text{e}15)(2)(0.298)}{(11.7)\ 8.854\text{e-}14\ (F/cm)}}$$

$$V_T = 1.4\ V$$

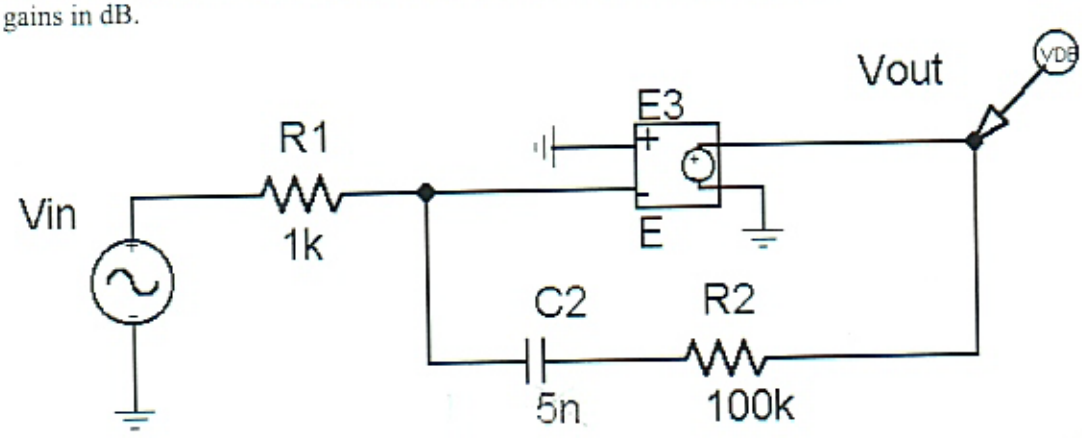
7.) (10-points) Draw and label the energy band diagram of a NMOS Enhancement mode Capacitor in ~~equilibrium, and~~ accumulation ~~(2 drawings)~~ labeling the fermi, intrinsic, conduction and valence energies.



Third 25% Problems (3rd 25%)

8.) You may assume that the **Op-Amps are ideal in parts a and b**.

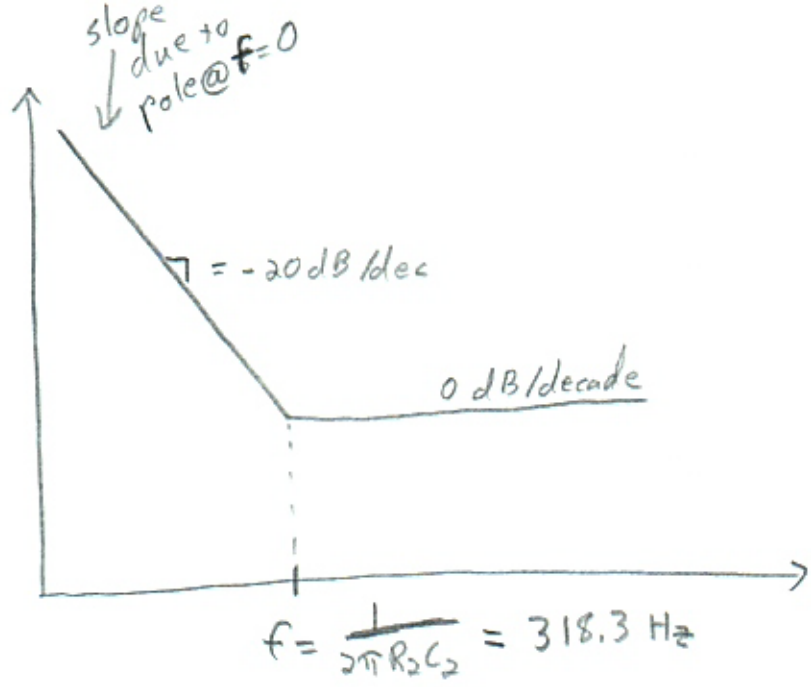
(a. 10-points) ~~Plot~~ sketch the voltage gain transfer function (Voltage gain in dB vs. Log(frequency)), v_{out}/v_{in} of the following circuit from 1Hz to 10MegHz showing the break frequencies and low and high frequency gains in dB.



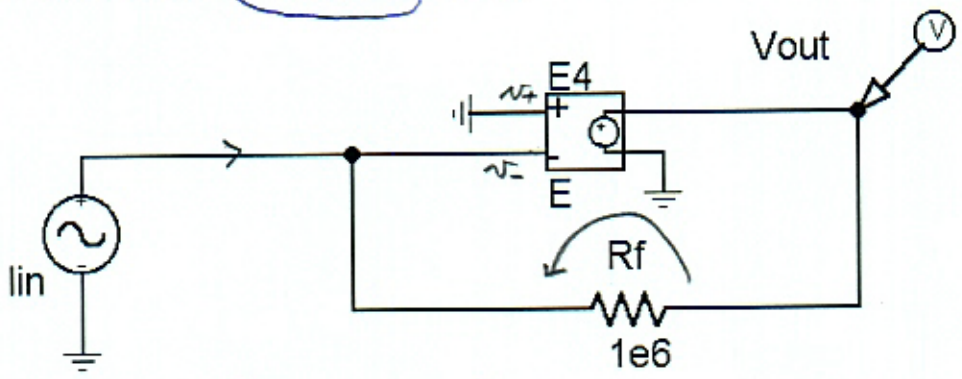
1 zero

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{C_2 s} + R_2}{R_1} = -\frac{1 + R_2 C_2 s}{R_1 C_2 s}$$

1 pole @ s=0



(b. 10-points) The circuit below takes a current input and converts it to a voltage output. Determine what the gain, v_{out}/i_{in} would be. Determine the input resistance and output resistance. Is this a current, voltage, transconductance or transresistance amplifier?



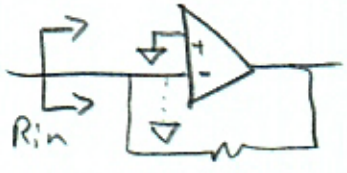
$$\frac{(v_- - v_{out})}{R_f} = i_{in}$$

but due to the virtual Ground,

$$v_- = 0 = v_+$$

$$\boxed{\frac{v_{out}}{i_{in}} = -R_f}$$

$R_{in} = 0$



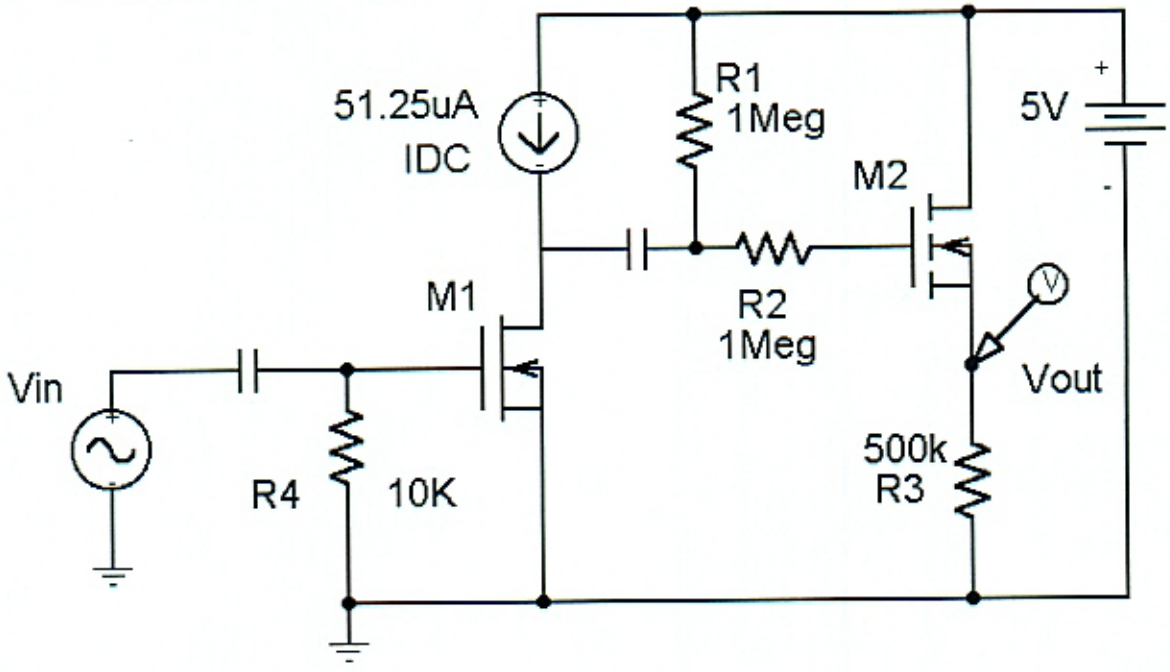
due to virtual Ground

$R_{out} = 0$

Pulling all the concepts together for a useful purpose: (4^{th} 25%)

12.) (40-points) Given the following circuit, what is the AC voltage gain, V_{out}/V_{in}? You may assume all capacitors have infinite capacitance and are thus, AC shorts. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: 15 points for DC solution (gate, source and drain voltages along with drain current), 5 points for the conversion to the small signal model and 20 points for small signal analysis.

Hint: The DC current source simplifies the DC analysis as IDC = I_{DS} =51.25 uA.



Use the following parameters:

For NMOS Depletion Transistors:

K_n'=25 uA/V^2 V_T=-2.0V λ=0.01 V^{-1} Length (L)=10 um Width (W)=10 um

For NMOS Enhancement Transistors:

K_n'=25 uA/V^2 V_T=0.75V λ=0.0 V^{-1} Length (L)=10 um Width (W)=10 um

For PMOS Depletion Transistors:

K_n'=25 uA/V^2 V_T=+3.0V λ=0.01 V^{-1} Length (L)=10 um Width (W)=10 um

For PMOS Enhancement Transistors:

K_n'=25 uA/V^2 V_T=-1.75V λ=0.0 V^{-1} Length (L)=10 um Width (W)=10 um

D.C. M1 Assume Saturation:

$$51.25\mu A = \frac{25e\text{-}6}{2}\left(\frac{1}{1}\right)\left(V_{GS_1} - (-2.0)\right)^2\left(1 + 0.01\, V_{DS_1}\right)$$

but $V_{GS_1} = 0\ V$

$$51.25e\text{-}6 = 50e\text{-}6\left(1 + 0.01\, V_{DS_1}\right)$$

$$V_{DS_1} = 2.5V$$

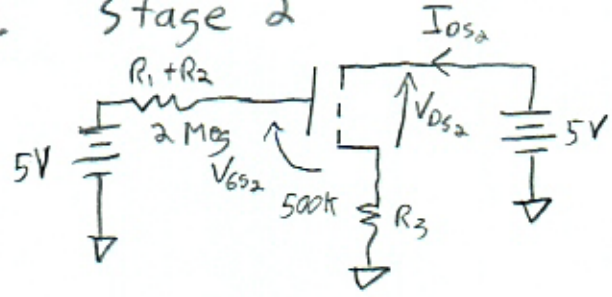
Check Assumption:

$$V_{DS_1} > V_{GS_1} - V_T = 2.5V > 0 - -2$$

$$2.5V > 2.0V \checkmark$$

Extra work can be done here, but clearly indicate with problem you are solving.

DC Stage 2



Assume Saturation

$$I_{DS_2} = \frac{k_n'}{2}\left(\frac{W}{L}\right)\left(V_{GS_2} - V_T\right)^2 \left(1 + \cancel{V_{DS_2}}^{\,0}\right)$$

$$I_{DS_2} = \frac{25e\text{-}6}{2}\left(V_{GS_2} - 0.75\right)^2 \qquad (4.25 - I_{DS}R_3)(4.25 - I_{DS}R_3)$$

but, $\quad 5V = V_{GS_2} + I_{DS_2}R_3$

$$I_{DS_2} = 12.5e\text{-}6\left(5 - I_{DS_2}R_3 - 0.75\right)^2$$

$$= 12.5e\text{-}6\left(18.0625 - 8.5\,I_{DS_2}R_3 + R_3^2 I_{DS_2}^2\right)$$

$$I_{DS_2} = 2.258e\text{-}4 - I_{DS_2}\,53.125 + 3.125e6\, I_{DS_2}^2$$

$$-3.125e6\, I_{DS}^2 - 54.125\, I_{DS} + 2.258e\text{-}4 = 0$$

$$I_{DS} = \frac{+54.125 \pm \sqrt{(54.125)^2 - 4(3.125e6)(2.56e\text{-}4)}}{2(3.125e6)}$$

$$= 10.316e\text{-}6 \text{ Amps}$$

or

$$7.004e\text{-}6 \text{ Amps}$$

$$V_{GS_2} = 5V - I_{DS_2}\,500k$$

$$V_{GS} = 1.49V \text{ or } -0.158V$$

Less than V_T ✗

$I_{DS} = 7e\text{-}6$ Amps

$V_{DS} = V_{GS} \Longrightarrow V_{DS} > V_{GS} - V_T$

$0 > -0.75$ ✓ Assumption verified!

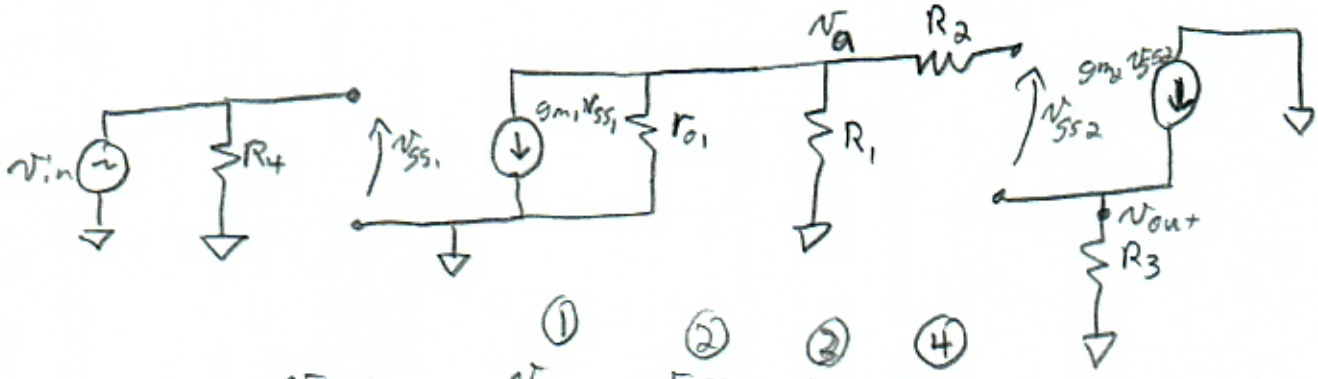
Extra work can be done here, but clearly indicate with problem you are solving.

$$g_{m1} = \frac{51.25e\text{-}6}{\frac{0-(-2.0)}{2}} = 51.25e\text{-}6 \ \Omega^{-1}$$

$$r_{o1} = \frac{\frac{1}{\lambda} + V_{DS}}{I_{DS}} = \frac{100 + 2.5}{51.25e\text{-}6} = 2e6 \ \Omega$$

$$g_{m2} = \frac{7e\text{-}6}{\left(\frac{1.49-0.75}{2}\right)} = 18.9e\text{-}6 \ \Omega^{-1}$$

$$r_{o2} = \infty \quad (\lambda = 0)$$



$$A_v = \frac{v_{out}}{v_{in}} = \underset{①}{\frac{v_{out}}{v_{gs2}}} \ \underset{②}{\frac{v_{gs2}}{v_a}} \ \underset{③}{\frac{v_a}{v_{gs1}}} \ \underset{④}{\frac{v_{gs1}}{v_{in}}}$$

① $v_{out} = g_{m2} v_{gs2} R_3$

$$\frac{v_{out}}{v_{gs2}} = g_{m2} R_3 = (18.9e\text{-}6)(500e3) = 9.46 \ V/V$$

② $v_a = v_{gs2} + g_{m2} v_{gs2} R_3$

$$\frac{v_{gs2}}{v_a} = \frac{1}{1 + g_{m2} R_3} = 0.0957 \ V/V$$

③ $v_a = -g_{m1} v_{gs1} (r_{o1} \| R_1)$

$$\frac{v_a}{v_{gs1}} = -g_{m1} (r_{o1} \| R_1) = -51.25e\text{-}6 \ (2e6 \| 1e6)$$
$$= -34.16\overline{6} \ V/V$$

Extra work can be done here, but clearly indicate with problem you are solving.

(4) $v_{ss1} = v_{in}$

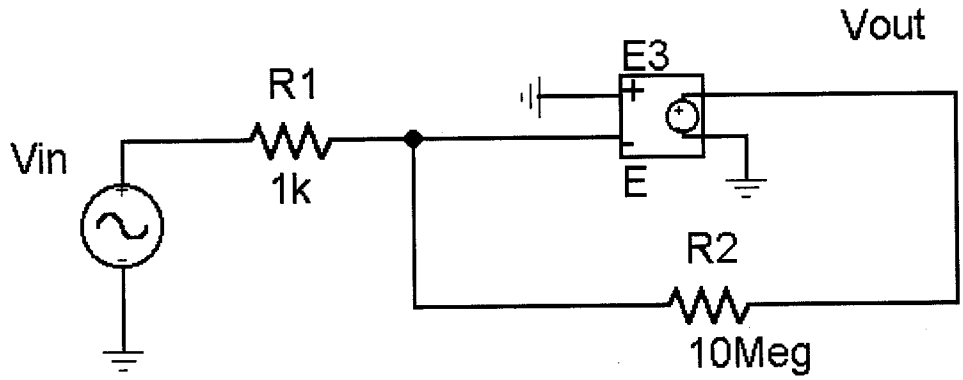
$$\frac{v_{ss1}}{v_{in}} = 1$$

$$A_v = (9.46)(0.0957)(-34.16)(1)$$

$$\boxed{A_v = -30.93 \text{ V/V}}$$

Bonus (10 points)

~~(e. 5 points)~~ A Clemson engineer designed the following circuit using an op-amp with a open loop gain of 10^5 V/V and an open loop bandwidth of 5 Hz to act as a "Yellow Jacket Repeller". It was supposed to output an amplified signal at 22 kHz. Sadly, this Clemson engineer was killed while testing his device on a swarm of killer bees. Please explain why this Clemson engineer's device failed to amplify the signal and include in your answer the maximum –3dB frequency (break frequency) this circuit could operate at. (Note: no yellow jackets were harmed in the making of this problem).



Ideal

Circuit Gain $= \frac{-R_2}{R_1}$

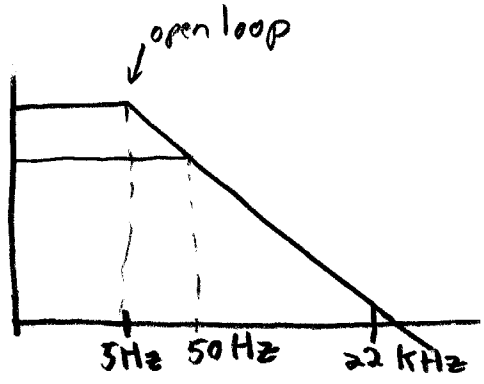
$= -10{,}000$ V

Max -3dB frequency $= f_{max}$

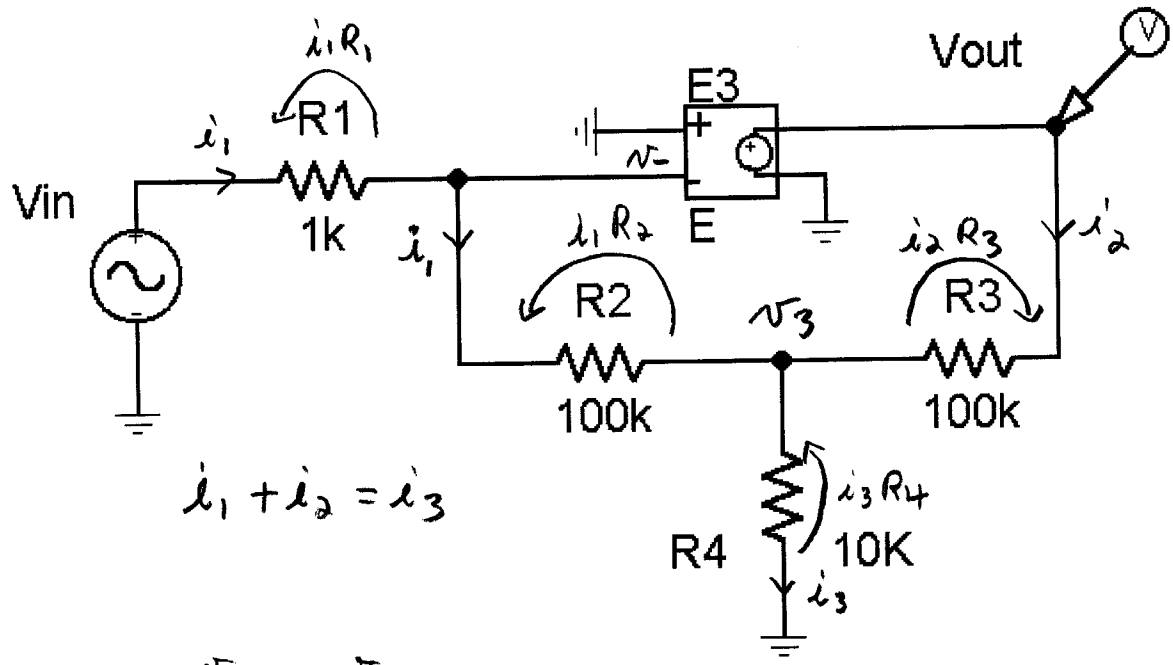
$GBW = |10^5|(5) = |10^4| f_{max}$

$f_{max} = 50$ Hz

Thus the circuit starts loosing gain at 50 Hz!



Bonus (15 points- Absolutely no partial credit)
Determine the voltage gain, v_{out}/v_{in} , of the following amplifier assuming the op-amp is ideal.
Hint: Use the approach we took in class, i.e. use voltage loops and current summation, etc…



$i_1 + i_2 = i_3$

$$\frac{v_{in} - v_-}{R_1} = i_1 \Rightarrow i_1 = \frac{v_{in}}{R_1}$$

$$\frac{v_{out} - v_3}{R_3} = i_2$$

$$v_3 = i_3 R_4 \quad \text{or} \quad i_3 = \frac{v_3}{R_4}$$

Thus,

$$\frac{v_{in}}{R_1} + \frac{v_{out} - v_3}{R_3} = \frac{v_3}{R_4}$$

$$\frac{v_{in}}{R_1} + \frac{v_{out} - (-i_1 R_2)}{R_3} = \frac{-i_1 R_2}{R_4}$$

$$\frac{v_{in}}{R_1} + \frac{v_{out} + \frac{v_{in}}{R_1} R_2}{R_3} = \frac{-\frac{v_{in}}{R_1} R_2}{R_4}$$

or $$\frac{v_{out}}{v_{in}} = -\left(\frac{R_3}{R_1} + \frac{R_2}{R_1} + \frac{R_2 R_3}{R_1 R_4}\right) \text{ V/V}$$

$$\frac{v_{out}}{v_{in}} = -1200 \text{ V/V}$$