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9:38

ECE 3040 Microelectronic Circuits

Exam 3

Nov 25, 2009

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Print your name clearly and largely: Solution

Instructions:
DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your two note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

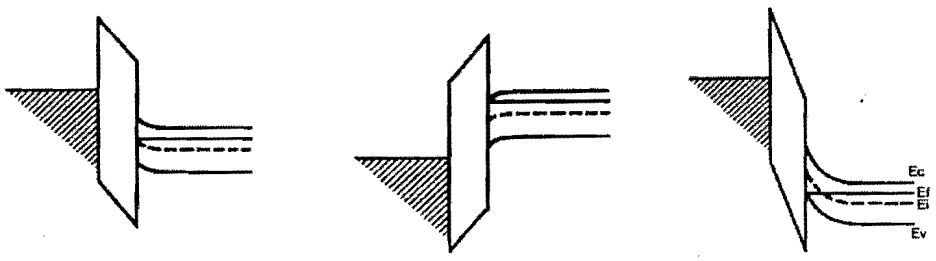
I observed an ethical violation during this exam:

Solution

First 30% **Multiple Choice and True/False (Select the most correct answer)**

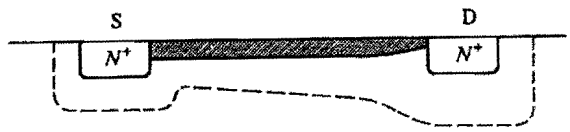
1.) (6-points total) Identify the bias mode of the following MOS capacitors.

(A) Depletion (B) Accumulation (C) Inversion

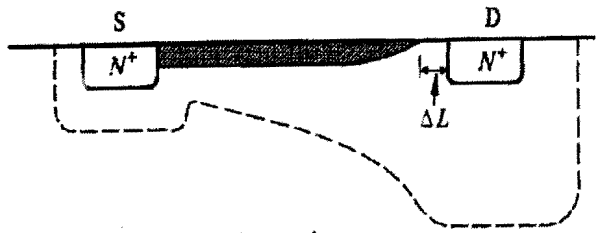


2.) (4-points) True / False: When the enhancement mode MOSFET is biased at threshold ($V_G=V_T$), the surface potential $\phi_S=2\phi_F$, where ϕ_F is dependent on channel doping

3.) (4-points) True / ~~False~~: The transistor to the right has a $V_{DS}>V_{GS}-V_T$.



4.) (4-points) True / False: In the MOSFET transistor to the right, if the drain voltage is increased further than it is in the picture, since the voltage at the end of the pinched off channel is constant, the drain current will be constant.



Accepted either as in hindsight the question is vague

5.) (3-points) True / False: Modern MOS devices are plagued with a problem of a gate oxide so thin it no longer blocks current effectively. Pre Dec. 2008 ⇒ True Post Dec. 2008 ⇒ False (sort of)

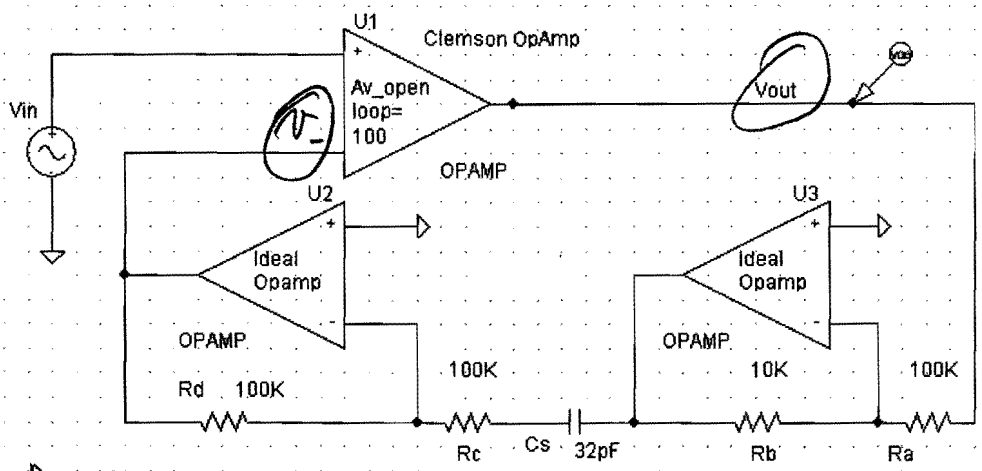
6.) (3-points) True / False: A well designed current amplifier should have a very low output resistance.

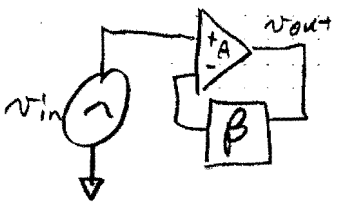
7.) (3-points) True/False: The larger dashed line around the drain compared to the source in the figure for problem 4 indicates a high drain voltage and a large depleted region around the drain contact.

True / False

8.) (3-points) The electrons that reach the end of the NMOS channel are accelerated through the pinch off region by the large drain voltage.

9.) (20-points) Sketch and Label the Bode plot showing the voltage gain in all flat regions and the break frequencies (gain in dB vs Log of Frequency). Opamps U2 and U3 are considered ideal in every way but opamp U1 was made at Clemson so it is ideal in all properties except its open loop gain is only 100 V/V.





$A_{open\,loop} = 100\,V/V$

$$A_{V_{closed}} = \frac{A_{open\,loop}}{1 + \beta A_{open\,loop}}$$

$$\beta = \frac{V_-}{V_{out}} = \left(\frac{-R_b}{R_a}\right)\left(\frac{-R_d}{R_c + \frac{1}{Cs}}\right) = \left(\frac{1}{10}\right)\left(\frac{R_d C_s}{1 + R_c C_s}\right)$$

$$= \left(\frac{1}{10}\right)\left(\frac{s(3.2e\text{-}6)}{1 + s(3.2e\text{-}6)}\right)$$

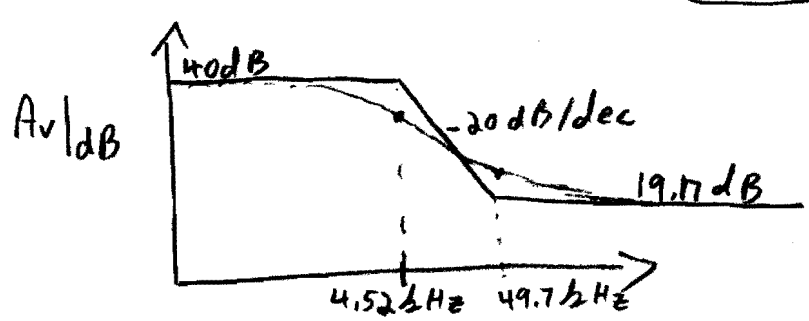
$$A_{V_{closed}} = \frac{100}{1 + 100\left(\frac{1}{10}\right)\left(\frac{s(3.2e\text{-}6)}{1 + s(3.2e\text{-}6)}\right)}$$

$$= \frac{100\,[1 + s(3.2e\text{-}6)]}{1 + s(3.2e\text{-}6) + 10s(3.2e\text{-}6)}$$

$$A_{V_{closed}} = \frac{100\,[1 + s(3.2e\text{-}6)]}{[1 + s(35.2e\text{-}6)]}$$

$$f_{zero} = \frac{1}{2\pi(3.2e\text{-}6)} = 49.7\,kHz$$

$$f_{pole} = \frac{1}{2\pi(35.2e\text{-}6)} = 4.52\,kHz$$



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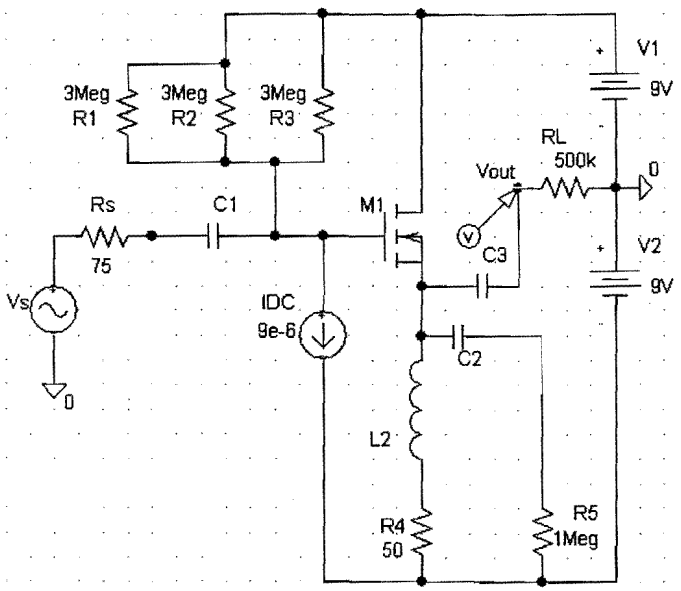
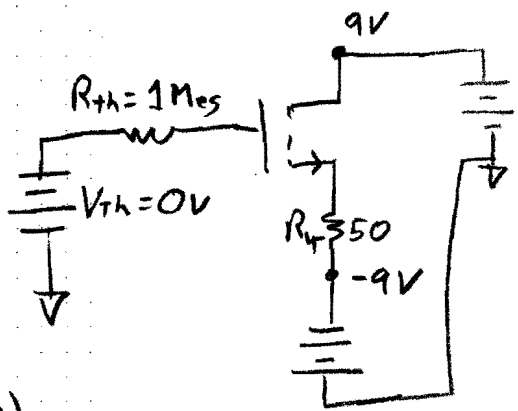
There is a new format for this section. Note 3 separate and unrelated problems remain: Pulling all the concepts together for a useful purpose:

11) (20-points DC Solution) Solve for the Q-point (I_{DS}, V_{GS}, V_{DS}). **SHOW ALL WORK TO GET CREDIT!!!!! DO NOT convert it to the small signal model and DO NOT solve the AC circuit.**





1) $0V = V_{GS} + I_{ds} R_4 - 9V$

$V_{GS} = I_{ds}\,50 + 9V$

2) $I_{DS} = \left(\frac{30e-6}{2}\right)\left(\frac{18}{0.18}\right)(V_{GS}-1.5)^2$

Use the following parameters (note that K, V_T and λ vary with transistor type):

For NMOS Depletion Transistors:
K_n'=20 uA/V^2 **V_T= -4.0V** **λ=0.15 V^{-1}** Length (L)= 0.18 um Width (W)=10 um

For NMOS Enhancement Transistors:
K_n'=30 uA/V^2 **V_T= +1.5V** **λ=0.0 V^{-1}** Length (L)=0.18 um Width (W)=18 um

For PMOS Depletion Transistors:
K_p'=40 uA/V^2 **V_T= +3.0V** **λ=0.0 V^{-1}** Length (L)=0.36 um Width (W)=10 um

For PMOS Enhancement Transistors:
K_p'=50 uA/V^2 **V_T= -0.75V** **λ=0.1 V^{-1}** Length (L)=0.36 um Width (W)=5 um

Putting 1 in 2,

$I_{DS} = 15e-6\,(100)(7.5 - I_{DS}50)^2$

$I_{DS} = 1.5e-3\,(2500 I_{DS}^2 - 750 I_{DS} + \;)$

$0 = 3.75 I_{DS}^2 - 2.125 I_{DS} + 0.084375$

I_{DS}= 42.96 mA or ~~0.523~~ A

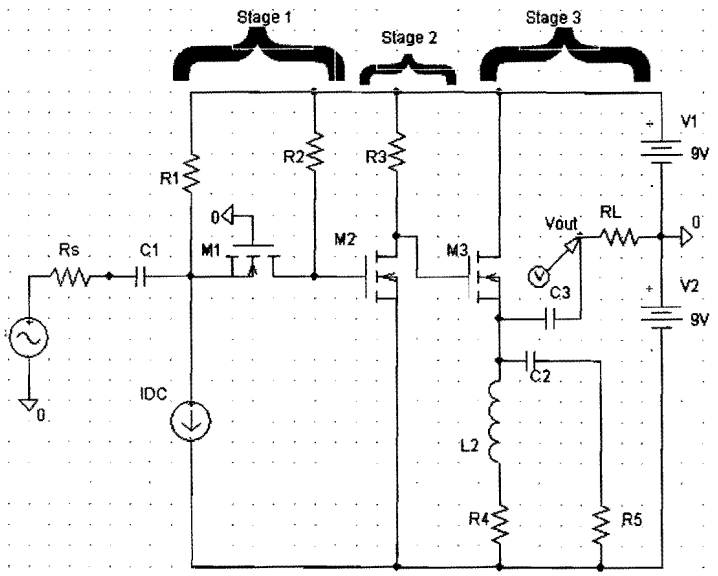
V_{GS} = 6.85V

$V_{DS} = 9 - I_{DS} R_4 + 9 = 15.85V$

$V_{DS} > V_{GS} - V_T$ ✓

12) ***(15-points Conversion to Small Signal Model):*** Given the following circuit, (a) Identify the configuration of ALL the stages of the amplifier (common ____). (b)Convert the circuit to its small signal (AC) equivalent circuit. (c) Solve for all small signal parameters (i.e. the transconductance etc…) for the 1st stage only. You may assume all capacitors have infinite capacitance and all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. **SHOW ALL WORK TO GET CREDIT!!!!! DO NOT solve the ac circuit – just convert it.**

Transistor 1 Q-Point: I_{DS}=1mA, V_T=2V, V_{GS}=3V, and V_{DS}=4V, λ=0.1 V^{-1}
Transistor 2 Q-Point: Not known.
Transistor 3 Q-Point: Not known.



Answers for parts a) and c):

Stage 1: Common Gate

Stage 2: Common Source

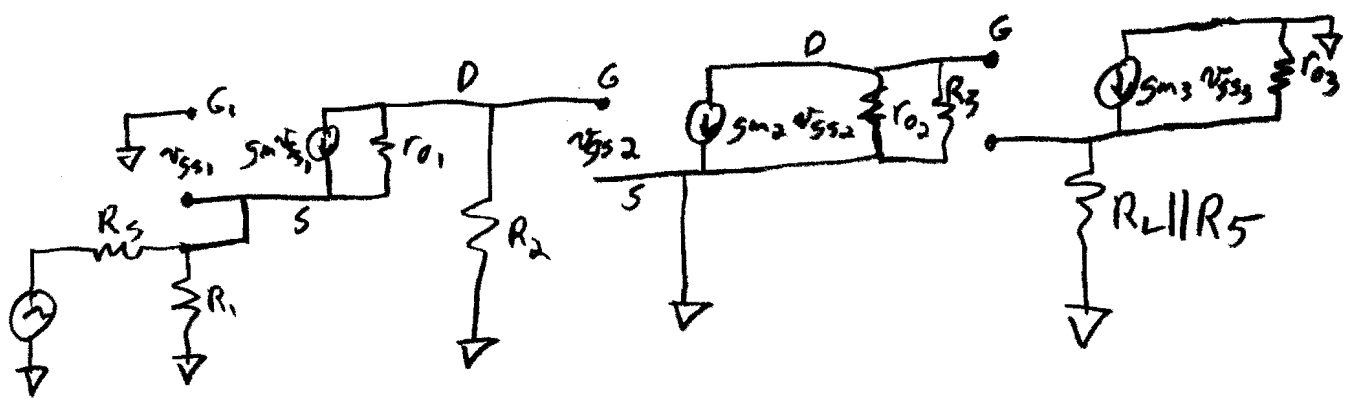
Stage 3: Common Drain

Stage 1: g_{m1}= 2mA/V

Stage 1: r_o= 14 kΩ

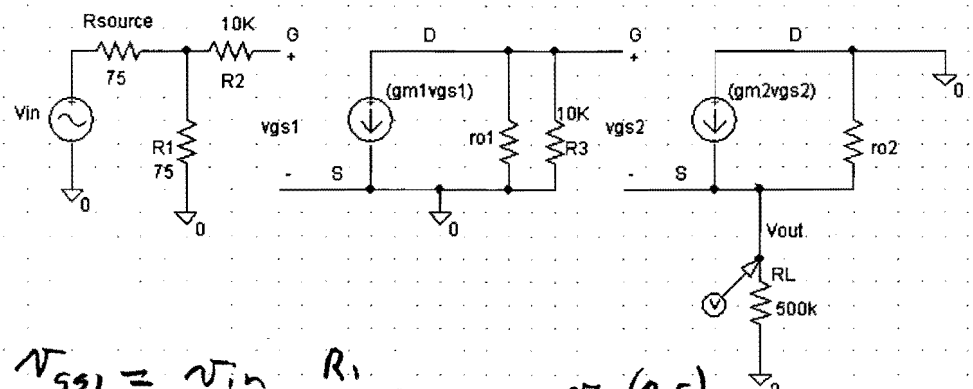
$$g_{m_1} = \frac{I_{DS_1}}{\left(\frac{V_{GS}-V_T}{2}\right)} = \frac{1mA}{\frac{3-1}{2}} = 2mA/V$$

$$r_o = \frac{V_{DS} + \frac{1}{\lambda}}{I_{DS}} = \frac{4+10}{1mA} = 14{,}000\,\Omega$$



13) (20-points) Given the following circuit, a) (15 points) what is the AC voltage gain, V_{out}/V_{in}? b) (5 points) What is the input resistance? **SHOW ALL WORK TO GET CREDIT!!!!!**

Transistor 1: g_{m1}=1mA/V, r_{o1}=52KΩ
Transistor 2: g_{m2}=3mA/V, r_{o2}=∞



1) $v_{gs1} = v_{in}\dfrac{R_1}{R_1+R_{source}} = v_{in}(0.5)$

2) $v_{g2}\,(not\ v_{gs2}) = -(g_{m1}v_{gs1})(r_{o1}\|R_3) = -v_{gs1}(8.38)$

3) $v_{g2} = v_{gs2} + v_{out}$

4) $v_{out} = (g_{m2}v_{gs2})(r_{o2}\|R_L) = v_{gs2}(1500)$

(4 into 3)

$$v_{g2} = v_{gs2}\left[1 + g_{m2}(r_{o2}\|R_L)\right] = v_{gs2}[1501]$$

$$A_v = \left(\frac{v_{out}}{v_{gs2}}\right)\left(\frac{v_{gs2}}{v_{g2}}\right)\left(\frac{v_{g2}}{v_{gs1}}\right)\left(\frac{v_{gs1}}{v_{in}}\right)$$

$$= \left[g_{m2}(r_{o2}\|R_L)\right]\left[\frac{1}{1+g_{m2}(r_{o2}\|R_L)}\right]\left[-g_{m1}(r_{o1}\|R_3)\right]\left[\frac{R_1}{R_1+R_{source}}\right]$$

$$= \left(\frac{1500}{1501}\right)(-8.38)(0.5)$$

$A_v = -4.19\ V/V$

$R_{in} = 75\,\Omega$