ECE 3040 Microelectronic Circuits

Exam 3

April 18, 2002

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Print your name clearly and largely: Solutions

Instructions:
Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

***First 25%* Multiple Choice, True/False (Select the most correct answer)**

1.) (3-points) The gate current in the MOSFET is
- a.) Highest under large positive gate bias
- b.) Highest under large negative gate bias
- c.) Is determined by the change in fermi level position at the semiconductor-oxide interface
- d.) Is always zero
- e.) Is zero except in inversion

2.) (3-points) A depletion mode PMOS transistor has a…
- a.) …p-type substrate.
- b.) …n-type substrate
- c.) n-type channel when biased into cutoff (either depletion or accumulation)
- d.) huge gate current.

3.) (4-points each, 12-points total) For the three transistor cross-sections I, II and III shown below, answer each of the three questions a-c:

I. II. III.

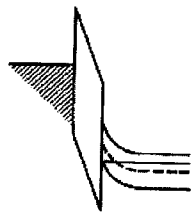
a.) For $V_{GS}>V_{DS}>0$ which cross-sectional view (I, II or III) is correct. II

b.) For $0<V_{GS}<V_{GS}-Vt<V_{DS}$ which cross-sectional view (I, II or III) is correct. I

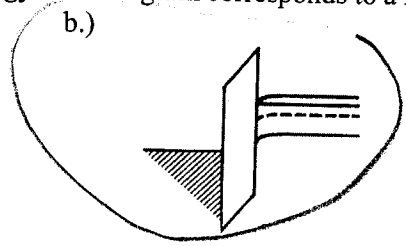
c.) For $V_{GS}<0$ and $V_{DS}>0$ which cross-sectional view (I, II or III) is correct. . III

4.) (4-points) Which energy band diagram corresponds to a PMOS capacitor biased into accumulation.

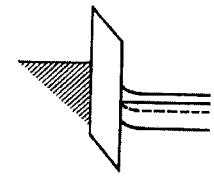
a.)



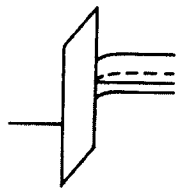
b.)



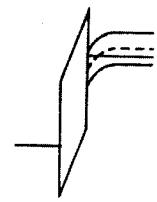
c.)



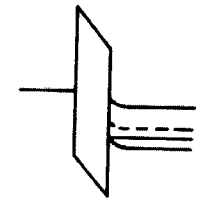
d.)



e.)



f.)



5.) (3-points) For a Transresistance amplifier designed for maximum gain (circle all that apply):
- a.) You should have a high input impedance?
- b.) You should have a low input impedance?
- c.) You should have a high output impedance?
- d.) You should have a low output impedance?
- e.) The output is a voltage

p-type substrate

Second 10% Short Answer:

6.) (10 points) A NMOS transistor at room temperature has an oxide thickness of 1000 angstroms (1 angstrom $=10^{-8}$ cm), determine the doping required to make the transistor begin conducting at 0.75 V. Use the following:

Substrate relative Dielectric Constant, $\varepsilon_{r\text{-semiconductor}}=K_S=11.7$
Oxide relative Dielectric Constant, $\varepsilon_{r\text{-oxide}}=K_{ox}=3.9$
Dielectric Constant of free space, ε_O =8.854e-14 F/cm
Substrate intrinsic concentration, n_i=1e10 cm^{-3}
Also recall that the total dielectric constant of the semiconductor is: $\varepsilon_s=\varepsilon_{r\text{-semiconductor}}\varepsilon_O$ while the total dielectric constant for the oxide is: $\varepsilon_{ox}=\varepsilon_{r\text{-oxide}}\varepsilon_o$

$$C_{ox}=\frac{\epsilon_{ox}}{X_{ox}}=\frac{3.9(8.854e\text{-}14)\ F/cm}{1000\times10^{-8}\ cm}=3.45e\text{-}8\ F/cm^2$$

$$\phi_F=\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\rightarrow 0.0259\ln\left(\frac{N_A}{1e10}\right)$$

$$V_T=2\phi_F+\frac{\epsilon_{si}}{C_{ox}}\sqrt{\frac{2qN_A}{\epsilon_s}(2\phi_F)}$$

$$0.75=2\phi_F+\frac{11.7(8.854e\text{-}14)\ F/cm}{3.45e\text{-}8\ F/cm^2}\sqrt{\frac{2(1.6e\text{-}9c)N_A(2)\phi_F}{(11.7)(8.854e\text{-}14)\ F/cm}}$$

$$0.75=2\phi_F+3e\text{-}5\sqrt{(6.178e\text{-}7)\phi_F N_A}$$

V_T	ϕ_F	N_A
1.003	0.298	1e15
0.592	0.239	1e14
0.839	0.280	5e14
0.716	0.262	2.5e14
0.745	0.267	3e14
0.750	0.268	3.1e14

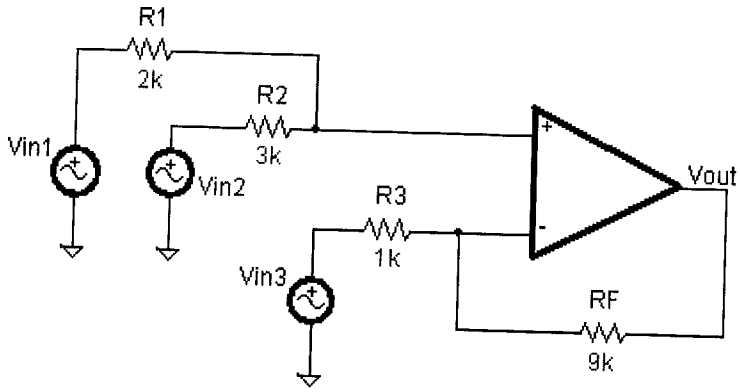
$N_A \sim 3.1e14\ cm^{-3}$

Problems (3rd 20%)

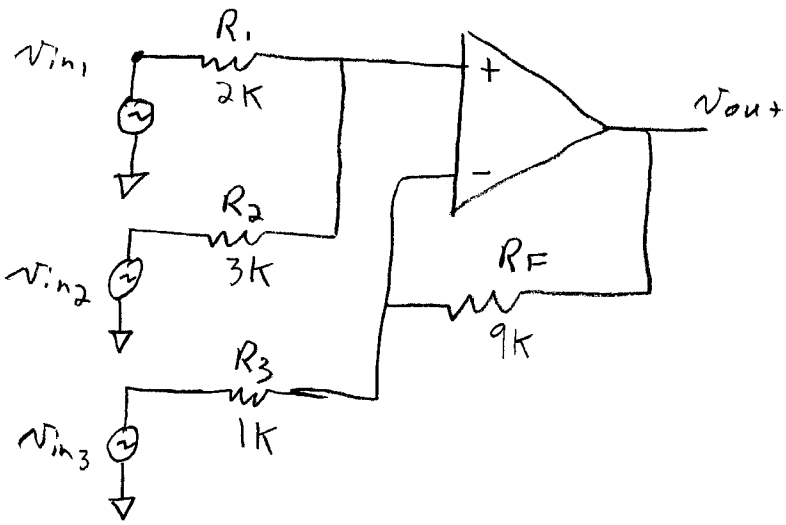
7.) You may assume that the **Op-Amps are ideal**.

a.) (15-points) Determine an equation relating the output voltage, Vout in terms of the three input voltages, Vin1, Vin2, Vin3.

b.) (5-points) Determine the input impedance seen by the source Vin3.

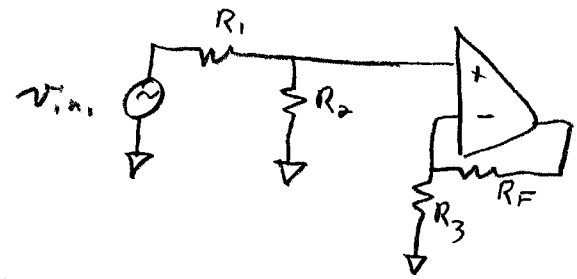


Extra work can be done here, but clearly indicate with problem you are solving.



Using Superposition:

step 1: Let $V_{in2} = V_{in3} = 0$

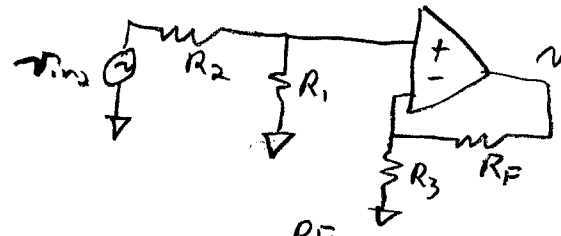


voltage divider on + input

$$V_{out} = V_{in1}\left(\frac{R_2}{R_1+R_2}\right)\left(1+\frac{R_F}{R_3}\right)$$

Non-inverting stage

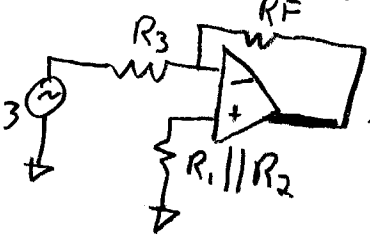
Step 2: Let $V_{in1} = V_{in3} = 0$



$$V_{out} = V_{in2}\left(\frac{R_1}{R_1+R_2}\right)\left(1+\frac{R_F}{R_3}\right)$$

Step 3:

(let $V_{in2} = V_{in1} = 0$)



$$V_{out} = V_{in3}\left(-\frac{R_F}{R_3}\right)$$

$$V_{out} = V_{in1}\left(\frac{R_2}{R_1+R_3}\right)\left(1+\frac{R_F}{R_3}\right) + \ldots$$

$$\ldots V_{in2}\left(\frac{R_1}{R_1+R_2}\right)\left(1+\frac{R_F}{R_3}\right) + \ldots$$

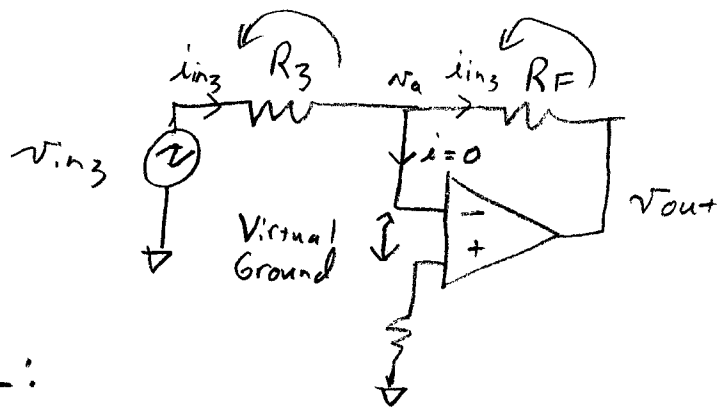
$$\ldots \left(-V_{in3}\frac{R_F}{R_3}\right)$$

Extra work can be done here, but clearly indicate with problem you are solving.

$$v_{out} = v_{in_1}\left(\frac{3}{5}\right)(10) + v_{in_2}\left(\frac{2}{5}\right)(10) - v_{in_3}\,9$$

$$\boxed{v_{out} = 6v_{in_1} + 4v_{in_2} - 9v_{in_3}}$$

R_{in_3}



Method 1:

Since the virtual ground assures $v_a = 0$, $R_{in_3} = R_3$ or

Method 2: $v_{out} + i_{in_3}(R_F + R_3) = v_{in_3}$

$$+\quad v_{out} = -\frac{R_F}{R_3} v_{in_3}$$

$$\Longrightarrow \quad -v_{in_3}\frac{R_F}{R_3} + (R_F + R_3)\, i_{in_3} = v_{in_3}$$

$$v_{in_3}\left(1 + \frac{R_F}{R_3}\right) = i_{in_3}(R_F + R_3)$$

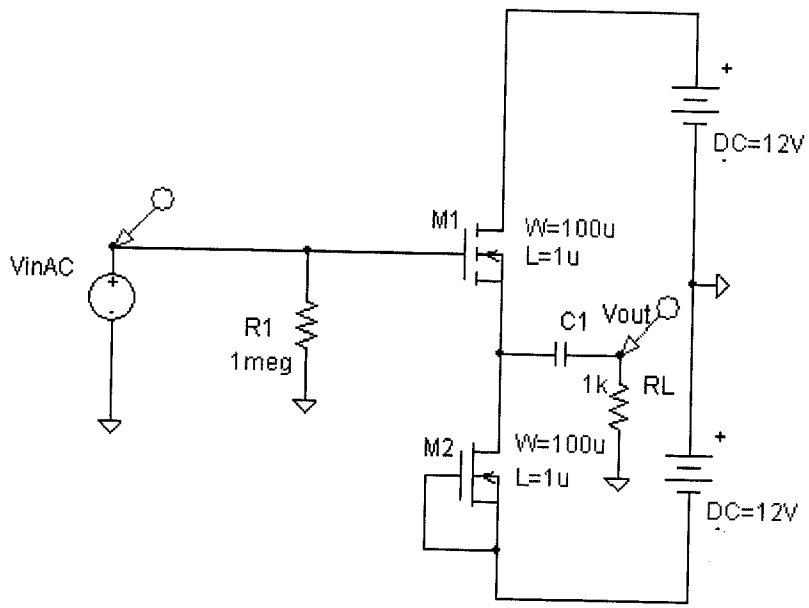
$$R_{in_3} = \frac{v_{in_3}}{i_{in_3}} = \frac{R_3}{R_F + R_3}(R_F + R_3)$$

$$\boxed{R_{in_3} = R_3}$$

Pulling all the concepts together for a useful purpose: (4th portion)

8.) ***(45-points)*** Given the following circuit, what is the AC voltage gain, V_{out}/V_{inAC}? You may assume all capacitors have infinite capacitance and are thus, AC shorts. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: 20 points for DC solution (***V_{GS}, V_{DS} along with I_{DS} for both transistors***), 5 points for the conversion to the small signal model and 20 points for the small signal analysis.

Hint: Assume and then verify that both transistors are saturated. If M2 is saturated, identify it's functionality (i.e. what is M2 being used for) in the DC circuit.
Do not panic! Performing this identification will make the AC solution easier but is not necessary to get the correct answer.



Use the following parameters:
For NMOS Depletion Transistors:
M2→ K_n'=20 uA/V^2 V_T=-1.0V λ=0.0 V^{-1} Length (L)=1 um Width (W)=100 um
M1→ For NMOS Enhancement Transistors:
K_n'=20 uA/V^2 V_T=1.0V λ=0.0 V^{-1} Length (L)=1 um Width (W)=100 um
For PMOS Depletion Transistors:
K_p'=40 uA/V^2 V_T=+3.0V λ=0.1 V^{-1} Length (L)=10 um Width (W)=10 um
For PMOS Enhancement Transistors:
K_p'=40 uA/V^2 V_T=-3.0V λ=0.1 V^{-1} Length (L)=10 um Width (W)=10 um

Extra work can be done here, but clearly indicate with problem you are solving.

DC solution:

M1 ⇒ NMOS Enhancement $\lambda = 0$, $K_n = 20e\text{-}6$, $V_{TN} = 1$

M2 = NMOS Depletion $\lambda = 0$, $K_n = 20e\text{-}6$, $V_{TN} = -1$

M2 is always saturated, (Note $V_{DS} > V_{GS} - V_T$ → always positive $> 0 - 1$)

$$I_{DS_2} = I_{DS_1} = \frac{K_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

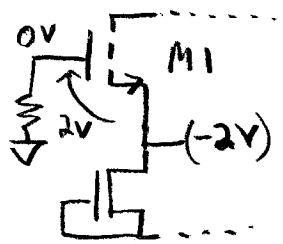
$$= \frac{20e\text{-}6}{2}\left(\frac{100\,\mu m}{1\,\mu m}\right)(0 - (-1))^2(1 + 0)$$

$$\boxed{I_{DS2} = I_{DS1} = 1\,mA}$$

$$1\,mA = I_{DS_1} = \left(\frac{20e\text{-}6}{2}\right)\left(\frac{100\,\mu m}{1\,\mu m}\right)(V_{GS} - 1)^2(1 + 0)$$

$$1 = (V_{GS} - 1)^2$$

$$V_{GS} - 1 = 1$$



$$\boxed{V_{GS} = 2\,V}$$

$$\boxed{V_{DS} = 12 - (-2V) = 14V}$$

M1 Saturation assumption is verified:

$$(V_{DS} > V_{GS} - V_{TN}) \Rightarrow (14 > (2V - 1V))$$

M2:

$$\boxed{\begin{aligned} V_{DS} &= 10V \\ V_{GS} &= 0 \\ I_{DS} &= 1mA \end{aligned}}$$

$V_{D_2} = -2V \qquad V_{S_2} = -12V$

$V_{DS} = -2V - (-12) = 10V$

$V_{DS} > V_{GS} - V_{TN}$

$10V > 0 - (-1)$

$10V > 1 \Rightarrow$ Assumption verified

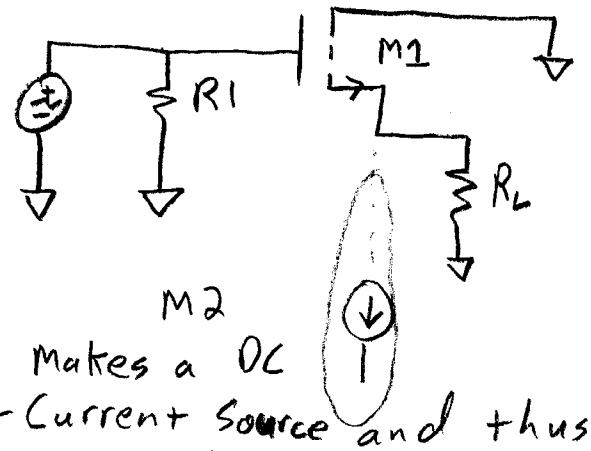
Extra work can be done here, but clearly indicate with problem you are solving.

AC Solution:

$$g_{m_1} = \frac{I_{DS_1}}{\left(\frac{V_{GS} - V_T}{2}\right)} = \frac{2mA}{2-1}$$

$$g_{m_1} = 2e\text{-}3\,S \quad \left(\frac{1}{0}\right)$$

$$r_{o_1} = \infty \left(= \frac{\frac{1}{\lambda} + V_{DS_1}}{I_{DS_1}}\right)$$

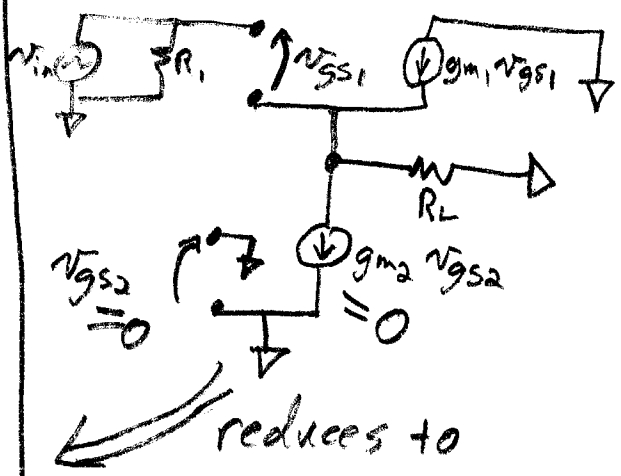


M2 makes a DC current source and thus is an AC open circuit

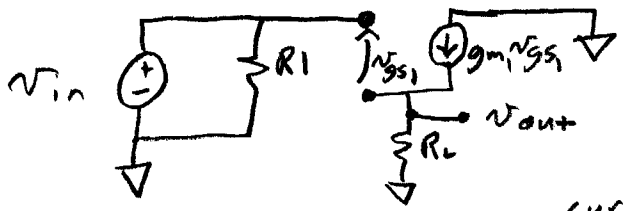
Saturated with V_{GS} = constant

I_{DS} = constant

If you did not recognize M2 forms a current source



reduces to



current through R_L

$$V_{in} = V_{gs_1} + (g_{m_1} V_{gs_1}) R_L$$

$$= V_{gs_1} (1 + g_{m_1} R_L)$$

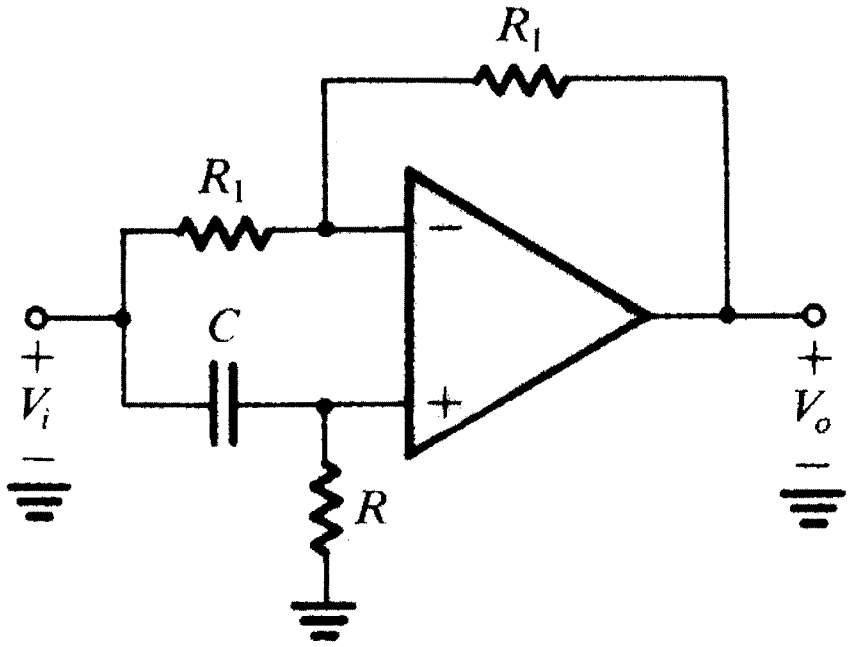
$$\frac{V_{gs_1}}{V_{in}} = \frac{1}{1 + g_{m_1} R_L} = \frac{1}{1+2} = \frac{1}{3}$$

$$V_{out} = g_m V_{gs_1} R_L$$

$$\frac{V_{out}}{V_{gs_1}} = g_m R_L = 2$$

$$A_v = \left(\frac{V_{out}}{V_{gs_1}}\right)\left(\frac{V_{gs_1}}{V_{in}}\right) = \frac{g_m R_L}{1 + g_m R_L} = \frac{2}{3} \text{ V/V}$$

Bonus: (10-points - Absolutely no partial credit) Determine an expression for ~~and sketch the frequency~~ the transfer voltage gain, Vo/Vi ~~in dB~~.



By superposition,

$$v_{out} = \left(\frac{R}{R + \frac{1}{Cs}}\right)\left(1 + \frac{R_1}{R_1}\right)v_{in} - \frac{R_1}{R_1}v_{in}$$

Voltage divider on + input

$$\frac{v_{out}}{v_{in}} = \frac{2RCs}{1+RCs} - 1$$

$$= \frac{2RCs - (RCs+1)}{1+RCs}$$

$$\frac{v_{out}}{v_{in}} = \frac{RCs - 1}{RCs + 1} \quad v/v$$