ECE 3040 Microelectronic Circuits

Exam 3

April 23, 2007

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Print your name clearly and largely: Solutions

Instructions:
DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheet from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

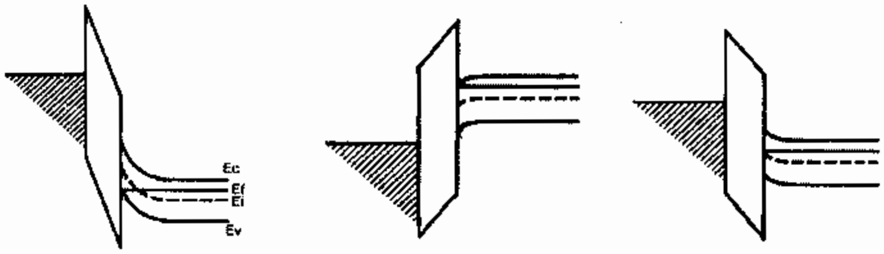
I DID NOT observe any ethical violations during this exam: __________

I observed an ethical violation during this exam: __________

First 30% **Multiple Choice and True/False (Select the most correct answer)**

1.) (6-points total) Identify the bias mode of the following MOS capacitors.

(A) Inversion (B) Accumulation (C) Depletion



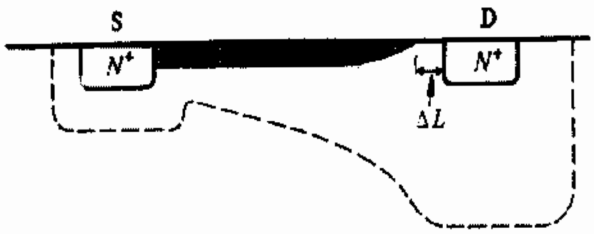
2.) (4-points) For the three capacitors in problem 1, which is true:

a) They could be used to make a NMOS MOSFET
b) They could be used to make a PMOS MOSFET
c) The diagrams clearly show the Source-Gate bias
d) The diagrams clearly show the Drain-Gate bias
e) The diagrams clearly show the Body-Gate bias

3.) (4-points) True / False: An enhancement mode NMOS MOSFET was invented after the depletion mode NMOS MOSFET and can conduct current in it's drain-source circuit even with V_{GS}=0 volts.

4.) (4-points) In the MOSFET transistor to the right, what is the voltage across the pinched off region?

a.) V_{GS}-V_T
b.) V_{DS}
c.) $V_{D\text{-}sat}$
d.) V_{DS}-V_{Dsat}
e.) Not enough information given to solve



5.) (3-points) True / False: A well designed current amplifier should have a very low input resistance.

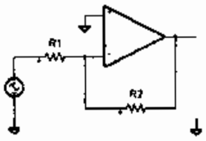
6.) (9-points) Name three improvements that feedback can do to a voltage amplifier

a) Increase Bandwidth (freq. response)
b) Increase input resistance
c) Decrease output resistance

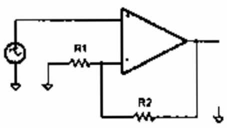
others ... Allows finite Gain
Creates a Virtual Ground

7.) (20-points) Sketch and label all break frequencies, the voltage gain in flat regions in a Bode plot (gain in dB vs Log(frequency)). ***You may assume that this "Clemson Designed" Op-Amp is ideal in every way EXCEPT that its open loop gain is an atrocious 200 V/V.*** To receive full credit the asymptotes and an estimate of the actual gain curve should BOTH be sketched on the same plot. <u>*Hint: you may find it helpful to determine the feedback factor, β as part of your solution. Also, to make the math easier, please note that ~~R1=R2 and C1=C2.~~*</u> $R_1C_1 = R_2C_2$

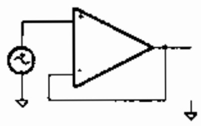
You may also use the following results for the three standard op-amp configurations but these results may or may not be needed for this problem.



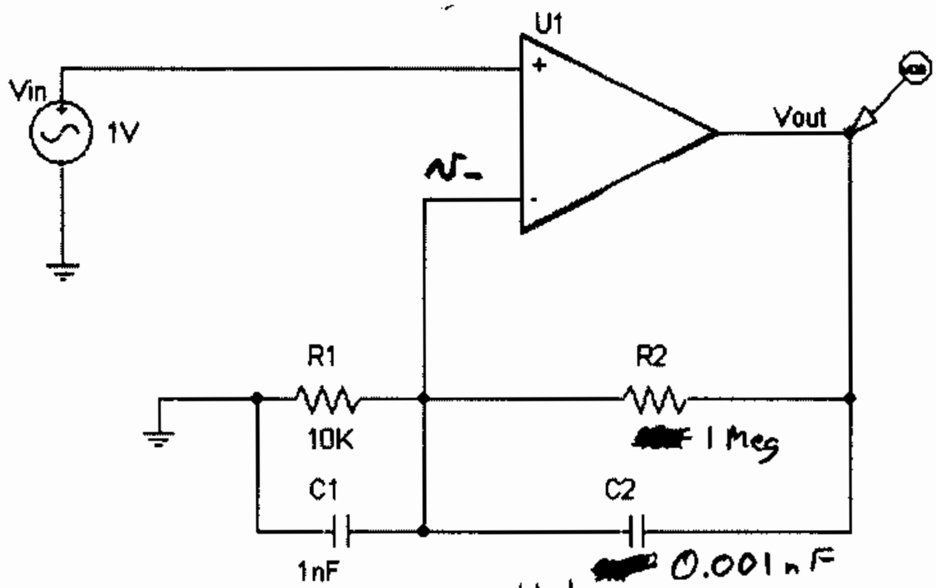
$A_v = V_{out}/V_{in} = -(R2/R1)$



$A_v = V_{out}/V_{in} = 1+(R2/R1)$



$A_v = V_{out}/V_{in} = 1$



$$\beta = \frac{v_-}{v_{out}} = \frac{R_1 \| \frac{1}{C_1 s}}{R_1 \| \frac{1}{C_1 s} + R_2 \| \frac{1}{C_2 s}}$$

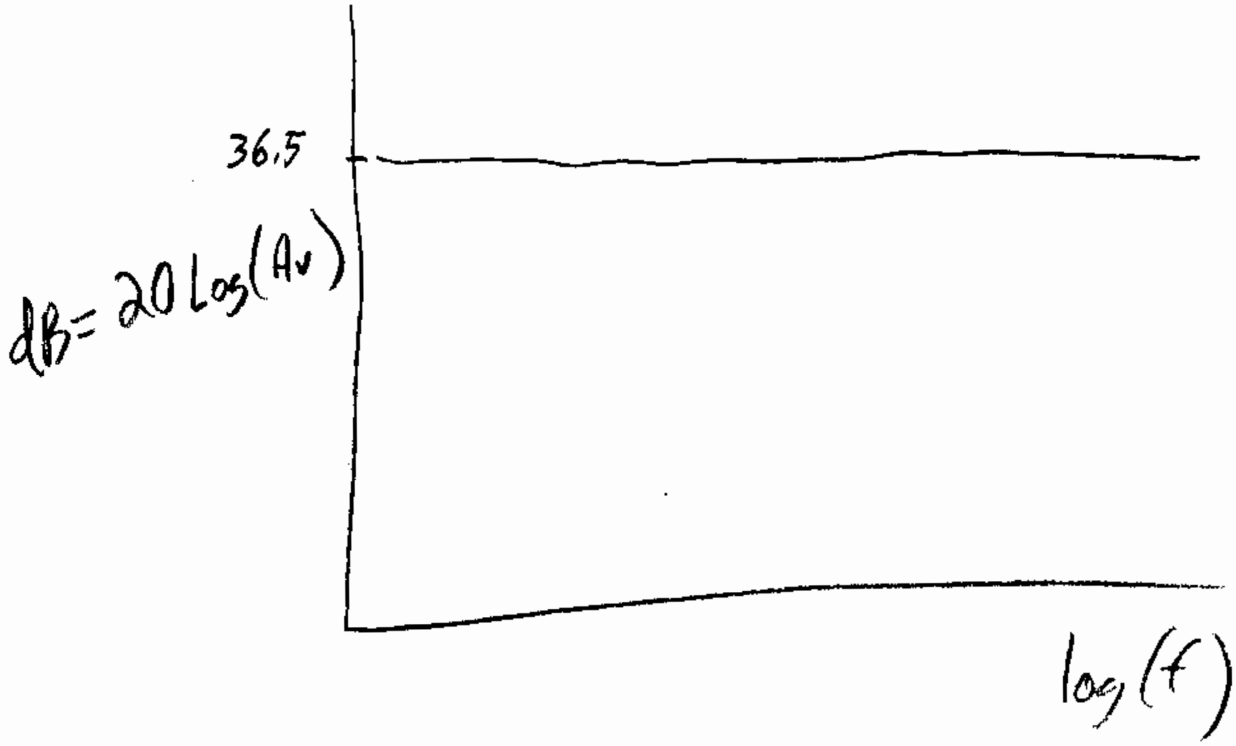
$$\beta = \frac{\frac{R_1}{1+R_1C_1s}}{\left(\frac{R_1}{1+R_1C_1s}\right) + \left(\frac{R_2}{1+R_2C_2s}\right)} = \frac{R_1}{R_1 + R_2\left(\frac{1+R_1C_1s}{1+R_2C_2s}\right)} = \frac{R_1}{R_1+R_2}$$

$$= 0.\overline{0099}$$

$$\boxed{A_{closed} = \frac{A_{open}}{(1+\beta A_{open})} = \frac{200}{1+0.\overline{0099}(200)} \quad 67.1\ V/V}$$

Note: $A_v \neq 1 + \frac{R_2}{R_1} = 101$

Extra work can be done here, but clearly indicate with problem you are solving.



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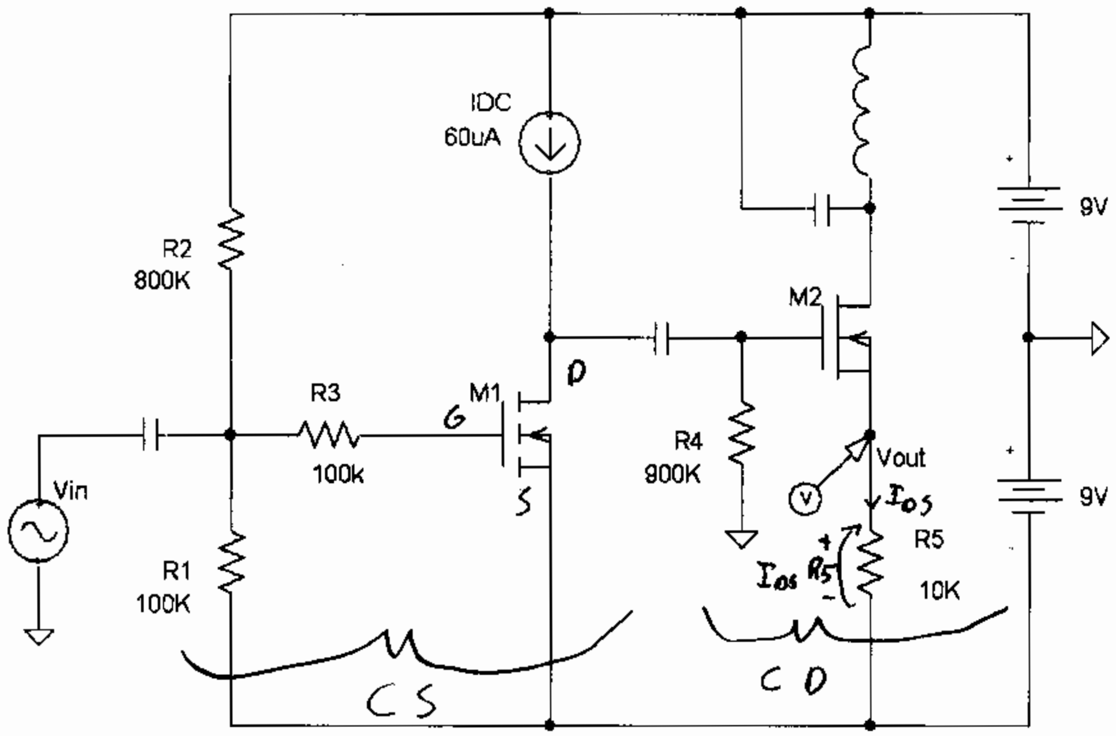
Pulling all the concepts together for a useful purpose:

8.) ***(50-points)*** Given the following circuit, (a) Identify the configuration of ***BOTH*** of the two stages (common ____). (b) What is the AC voltage gain, V_{out}/V_{in}? You may assume all capacitors have infinite capacitance. You may assume all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances.
Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain current), 9 points for the conversion to the small signal model and 18 points for small signal analysis.



Use the following parameters (note that V_T and λ vary with transistor type):

M2 For NMOS Depletion Transistors:
K_n'=20 uA/V^2 **V_T= -4.0V** **λ=0.0 V^{-1}** Length (L)=10 um Width (W)=10 um

M1 For NMOS Enhancement Transistors:
K_n'=30 uA/V^2 **V_T= +0.75V** **λ=0.1 V^{-1}** Length (L)=10 um Width (W)=10 um

For PMOS Depletion Transistors:
K_p'=40 uA/V^2 **V_T= +3.0V** **λ=0.0 V^{-1}** Length (L)=10 um Width (W)=10 um

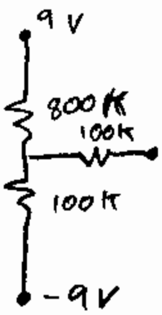
For PMOS Enhancement Transistors:
K_p'=50 uA/V^2 **V_T= -1.75V** **λ=0.1 V^{-1}** Length (L)=10 um Width (W)=10 um

Part a) Stage 1 Common Source
Stage 2 Common Drain

Extra work can be done here, but clearly indicate with problem you are solving.

DC:

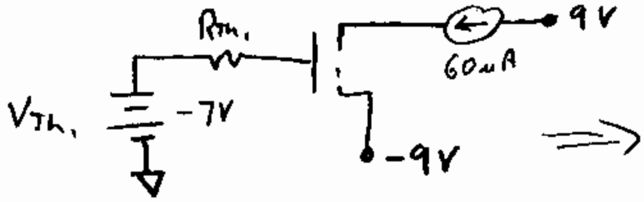
Stage 1:



$$V_{Th_1} = 9\left(\frac{100k}{100k+800k}\right) + (-9)\left(\frac{800k}{100k+800k}\right) = 1 - 8$$

$$V_{Th_1} = -7V$$

$$R_{Th_1} = R_3 + R_1 || R_2 = 100k + 188.\bar{8}k$$



$\Longrightarrow$ $\boxed{V_{GS_1} = 2V}$

$$I_{DS} = 60\mu A = \left(\frac{10}{10}\right)\frac{1}{2}(30e\text{-}6)(V_{GS} - 0.75)^2(1 + 0.1(V_{DS}))$$

$$60\mu A = 15e\text{-}6\,(2 - 0.75)^2(1 + 0.1V_{DS})$$

$$\boxed{V_{DS_1} = 15.6V}$$

Assumption: $(V_{GS} - V_T) = (2 - 0.75) = 1.25V < V_{DS} = 15.6V$ ✓

Stage 2:

$V_G = 0V$
$V_D = +9V$ $\Longrightarrow$ $V_{GS} = -(-9 + I_{DS}R_5) = (9 - I_{DS}R_5)$

$V_{DS} = 9V - (-9 + I_{DS}R_5)$

D-NMOS

$V_{DS} = 18V - I_{DS}R_5$

$$I_{DS} = \left(\frac{10}{10}\right)\frac{1}{2}(20e\text{-}6)(V_{GS} - (-4))^2(1 + 0(V_{DS}))$$

$$= (10e\text{-}6)(V_{GS}^2 + 8V_{GS} + 16)$$

$$I_{DS} = 10e\text{-}6\,(81 - 18I_{DS}R_5 + I_{DS}^2R_5^2 + 72 - 8I_{DS}R_5 + 16)$$

$$I_{DS} = 1.69e\text{-}3 - 2.6\,I_{DS} + I_{DS}^2\,1000$$

$$0 = 1000I_{DS}^2 - 3.6\,I_{DS} + 1.69e\text{-}3$$

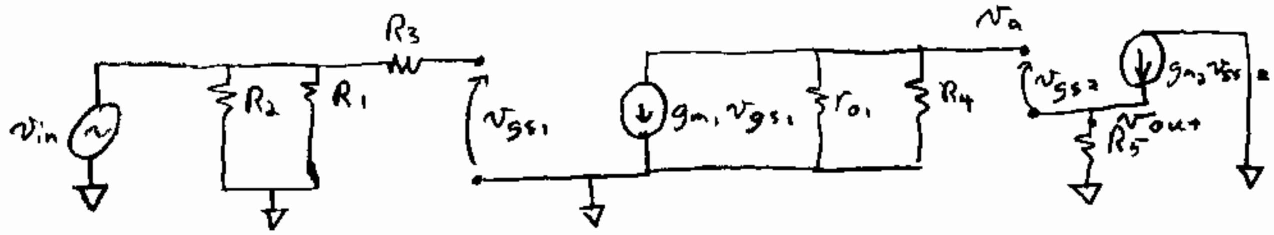
$$I_{DS} = \frac{3.6 \pm \sqrt{(3.6)^2 - 4\,1000\,(1.69e\text{-}3)}}{2(1000)}$$

$I_{DS} = 555\mu A$ or $3.0\cancel{4}\overset{2}{}\,mA$

$\boxed{\text{Try } 555\mu A:\ V_{GS} = 3.45\,V \quad V_{DS} = 12.45\,V}$ $V_{GS} - (-4) = 7.45V < V_{DS} = 12.45V$ ✓

Extra work can be done here, but clearly indicate with problem you are solving.

Convert to Small signal Model:



$$g_{m1} = \frac{I_{DS1}}{\left(\frac{V_{GS}-V_T}{2}\right)} = 9.6e\text{-}5\ \Omega^{-1} \qquad g_{m2} = \frac{555\,\mu A}{\frac{3.45-(-4)}{2}} = 1.48e\text{-}4\ \Omega^{-1}$$

$$(r_{o1})^{-1} = \frac{I_{DS}}{\frac{1}{\lambda} + V_{DS}} = \frac{60e\text{-}6}{10 + 15.6} = \qquad r_{o2} = \infty$$

$$\Downarrow$$

$$r_{o1} = 426.\bar{6}K$$

AC Solution

$$v_{gs1} = v_{in}$$

$$v_a = -(g_{m1} v_{gs1})(r_{o1} \| R_4)$$

$$v_a = g_{m2} v_{gs2} R_5 + v_{gs2} = (1 + g_{m2} R_5)\, v_{gs2}$$

$$v_{out} = + g_m v_{gs2} R_5$$

$$A_v = \left(\frac{v_{gs1}}{v_{in}}\right)\left(\frac{v_a}{v_{gs1}}\right)\left(\frac{v_{gs2}}{v_a}\right)\left(\frac{v_{out}}{v_{gs2}}\right)$$

$$= (1)\left(-g_{m1}(r_o \| R_4)\right)\left(\frac{1}{1 + g_{m2} R_5}\right)(g_m R_5)$$

$$= -(9.6e\text{-}5)(426.\bar{6}K \| 900K)\left(\frac{1}{1 + 1.489}\right)(1.489)$$

$$\boxed{A_v = -16.62\ V/V}$$