ECE 3040 Microelectronic Circuits

Exam 3

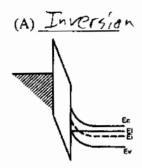
April 18, 2008

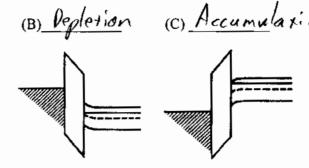
Dr. W. Alan Doolittle

Print your name clearly and largely: Solutions
Instructions: DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your two note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!
Sign your name on <u>ONE</u> of the two following cases:
I DID NOT observe any ethical violations during this exam:
I observed an ethical violation during this exam:

First 30% Multiple Choice and True/False (Select the most correct answer)

1.) (6-points total) Identify the bias mode of the following MOS capacitors.





2.) (4-points) For a MOS Capacitor...

a) ...it can be used to form a charge storage element in a memory circuit.

(all 4)

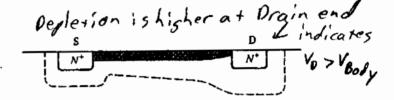
b) ...it can be used as a frequency tuning element in an amplifier.

c) Lit's capacitance will never be greater than when biased into accumulation.

dy ...it's capacitance will never be smaller than when biased in inversion.

e) None of the above.

3.) (4-points) True / False The transistor to the right is biased in linear/triode mode and has a zero volt VDS.



4.) (4-points) In the MOSFET transistor to the right, what is the voltage norces the _pinched off region? -

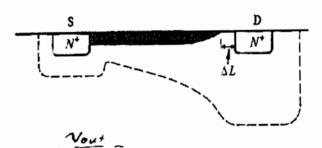
 $\underline{a.)} \quad V_{GS}-V_T > \overline{V}_{DS}$

b.) V_{DB} is reverse biased

 \overline{c} $V_{DS}>V_{Dsat}$ $(T_{\rm GS} - V_{\rm T} < V_{\rm DS})$

e.) Not enough information given to solve

lrue

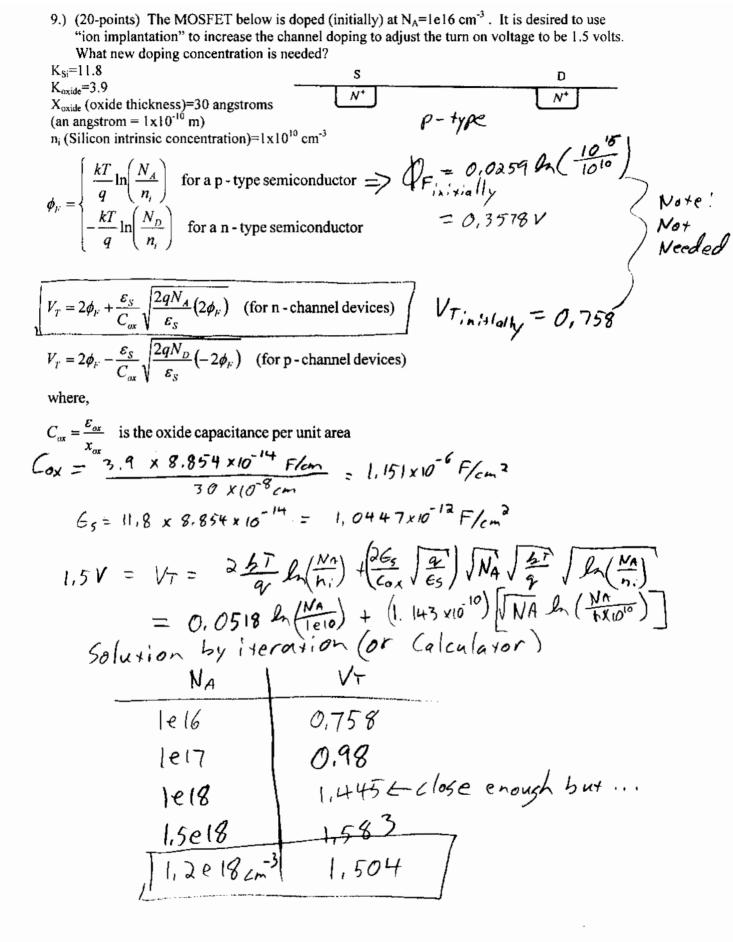


5.) (3-points) True/ False: A well designed transresistance amplifier should have a very low input resistance. Get Current into the amplifier

6.) (3-points) True/ False: A well designed transresistance amplifier should have a very low output resistance. Get all voltage delivered to the load

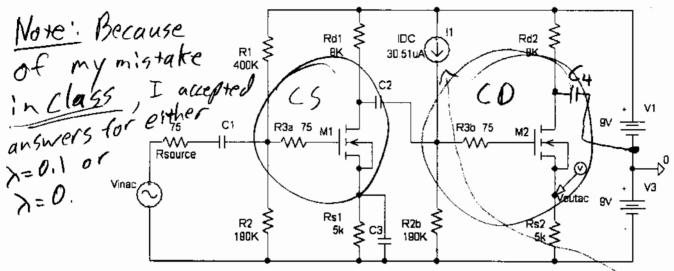
7.) (3-points) (True False: The body of a PMOS Enhancement mode transistor should be tied to

8.) (3-points) The region beneath the channel of a PMOS transistor biased into saturation is extremely high-resistivity due to this region being desired.



Pulling all the concepts together for a useful purpose:

10 \$\text{30-points}\$) Given the following circuit, (a) Identify the configuration of **BOTH** of the two stages (common _____). (b) What is the AC voltage gain, V_{outac}/V_{inac}? You may assume all capacitors have infinite capacitance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain currents), 9 points for the conversion to the small signal model and 18 points for small signal analysis. Hint: Noting similarities in the DC solution will greatly speed up your solution. SHOW ALL WORK TO GET CREDIT!!!!!



Use the following parameters (note that V_T and λ vary with transistor type):

For NMOS Depletion Transistors:

$$K_n'=200 \text{ uA/V}^2$$
 $V_T=-4.0V$ $\lambda=0.0 \text{ V}^{-1}$ Length (L)= 0.18 um Width (W)=10 um

For NMOS Enhancement Transistors:

$$K_0'=100 \text{ uA/V}^2 \text{ V}_T = +0.5 \text{V} \quad \lambda = 0.1 \text{ V}^{-1} \text{ Length (L)} = 0.18 \text{ um} \text{ Width (W)} = 5 \text{ um}$$

For PMOS Depletion Transistors:

$$K_p$$
'=400 uA/V² V_T = +3.0V λ =0.0 V⁻¹ Length (L)=0.36 um Width (W)=10 um

For PMOS Enhancement Transistors:

$$K_p$$
'=50 uA/V² V_T = -0.75V λ =0.1 V⁻¹ Length (L)=0.36 um Width (W)=5 um

$$I = \frac{9 - (9)}{400K + 190K} = 30.51 \text{ as } A$$

$$V_{T} = -0.75V \quad \lambda = 0.1 \text{ V}^{-1} \quad \text{Length (L)} = 0.36 \text{ um} \quad \text{Width (W)} = 5 \text{ um}$$

$$S + a_{5}e \quad 1 \quad V_{7L}$$

$$Q = \int_{-1}^{1} \int_{-1}^{1} R_{1} V_{6}, \quad I = \frac{Q - (-9)}{400R + 190R} = 30.51 \text{ uA} \quad A = 30.51 \text{ uA}$$

$$V_{61} = -Q + I R_{2} = -Q + (30.51 \text{ uA}) \cdot 190R$$

$$V_{61} = -3.2 \text{ V}$$

$$S + a_{5}e \quad 2 \quad V_{7L}$$

$$R_{3b} = \frac{1}{2} \int_{-1}^{1} R_{1} V_{6}, \quad I = \frac{1}{2} \int_{-1}^{1} R_{1} V_{6}, \quad I$$

Extra work can be done here, but clearly indicate with problem you are solving.

$$V_{Th} = V_{G} = \frac{1}{V_{G}} = \frac{1}{V_{G}}$$

Ios = 1/Kn W) (165 - VT)2 (1+ 2 Vos)

$$I_{05} = \frac{1}{2}(0.0037) (+5.8 - I_{0.5000} - 0.5)^{2} (1 + 0.1(18 - I_{0}(13,000)))$$

$$= \frac{1}{2}(0.0037) (33.64 - 117,000I_{0} + 25 \times 10\frac{6}{10})(1 + 1.8 - I_{01300})$$

$$= \frac{1}{2}(0.0934 - 325I_{0} + 69.444I_{0}^{2})(2.8 - 1300I_{0})$$

$$= \frac{1}{2}[0.2616 - 910I_{0} + 194.444I_{0}^{2} - 121.47I_{0}^{4} + 422,500I_{0}^{2}...$$

$$-90.277,777I_{0}^{3}]$$

$$0 = \frac{1}{2}[0.2616 - 1031.47I_{0} + 616.944I_{0}^{2} - 90.277,777I_{0}^{3}] - I_{05}$$

$$0 = 0.1308 - 516.74I_{0} + 308.472I_{0}^{2} - 45.138.888.5$$
In

VG5-VT = 0.65 VZ 5.91V = VOS Saturation

$$\lambda = 0.0 \text{ case}$$
 (1+ λV_{PS}) $\rightarrow 2 \text{ in above}$

$$I_0 = 9e - 4 \text{ Aor } 900 \text{ mA}$$

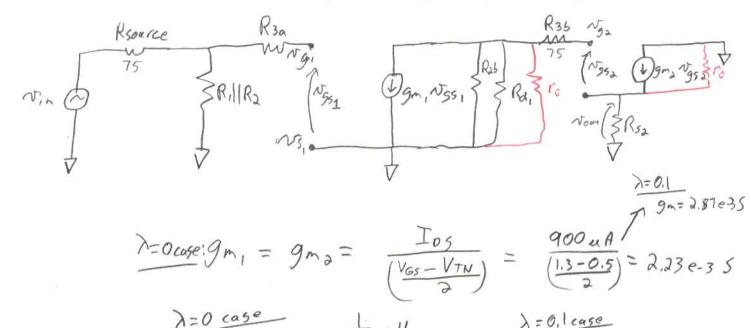
$$V_{OS} = 6.31 \text{ V}$$

$$V_{GS} = 1.3 \text{ V}$$

conversion

Red indicates circuit

Extra work can be done here, but clearly indicate with problem you are solving



$$\lambda = 0 \cos \frac{1}{r_{01}} = r_{02} = \frac{1}{\lambda} + \frac{V_{05}}{I_{05}} = \infty$$

$$\frac{\lambda = 0.1 \cos \frac{1}{2}}{r_{01} = r_{02}} = \frac{10 + 5.91}{930 \text{ MA}} = 17.1 \text{ K}$$

 $0 \frac{N_{954}}{R!R_2 + R_{source}} = \frac{128.8 \text{ H}}{128.8 \text{ H} + 75} \sim 1 \text{ V/V}$

(a)
$$\frac{N_{52}}{N_{551}} = -(g_m, Rd_2||R_2) = -17,11 v/v$$

where Nout = gm2 N552 R52

(4) Nout = gm2 R52 = 11.15 V/L Nga = Ngsa + Nout N52 = Ngs2 + 9m Ngs2 Rs2

$$Av = \frac{N_{out}}{N_{in}} = \frac{N_{gsi}}{N_{in}} \left(\frac{N_{gsi}}{N_{gsi}}\right) \left(\frac{N_{gsi}}{N_{gsi}}\right) \left(\frac{N_{gsi}}{N_{gsi}}\right) \left(\frac{N_{gsi}}{N_{gsi}}\right) \left(\frac{N_{out}}{N_{gsi}}\right).$$

$$= \frac{1}{Av} = -15.7 \text{ V/V}$$

Extra work can be done here, but clearly indicate with problem you are solving.

AC case with $\lambda = 0.1$ use $gr_{(Ra)} = 2.878-35$ In (3) Replace: $Rd_{1}||R_{3b}|| = 15.16 \text{ W/L}$ In (3) + (4) Replace R_{5a} with $R_{5a}||r_{0}$ $\frac{\sqrt{952}}{\sqrt{954}} = \frac{1}{12.07}$ $\frac{\sqrt{953}}{\sqrt{955}} = \frac{1}{12.07}$ $Av = (1)(-15.16)(\frac{1}{12.07})(11.07)$ Av = -13.9 V/V