ECE 3040 Microelectronic Circuits

Exam 3

April 20, 2012

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Print your name clearly and largely:

Solutions

Instructions:
DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your two note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

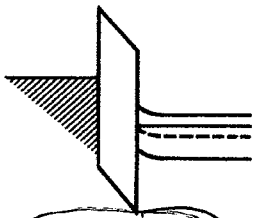
I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

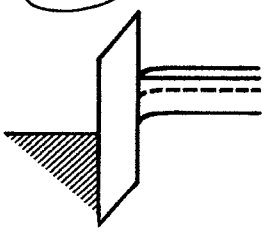
First 24% **Multiple Choice and True/False (Select the most correct answer)**

1.) (6-points total) For each MOS Capacitor, Circle the correct capacitor bias mode and what corresponding MOSFET Bias mode would result

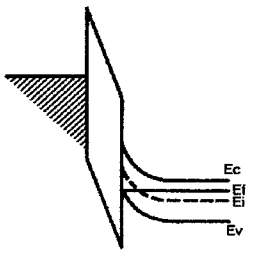
(A) Capacitor: Accumulation, Depletion, Inversion
MOSFET: Cutoff, Linear/triode, Saturation



(B) Capacitor: Accumulation, Depletion, Inversion
MOSFET: Cutoff, Linear/triode, Saturation



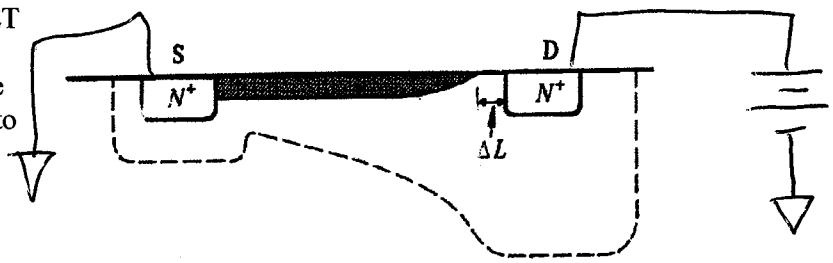
(C) Capacitor: Accumulation, Depletion, Inversion
MOSFET: Cutoff, Linear/triode, Saturation



2.) (3-points) True / False: Feedback can increase the closed loop bandwidth of an opamp.

3.) (3-points) True / False: When a MOSFET channel is "pinched-off" the transistor is biased into cutoff. Linear or Saturation

4.) (3-points) True / False: In the MOSFET transistor to the right, the dashed line represents a depletion region where the drain has a large positive bias relative to the source.



5.) (3-points) True / False: A well designed transresistance amplifier should have a very high input resistance. $\frac{V_{out}}{I_{in}}$

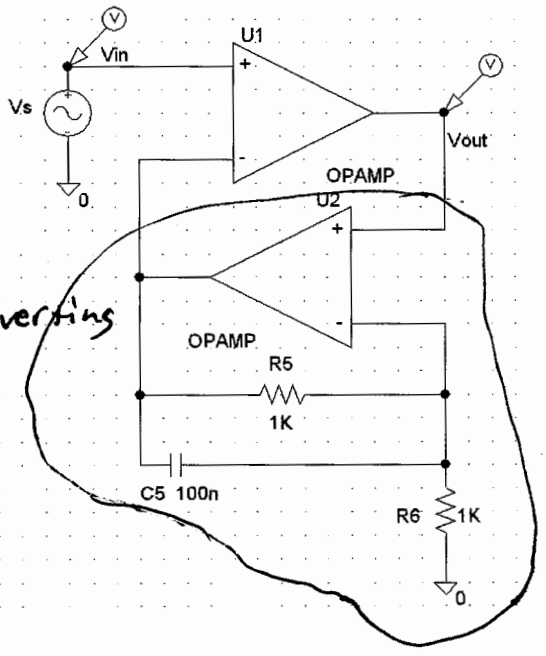
6.) (3-points) True/False: Ideal operational amplifiers have very low input impedance.

7.) (3-points) True/False: MOSFETs are majority carrier devices.

→ Aopen

8.) (26-points) The opamps used in the circuit below can be considered ideal except U1 (and only U1) has an open loop gain of only 50 volts/volt. Determine the closed loop gain and sketch and label the Bode plot showing the voltage gain in all flat regions and the break frequencies (gain in dB vs Log of Frequency).

Let $C = C_5$, $R_5C = 0.0001 = 1e\text{-}4$



Non-Inverting

$$A_{closed\ Loop} = \frac{A_{open}}{1 + \beta A_{open}}$$

$$\beta = 1 + \frac{R_5 \| \frac{1}{Cs}}{R_6}$$

$$= 1 + \frac{\frac{R_5 \frac{1}{Cs}}{R_5 + \frac{1}{Cs}}}{R_6} \left(\frac{Cs}{Cs}\right)$$

$$= 1 + \frac{R_5}{R_6}\left(\frac{1}{1+CR_5s}\right)$$

$$A_{closed\ loop} = \frac{50}{1 + \left[1 + \frac{R_5}{R_6}\left(\frac{1}{1+CR_5s}\right)\right]50}$$

$$= \frac{50(1+R_5Cs)}{(1+R_5Cs) + 50(1+R_5Cs) + 50\left(\frac{R_5}{R_6}\right)} \quad \hookrightarrow (1)$$

$$= \frac{50(1+R_5Cs)}{101 + 51R_5Cs}$$

$$= \frac{50(1+R_5Cs)\left(\frac{1}{101}\right)}{\left[1 + \left(\frac{51}{101}\right)R_5Cs\right]}$$

→ zero @ 1.59 KHz

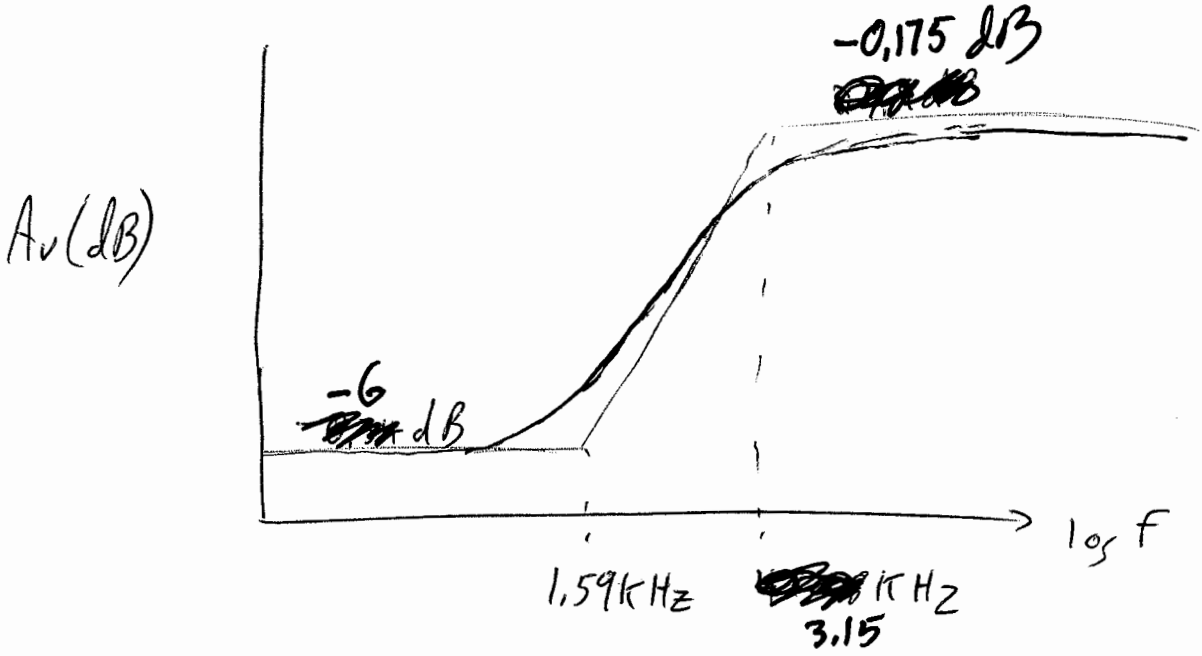
$$= \left(\frac{50}{101}\right)\frac{(1+R_5Cs)}{\left(1 + \frac{51}{101}R_5Cs\right)}$$

→ Pole @ 3.15 KHz

DC: $A = 0.495$ v/v or -6 dB

HF: $A = \frac{50}{51} = 0.98$ v/v or -0.175 dB

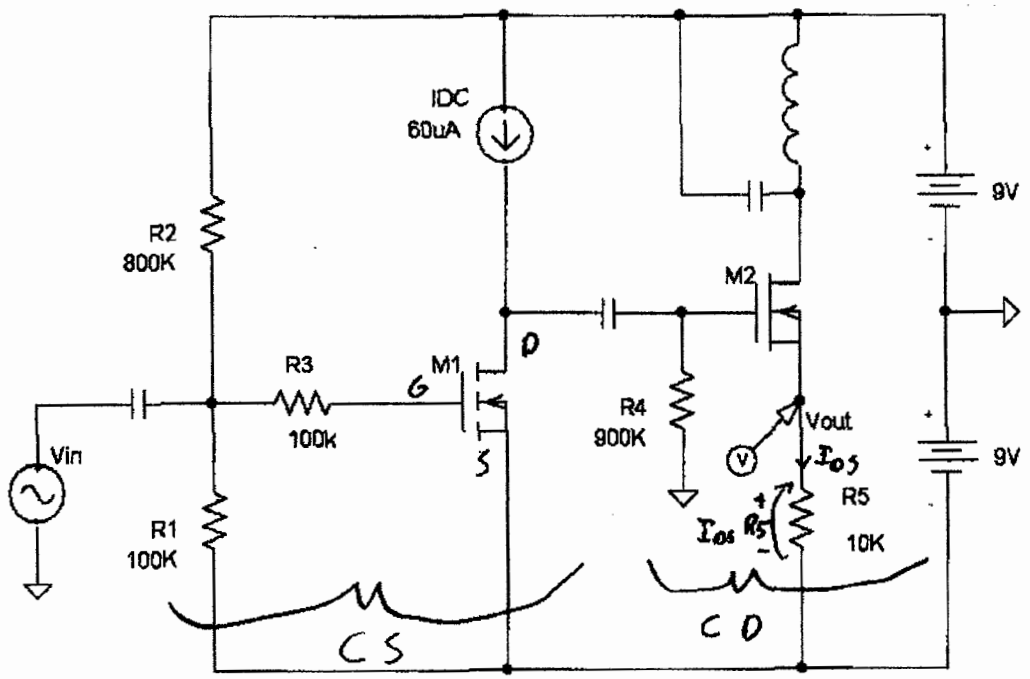
Extra work can be done here, but clearly indicate with problem you are solving.



7:10

Pulling all the concepts together for a useful purpose:

8.) ***(50-points)*** Given the following circuit, (a) Identify the configuration of ***BOTH*** of the two stages (common ____). (b) What is the AC voltage gain, V_{out}/V_{in}? You may assume all capacitors have infinite capacitance. You may assume all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances.
Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain current), 9 points for the conversion to the small signal model and 18 points for small signal analysis.



Use the following parameters (note that V_T and λ vary with transistor type):

M2 For NMOS Depletion Transistors:
K_n'=20 uA/V^2 V_T= -4.0V λ=0.0 V^{-1} Length (L)=10 um Width (W)=10 um

M1 For NMOS Enhancement Transistors:
K_n'=30 uA/V^2 V_T= +0.75V λ=0.1 V^{-1} Length (L)=10 um Width (W)=10 um

For PMOS Depletion Transistors:
K_p'=40 uA/V^2 V_T= +3.0V λ=0.0 V^{-1} Length (L)=10 um Width (W)=10 um

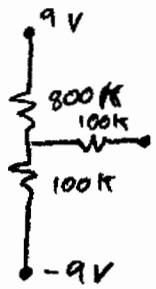
For PMOS Enhancement Transistors:
K_p'=50 uA/V^2 V_T= -1.75V λ=0.1 V^{-1} Length (L)=10 um Width (W)=10 um

Part a) Stage 1 Common Source
Stage 2 Common Drain

Extra work can be done here, but clearly indicate with problem you are solving.

DC:

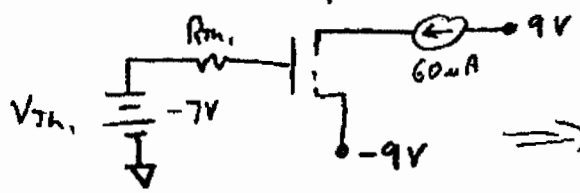
Stage 1:



$V_{Th_1} = 9\left(\frac{100k}{100k+800k}\right) + (-9)\left(\frac{800k}{100k+800k}\right) = 1 - 8$

$V_{Th_1} = -7\,V$

$R_{Th_1} = R_3 + R_1 \| R_2 = 100k + 188.8\,k$



$\Rightarrow \boxed{V_{GS_1} = 2\,V}$

$I_{DS} = 60mA = \left(\frac{10}{10}\right)\frac{1}{2}(30e\text{-}6)(V_{GS} - 0.75)^2(1 + 0.1(V_{DS}))$

$60mA = 15e\text{-}6\,(2 - 0.75)^2(1 + 0.1\,V_{DS})$

$\boxed{V_{DS_1} = 15.6\,V}$

Assumption: $(V_{GS} - V_T) = (2 - 0.75) = 1.25\,V < V_{DS} = 15.6\,V$ ✓

Stage 2:

$V_G = 0V \Rightarrow V_{GS} = -(-9 + I_{DS}R_5) = (9 - I_{DS}R_5)$

$V_D = +9V \quad V_{DS} = 9V - (-9 + I_{DS}R_5)$

D-NMOS

$V_{DS} = 18V - I_{DS}R_5$

$I_{DS} = \left(\frac{10}{10}\right)\frac{1}{2}(20e\text{-}6)(V_{GS} - (-4))^2(1 + 0(V_{DS}))$

$= (10e\text{-}6)(V_{GS}^2 + 8V_{GS} + 16)$

$I_{DS} = 10e\text{-}6\,(81 - 18I_{DS}R_5 + I_{DS}^2R_5^2 + 72 - 8I_{DS}R_5 + 16)$

$I_{DS} = 1.69e\text{-}3 - 2.6\,I_{DS} + I_{DS}^2\,1000$

$0 = 1000\,I_{DS}^2 - 3.6\,I_{DS} + 1.69e\text{-}3$

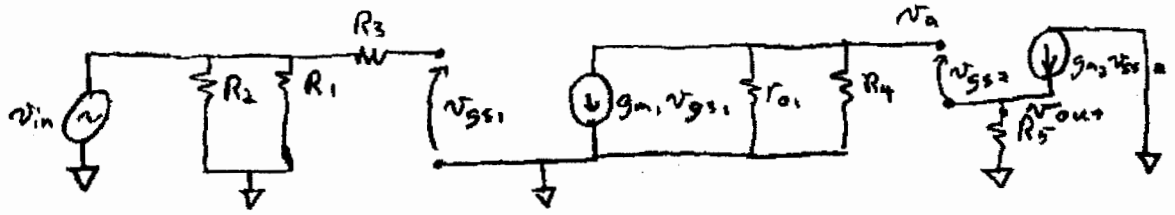
$I_{DS} = \frac{3.6 \pm \sqrt{(3.6)^2 - 4\,1000\,(1.69e\text{-}3)}}{2(1000)}$

$I_{DS} = 555\,mA$ or $3.04\,mA$

Try 555mA: $V_{GS} = 3.45\,V \quad V_{DS} = 12.45\,V$ $\quad V_{GS} - (-4) = 7.45V < V_{DS} = 12.45V$ ✓

Extra work can be done here, but clearly indicate with problem you are solving.

Convert to small signal Model:



$$g_{m1} = \frac{I_{DS1}}{\left(\frac{V_{as}-V_T}{2}\right)} = 9.6e-5\ \Omega^{-1} \qquad g_{m2} = \frac{555\mu A}{\frac{3.45-.4}{2}} = 1.48e-4\ \Omega^{-1}$$

$$(r_{o1})^{-1} = \frac{I_{DS}}{\frac{1}{\lambda} + V_{DS}} = \frac{60e-6}{10+15.6} = \qquad r_{o2} = \infty$$

$$\Downarrow$$

$$r_{o1} = 426.6\,k$$

AC Solution

$$v_{gs1} = v_{in}$$

$$v_a = -(g_{m1}v_{gs1})(r_{o1} \| R_4)$$

$$v_a = g_{m2}v_{gs2}R_5 + v_{gs2} = (1 + g_{m2}R_5)\,v_{gs2}$$

$$v_{out} = +g_m v_{gs2} R_5$$

$$A_v = \left(\frac{v_{gs1}}{v_{in}}\right)\left(\frac{v_a}{v_{gs1}}\right)\left(\frac{v_{gs2}}{v_a}\right)\left(\frac{v_{out}}{v_{gs2}}\right)$$

$$= (1)\left(-g_{m1}(r_o \| R_4)\right)\left(\frac{1}{1+g_{m2}R_5}\right)(g_m R_5)$$

$$= -(9.6e-5)(426.6\,k \| 900k)\left(\frac{1}{1+1.489}\right)(1.489)$$

$$\boxed{A_v = -16.62\ V/V}$$