ECE 3040 Microelectronic Circuits

Exam 3

April 19, 2012

Dr. W. Alan Doolittle

18 minutes

Print your name clearly and largely: Solutions

Instructions:
DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your two note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam: ______________________

I observed an ethical violation during this exam: ______________________

***First 30%* Multiple Choice and True/False (Select the most correct answer)**

1.) (3-points total) True A n-type MOS Capacitor with a large positive gate voltage and the body grounded would be biased into accumulation.

2.) (3-points) True / False: Negative feedback can cause and opamp to oscillate and so is never used in an amplifier.

3.) (3-points) True / False: The MOSFET channel length can vary with the DC bias across V_{DS} and leads a non-flat saturate drain current and to the existence of r_o in the small signal model.

4.) (3-points) True / False: In the PMOSFET the body is n-type is it is an enhancement mode mosfet and p-type if it is a depletion mode mosfet.

5.) (3-points) True / False: If the source resistance is large, a well-designed voltage amplifier should have a very high input resistance.

6.) (3-points) True/False: Negative feedback can decrease the input resistance of an amplifier.

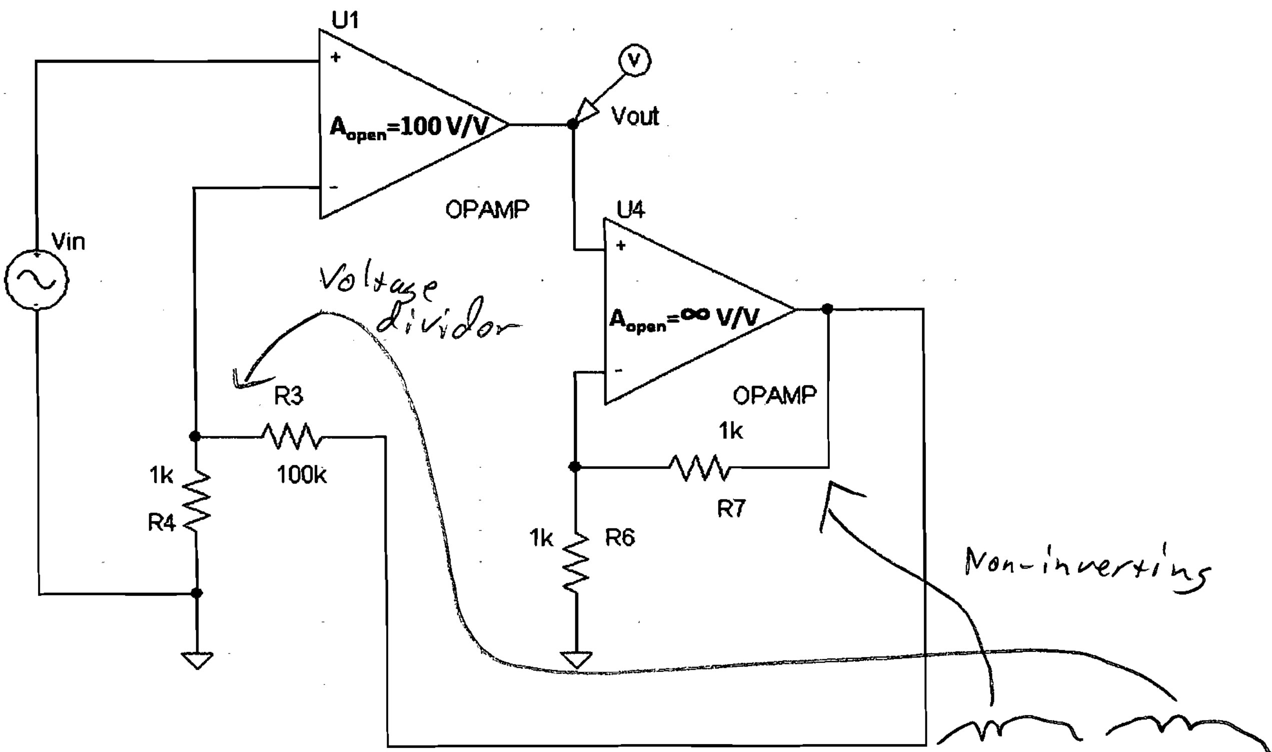
7.) (3-points) True/False: By changing the width from 100 um to 10 um and the length from 10 um to 100 um changes the drain current (everything else the same) by a factor of 100.

8.) (3-points) True/False: NMOS depletion mode transistors have a positive threshold voltage.

9.) (3-points) True/False: Dr. Doolittle is very kind for throwing in a free 3 point question.

10.) (3-points) True/False: The first thing I will buy with my engineering paycheck is a new car.

11.)(20-points) The opamps used in the circuit below can be considered ideal except U1 (and only U1) has an open loop gain of only 100 volts/volt. Determine the closed loop gain.



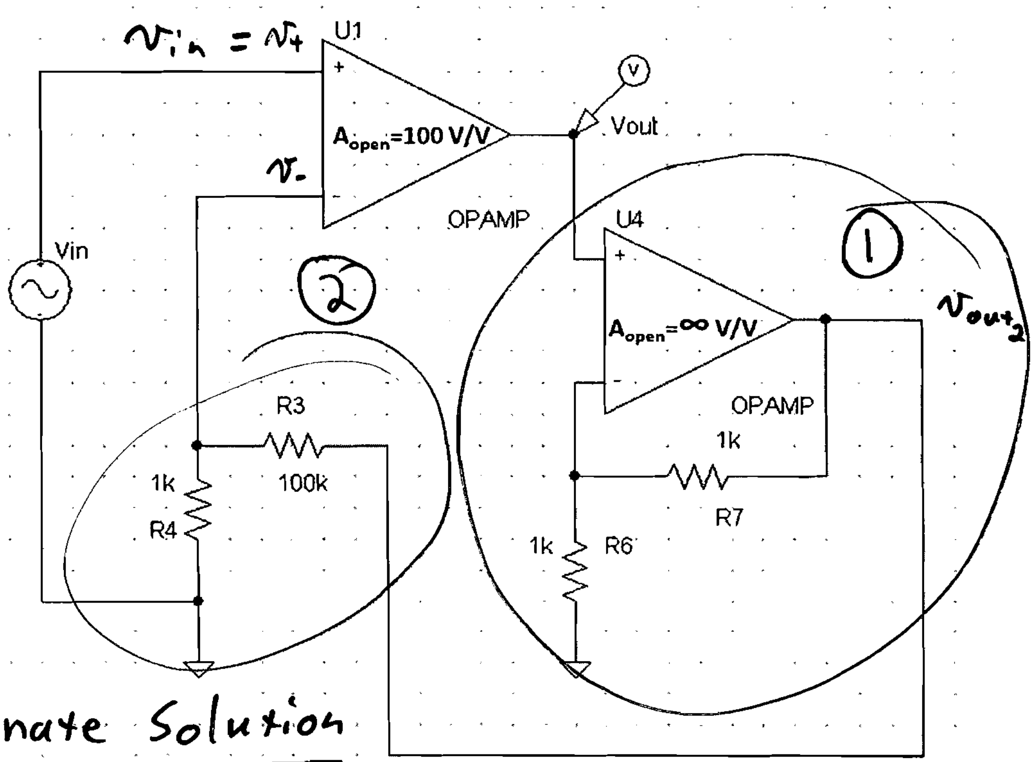
$$A_{closed\,loop} = \frac{A_{open}}{(1+\beta A_{open})}$$

$$\beta = \left(1+\frac{1k}{1k}\right)\left(\frac{1k}{1k+100k}\right) = \frac{2}{101}$$

$$= \frac{100}{1+\left(\frac{2}{101}\right)100} = 33.55\ V/V$$

$$\boxed{A_{closed\,loop} = 33.55\ V/V}$$

11.)(20-points) The opamps used in the circuit below can be considered ideal except U1 (and only U1) has an open loop gain of only 100 volts/volt. Determine the closed loop gain.



Alternate Solution

$$v_{out} = (v_{in} - v_-)100$$

1) $v_{out_2} = v_{out}\left(1 + \frac{R_7}{R_6}\right) = 2\,v_{out}$

2) $v_- = v_{out_2}\left(\frac{R_4}{R_4 + R_3}\right) = v_{out_2}\left(\frac{1}{101}\right)$

3) $v_- = \left(\frac{2}{101}\right)v_{out}$

$$v_{out} = \left(v_{in} - \frac{2}{101}v_{out}\right)100$$

$$v_{out}\left(1 + \frac{200}{101}\right) = 100\,v_{in}$$

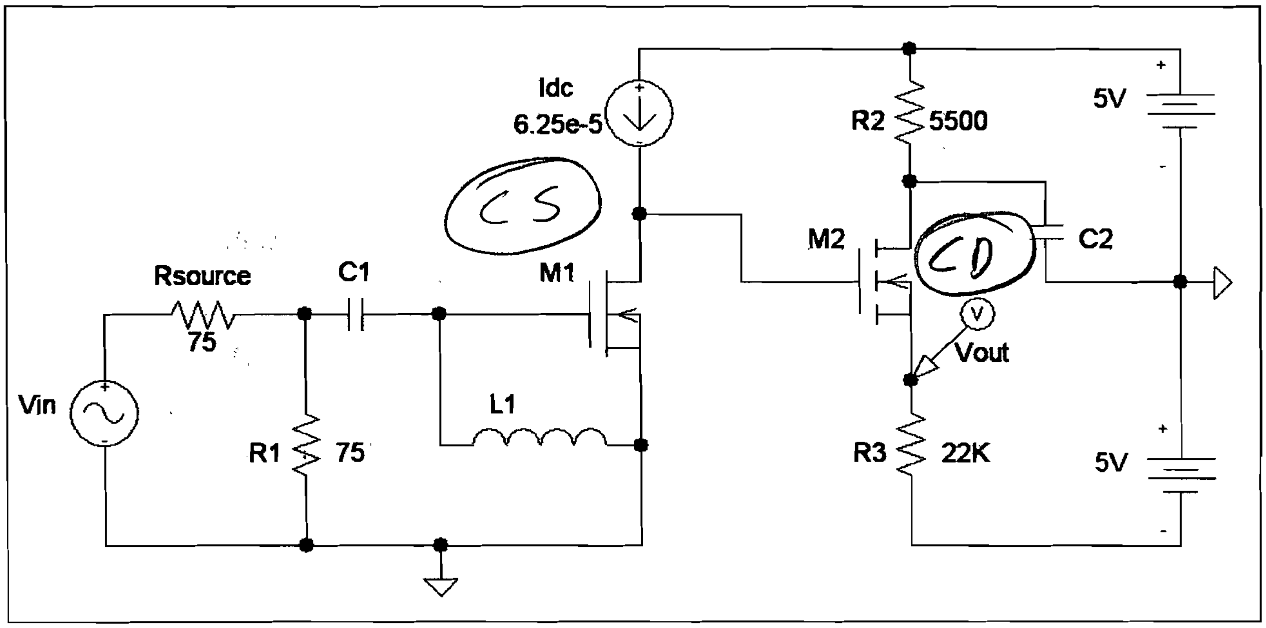
$$\frac{v_{out}}{v_{in}} = \frac{100}{1 + \left(\frac{200}{101}\right)} = \frac{100}{1 + \left(\frac{2}{101}\right)100} = \frac{A_{open}}{1 + \beta A_{ope}}$$

$$\boxed{\frac{v_{out}}{v_{in}} = 33.55\ v/v}$$

Pulling all the concepts together for a useful purpose:

10) (50-points) Given the following amplifier circuit, (a) Identify the configuration of the stage (common ____). (b) What is the AC voltage gain, v_{out}/v_{in}? You may assume all capacitors have infinite capacitance and all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances.

Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain currents), 12 points for the conversion to the small signal model and 15 points for small signal analysis. ***SHOW ALL WORK TO GET CREDIT!!!!!***



Use the following parameters (note that K, V_T and λ vary with transistor type):

M1 For NMOS Depletion Transistors:
K_n'=1 uA/V^2 **V_T= -1.0V** **λ=0.1 V^{-1}** Length (L)=1 um Width (W)=100 um

M2 For NMOS Enhancement Transistors:
K_n'=50 uA/V^2 **V_T= +1.0V** **λ=0.0 V^{-1}** Length (L)=10 um Width (W)=100 um

For PMOS Depletion Transistors:
K_p'=40 uA/V^2 **V_T= +3.0V** **λ=0.0 V^{-1}** Length (L)=10 um Width (W)=10 um

For PMOS Enhancement Transistors:
K_p'=30 uA/V^2 **V_T= -1.75V** **λ=0.1 V^{-1}** Length (L)=10 um Width (W)=10 um

Extra work can be done here, but clearly indicate with problem you are solving.

M1:

$$I_{DS} = (6.25e-5) = \frac{1}{2}(K_n')\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

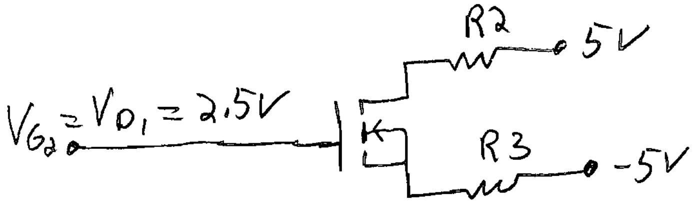
$$= \frac{1}{2}(1e-6)(100)(\underset{\uparrow}{0}-(-1))^2(1+0.1V_{DS})$$

shorted at DC by L1

$$\boxed{\begin{aligned} V_{DS} &= 2.5V \\ V_{GS} &= 0V \\ I_{DS} &= 6.25e-5\,A \end{aligned}}$$

$V_{GS}=0 > V_T=-1$; $V_{DS} = 2.5V > (V_{GS}-V_T) = 0--1$ ✓ saturation confirmed

M2:



$$V_{GS} = V_G - V_S = 2.5-(-5+I_D R_3)$$

$$V_{GS} = 7.5 - I_D R_3$$

$$-5 + I_D R_1 + V_{DS} + I_D R_2 = 5$$

$$V_{DS} = 10 - I_D(R_3+R_2)$$

$$I_D = \frac{1}{2}\left(\frac{W}{L}\right)(K_n')(\underbrace{7.5-I_D R_3}_{V_{GS}} - \underset{V_T}{1})^2(1+0V_{DS})$$

$$I_D \; (-I_D) = 250e-6\,(6.5 - I_D R_3)^2 \; (-\underline{\underline{I_D}})$$

$$0 = 250e-6\,(42.25 - 13R_3 I_D + I_D^2 R_3^2) - \underline{\underline{I_D}}$$

$$0 = 0.0105625 - 72.5 I_D + 121{,}000 I_D^2$$

$I_D =$	~~349 uA~~	250 uA
V_{GS}	~~-0.818V~~	2 V
V_{DS}		3.125V
$V_{GS}-V_T$		1 V

transistor not turned on!

$V_{GS} > V_T$ ✓

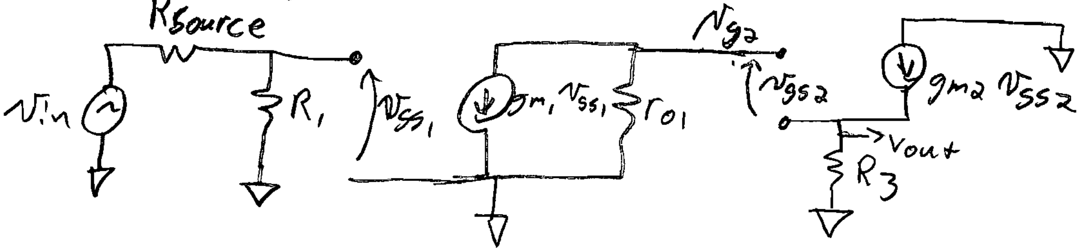
$V_{DS} = 3.125 > V_{GS}-V_T = 1V$ ✓

Assumption verified

Extra work can be done here, but clearly indicate with problem you are solving.

$$g_{m_1} = \frac{I_D}{\frac{V_{GS} - V_T}{2}} = 125\,\mu A/V \qquad g_{m_2} = 500\,\mu A/V$$

$$r_{o_1} = \frac{I_{DS}}{\frac{1}{\lambda} + V_{DS}} = 200{,}000\,\Omega \qquad r_{o_2} = \infty$$



1) $v_{gs1} = v_{in} \dfrac{R_1}{R_1 + R_{source}} = 0.5\, v_{in} \Rightarrow \overset{①}{\dfrac{v_{gs1}}{v_{in}}} = 0.5 \ \text{v/v}$

2) $v_{g2} = -g_{m_1} v_{gs1} r_{o1}$

3) $v_{g2} = v_{gs2} + g_{m_2} v_{gs2} R_3$

4) $v_{out} = g_{m_2} v_{gs2} R_3 \Rightarrow \overset{③}{\dfrac{v_{out}}{v_{gs2}}} = g_{m_2} R_3 = 11 \ \text{v/v}$

$$\rightarrow \quad v_{gs1}(-g_{m_1} r_{o1}) = v_{gs2}(1 + g_{m_2} R_3)$$

$$\overset{②}{\frac{v_{gs2}}{v_{gs1}}} = \left(\frac{-g_{m_1} r_{o1}}{1 + g_{m_2} R_3}\right) = \left(\frac{-(125\,\mu A/V)\, 2E5}{1 + 500\,\mu A/V\,(22k)}\right) = -2.08\bar{3} \ \text{v/v}$$

$$A_v = \overset{①}{\left(\frac{v_{gs1}}{v_{in}}\right)} \overset{②}{\left(\frac{v_{gs2}}{v_{gs1}}\right)} \overset{③}{\left(\frac{v_{out}}{v_{gs2}}\right)} = \overset{①}{(0.5)} \overset{②}{(-2.08\bar{3})} \overset{③}{(11)}$$

$$\boxed{A_v = -11.458 \ \text{v/v}}$$