Static Random Access Memory (SRAM)

ECE 3080

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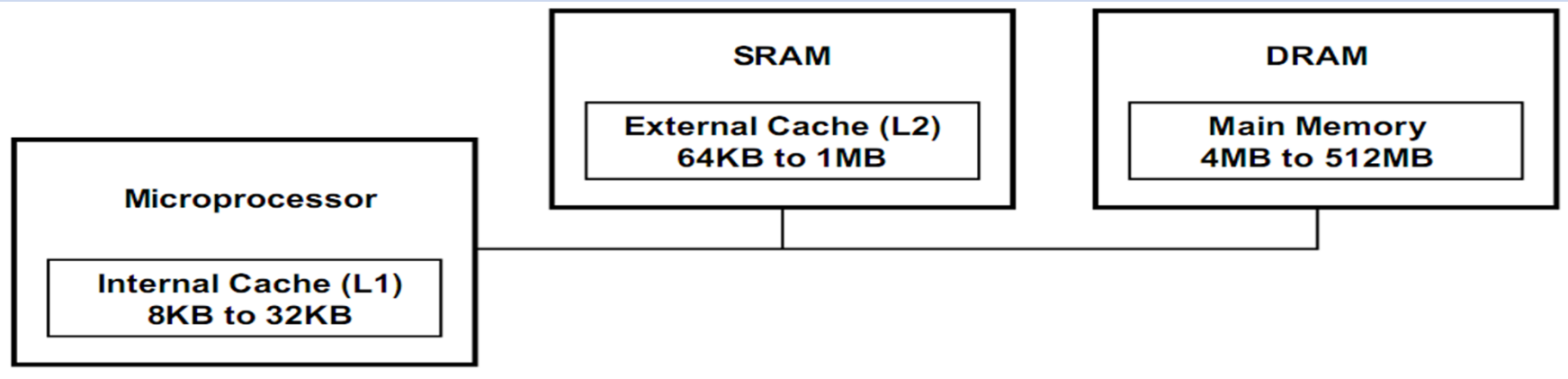
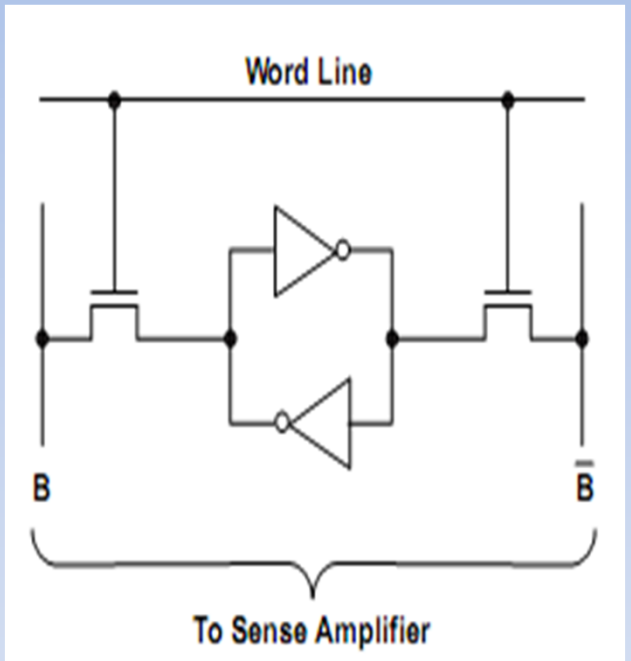
Introduction

- Creates an interface with the CPU at speeds not attainable by DRAMs.
- Replaces DRAM in systems that requires low power consumption.
- Serves as cache memory interfacing between DRAMs and the CPU.



Introduction

- SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two transistors.
- SRAM cell's data is volatile.
- SRAM doesn't have a refresh periodically like DRAM since It uses a bi-stable flip-flop

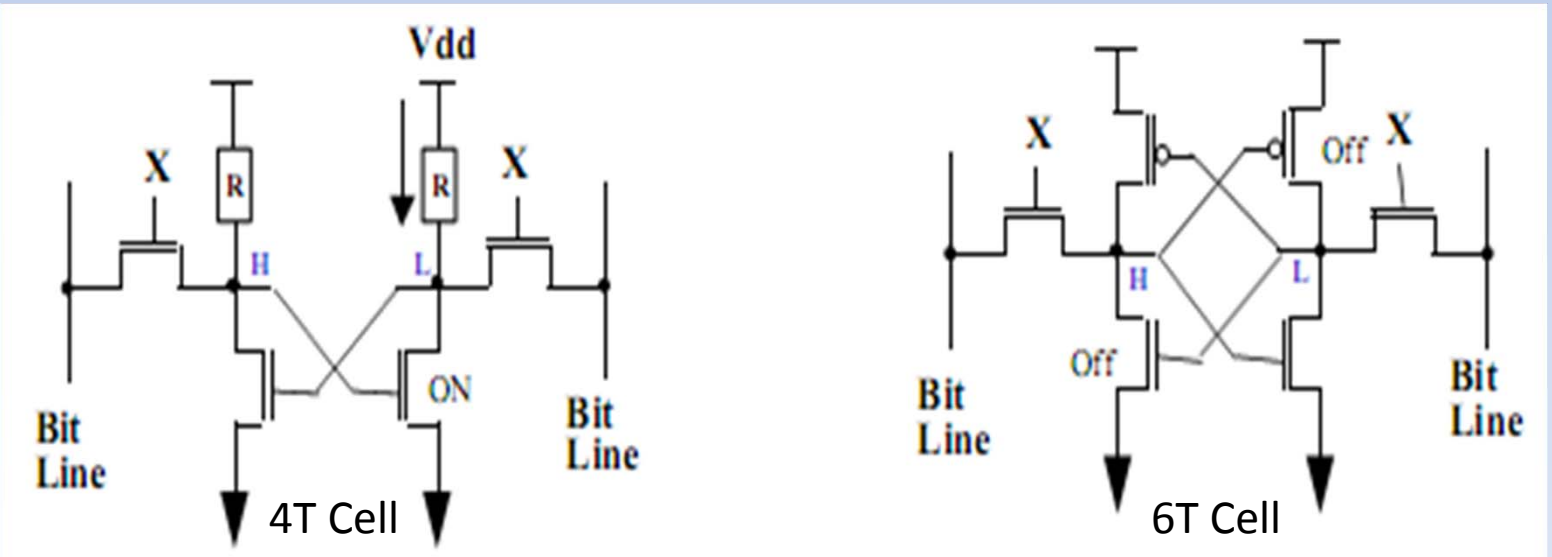


SRAM Cell Operation

- Stand-By Mode
- Data Retention Mode
- Write/Read Mode

Stand-By

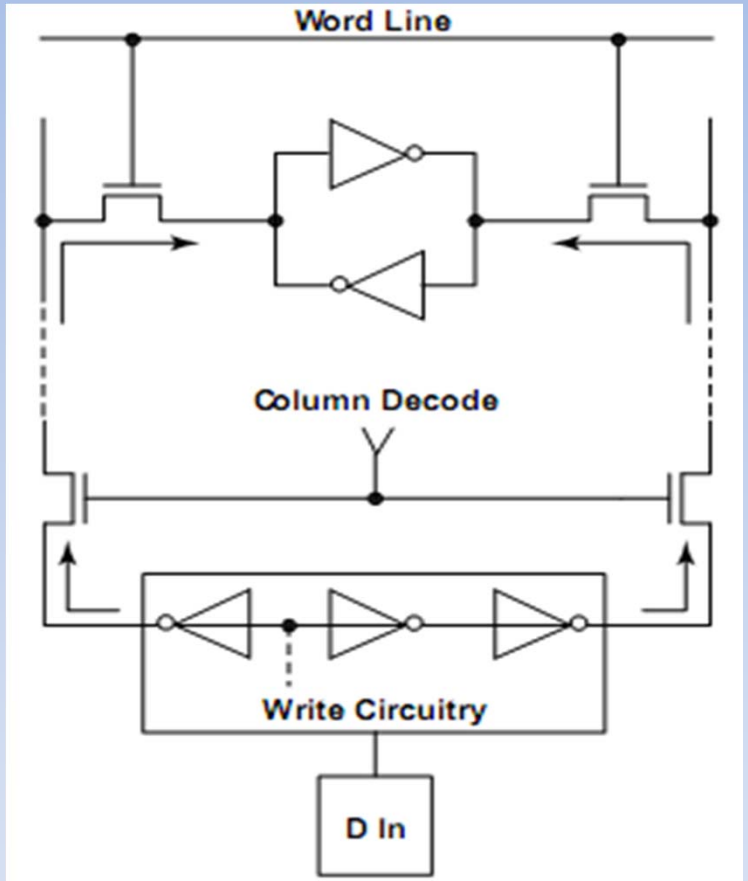
- One inverter is always ON for the 4T cell
- One transistor in each of the coupled inverters is OFF for the 6T cell



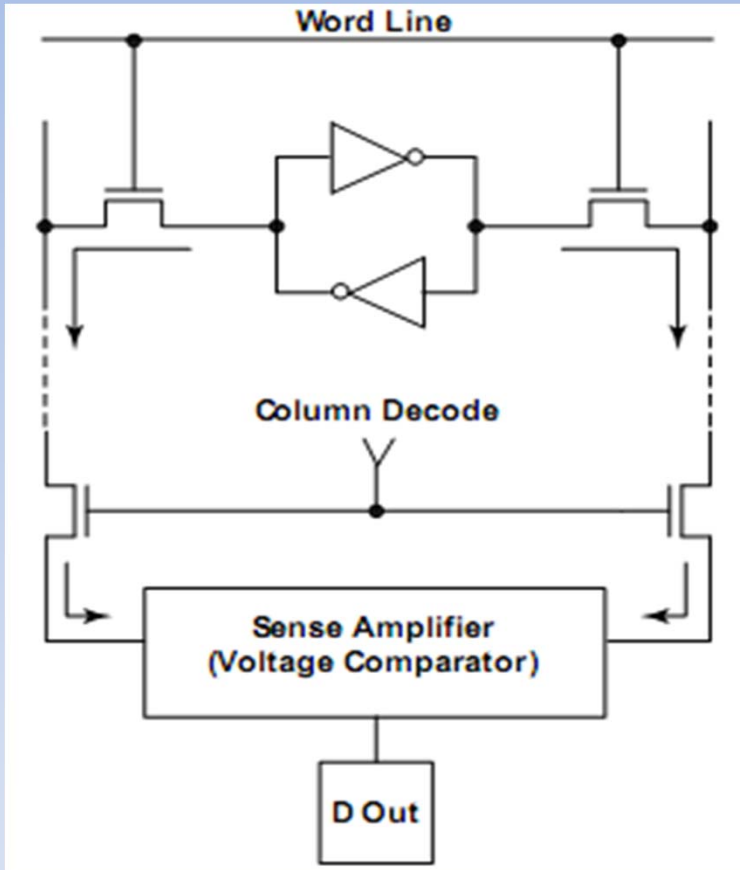
Data Retention

- The SRAM must be supplied by a power supply that will not fluctuate beyond certain level
- At lower voltage, the SRAM is set to retention mode where the part is no longer accessible, but the cell will keep the data.

Write/Read



Write Operation



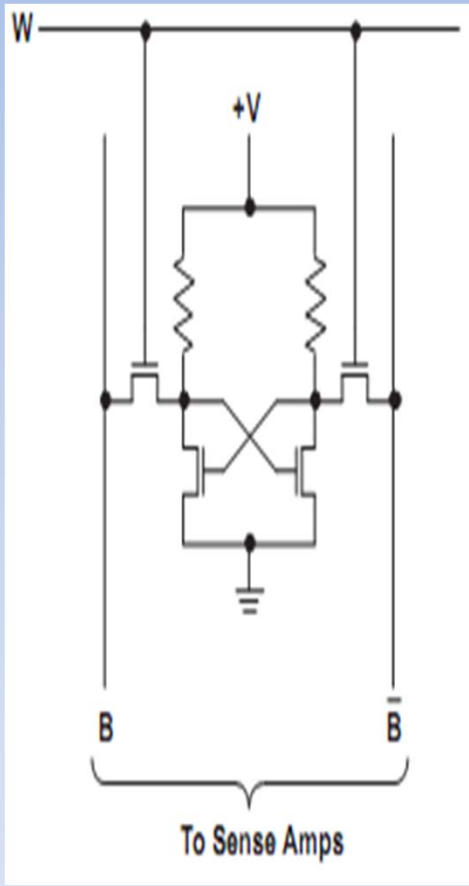
Read Operation

SRAM Types

- Different types of SRAM are based on the type of load used in the elementary inverter of the flip-flop cell.
- PMOS Enhancement Load Cell, NMOS Enhancement Load Cell, NMOS Depletion Load Cell, High-Resistivity Poly Load Cell (4T Cell), TFT (Thin Film Transistor) Load Cell, and Full CMOS Cell (6T Cell)

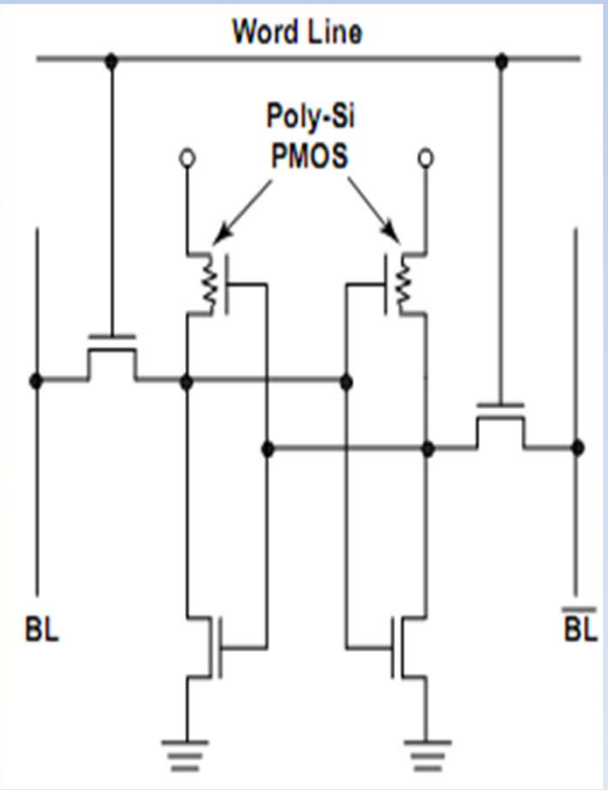
High-Resistivity Poly Load Cell (4T Cell)

- It Consists of four NMOS transistors (two pass-transistors and two pull-downs of the flip-flop inverters) and two poly-load resistors (very high polysilicon resistor).
- Pros:
  - 4T Cell is cost effective chip size compare to 6T Cell
- Cons:
  - In high density, it has high stand-by current
  - It is sensitive to noise and soft error rate (SER) due to high resistance
  - It is not as fast as 6T Cell



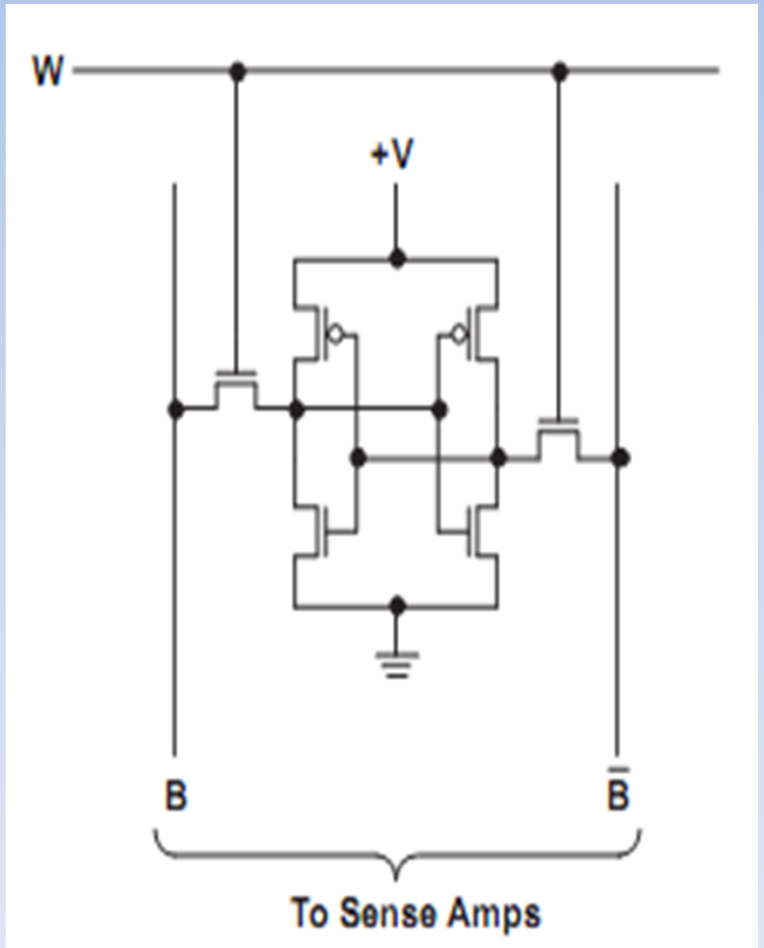
TFT (Thin Film Transistor) Cell

- TFT is formed through configuring a PMOS by depositing several layers of polysilicon above the silicon surface.
- The source/channel/drain is formed in this polysilicon load.
- Pros:
  - Compatible cell size as compared with 4T Cell
  - Improved SER
- Cons:
  - Complicated process
  - Poor TFT electrical characteristics



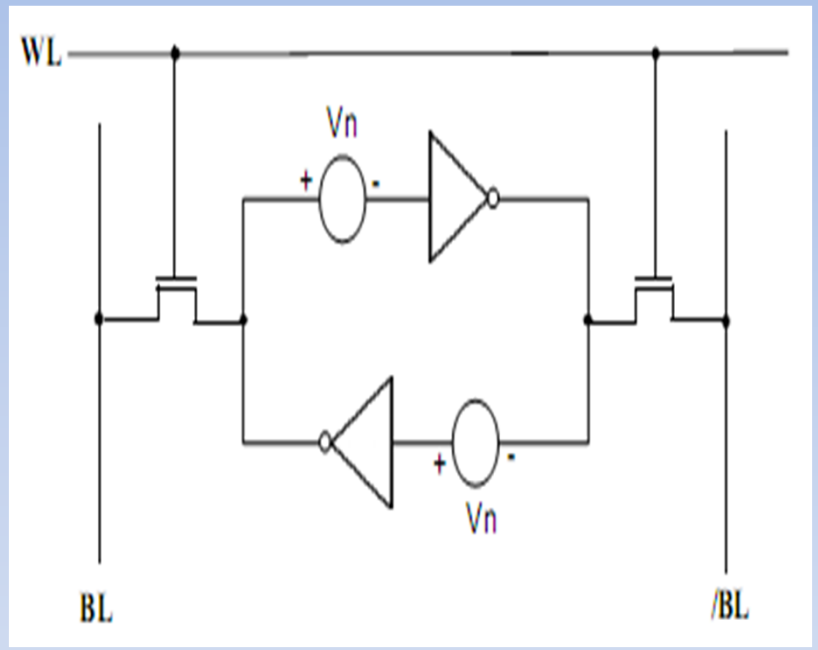
Full CMOS Cell (6T Cell)

- It consists of four NMOS transistors and two PMOS transistors.
- Pros:
  - Very low stand-by power dissipation
  - Noise immunity
  - Good SER characteristics
  - High speed
- Cons:
  - Large cell size



SRAM Cell Stability

- Static-Noise Source (Vn):
  - DC Disturbance
    - Layout pattern offset
    - Process mismatches
  - Dynamic Disturbance
    - Alpha Particles
    - Crosstalk
    - Thermal noise
    - Voltage supply ripple



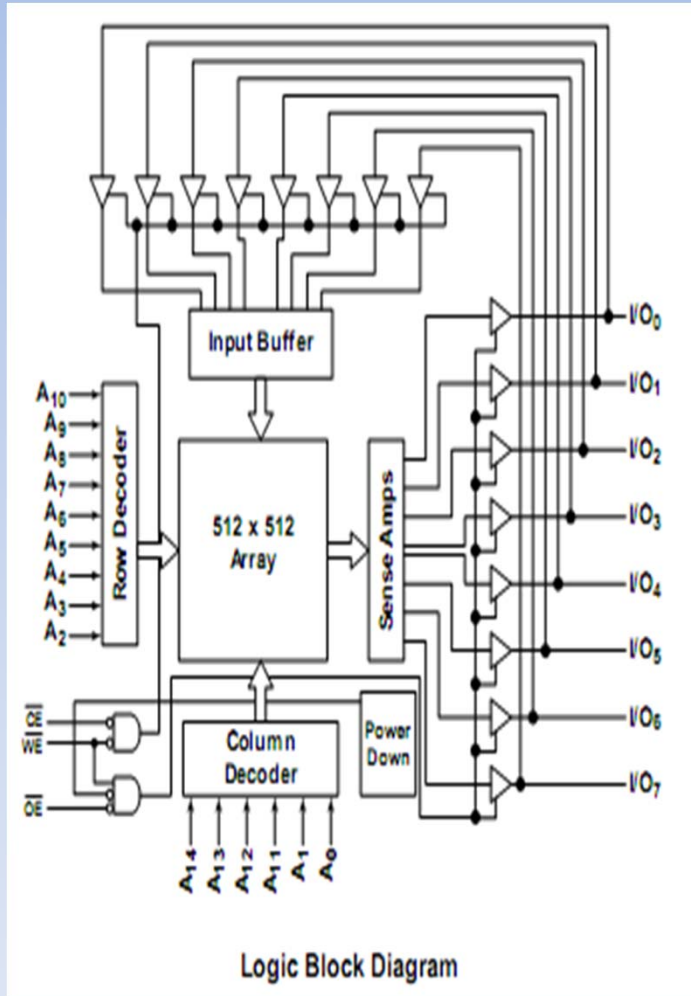
- Static-Noise Margin (SNM): Maximum value of the static noise source.

SRAM Configuration

- Asynchronous SRAMs
- Synchronous SRAMs
- Special SRAMs
- Non-Volatile SRAMs

Asynchronous SRAMs

- The memory is controlled by three signals:
  - Chip Select (CS) or Chip Enable (CE): Selects or de-selects the chip
  - Output Enable (OE): Controls the output
  - Write Enable (WE): Selects read or write cycles



Logic Block Diagram

Synchronous SRAMs (SSRAM)

- Read or write cycles are synchronized with the microprocessor clock and can be used in very high-speed applications.
- SSRAM can be achieved through Burst Mode, flow-through SRAM, Pipelined SRAMs, Late-Write SRAM, ZBT (Zero Bus Turn-around), and DDR (Double Data Rate) SRAMs.

Special SRAMs

- Cache Tag RAMs
  - It uses special memory chip called cache tag RAMs to keep track of which data is in both the SRAM cache memory and the main memory (DRAM).
- FIFO SRAMs
  - A FIFO (first in, first out) memory is a specialized memory used for temporary storage, which aids in the timing of non-synchronized events.

Non-Volatile SRAMs

- Shadow RAMs
  - It integrates SRAM and EEPROM (Electrically Erasable Programmable Read-Only Memory).
  - It preserves the data when a power failure occurs by moving the data from the SRAM to the EEPROM.
- Battery-Backed SRAMs (BRAMs)
  - SRAM with a small lithium battery
  - While the power consumption is very low, SRAMs will be in sleep mode.

Questions?