

Memristors

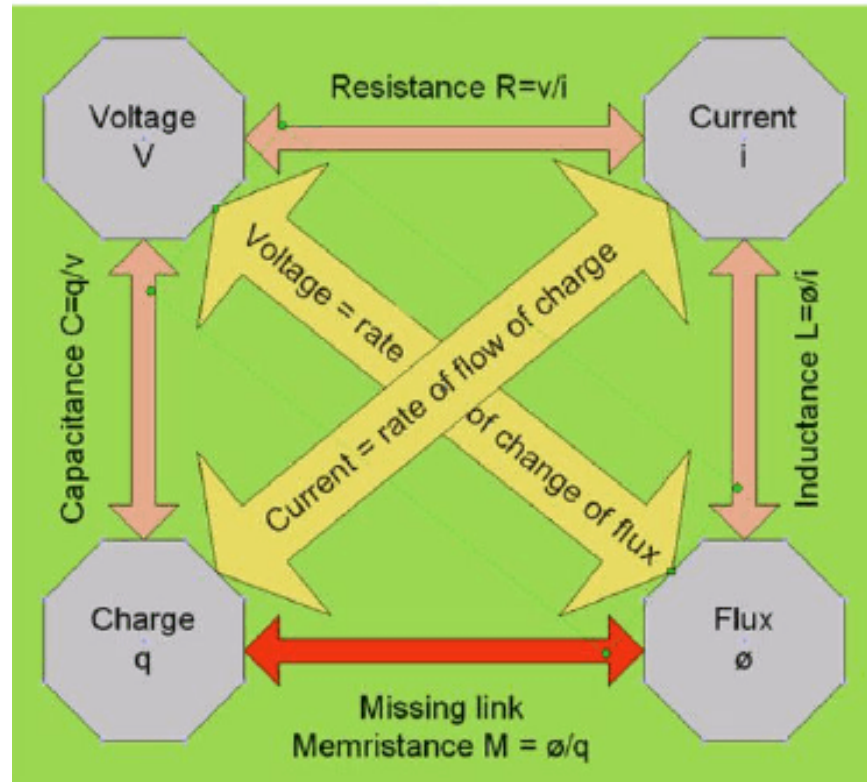
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ECE 3080

The Basics

- “Missing” passive circuit element that relates charge and voltage and keeps a previous resistance in the absence of current
- Unites the other passive circuit elements in relation to each other
 - Resistor: Voltage and Current
 - Capacitor: Charge and Voltage
 - Inductor: Flux-Linkage and Current
 - **Memristor: Flux-Linkage and Charge**

Basics



History

- In 1960 Widrow wrote a paper on 3 terminal “memistors” called “An Adaptive ADALINE Neuron using chemical memistors” in which he describes 3 terminal devices similar to memristors
- In 1968 Argall wrote a paper title "Switching phenomena in titanium oxide thin films," which talks about the resistance switching of Titanium Dioxide
- In 1971 Leon Chua independently predicted and described the memristor's function in his paper “Memristor-the Missing Circuit Element”
- Several Variable resistance devices were developed but none made a connection to the original theory including Samsung who filed a patent on oxygen vacancies in TiO_2
- In 2008 Several members of HP Labs published a paper that outlined the memristor behavior in nanoscale systems using Titanium Dioxide

<http://tinytechip.blogspot.com/2011/04/hps-memristor-is-greatest-hoax-in.html>

Theory

- Memristance (M) is a varying resistance as a function of flux (ϕ) and charge (q)

$$M(q) = d\phi(q)/dq$$

- The voltage across a memristor is defined as

$$v(t) = M(q(t))i(t)$$

- Memconductance (W) follows similarly

$$W(f) = dq(\phi)/d\phi$$

- The current across a memristor is described by

$$I(t) = W(\phi(t)) v(t)$$

Reality of the Theory

- Controversy over the 4th circuit component
 - memristors are actually a non-linear version of the same system as the resistor
- This leads to idea of memcapacitors and meminductors as being other non-linear circuit elements

Non-Linear Resistor

- General description for a resistor over time

$$V = R(w) * I(t)$$

- In a resistor

$$\frac{dw}{dt} = 0$$

- In memristor (2nd Order)

$$\frac{dw}{dt} = \frac{dq}{dt} = I$$

- There may be higher order allowing for an infinite number of circuit elements to be built

1. The Mythology of the Memristor – Blaise Mouttet of George Mason University
2. Canonical Realization of Chua's Circuit Family – Leon Chua
<http://www.ee.berkeley.edu/~chua/papers/Chua90.pdf>

Why it works

- The change in resistance is due to a change of the material and the resistance will remain constant until voltage or current are altered
- In most memristors used today current direction is used to control the amount of resistance.
 - Negative and positive voltages can open and close the memristors like switches.
 - The resistance is related to the integral of charge

Metal Oxide Memristor

- The memristor developed by HP uses thin film layers of Titanium Dioxide on a nano scale
 - One layer is depleted of oxygen
 - The depleted layer has a much lower resistance
- As current moves through the layers it causes the oxygen to drift changing the thickness of the doped layer which alters the resistance of the material as a whole

- The Titanium Oxide forms two layers
 - TiO_2
 - TiO_x where $x < 2$
- The applied voltage changes the width of the depleted layer changing its value within a specified range determined when making the system
- Layers stay constant indefinitely after the device is “off”
 - Measured to be upwards of 10^6 seconds

Strukov, D. , Snider, G. , Williams, R. , & Stewart, D. (2008). “The Missing Memristor Found” . *Nature*, 453(7191)

Titanium Oxide Memristor

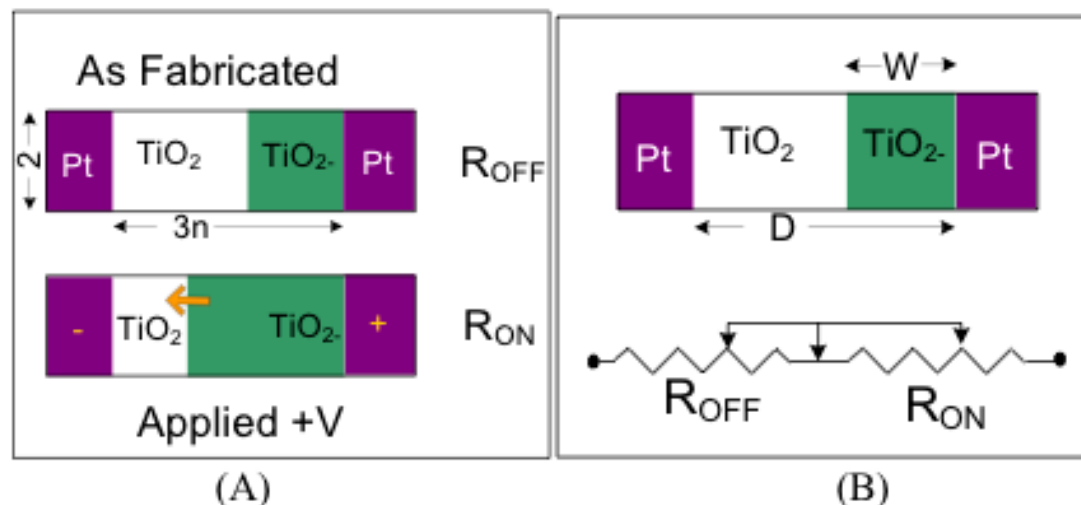


Fig. 3 (A) Memristor size 50 nm showing both possible states; The low resistance case R_{ON} and high resistance case R_{OFF} (B) Its circuit model as a variable resistance[11]

Titanium Oxide Memristor

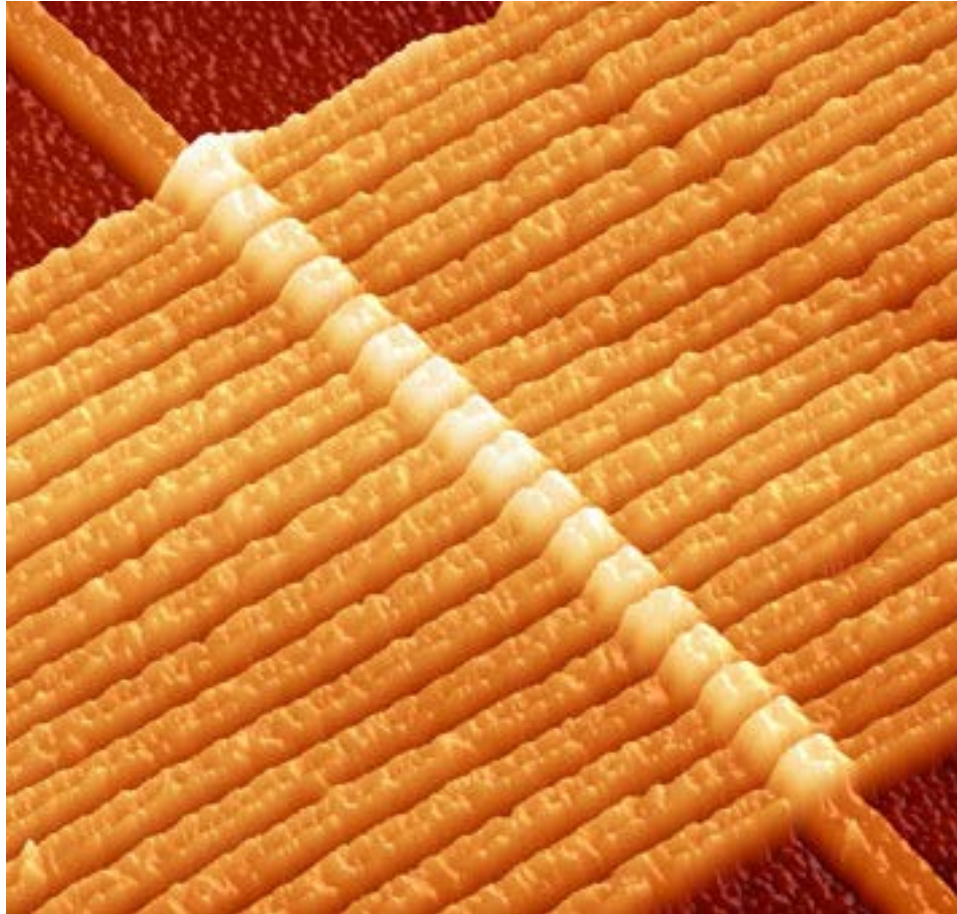
- From the model provided a voltage relationship is obtained

$$v(t) = (R_{on} \frac{w(t)}{D} + R_{off} (1 - \frac{w(t)}{D})) i(t)$$

- $\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t)$
- Solving for $w(t)$ and combining the equations gives

$$M(q) = R_{off} (1 - q(t) \left[\mu_v \frac{R_{on}}{D^2} \right])$$

HP's Memristor



<http://spectrum.ieee.org/semiconductors/design/the-mysterious-memristor>

Problems with HP's Memristor

- Limited by the doping of the material in the amount of resistance it can create
- Does not behave ideally
 - Device has capacitance due to the electrodes
 - Schottky barriers and charge trapping alters the $V=MI$ relationship
 - Ionic mobility and tunneling alter the effect of charge on the resistance
 - Oxygen has a slow drift limiting it to lower frequency applications and is sometimes difficult to control
- Reliability and longevity of the device

Other types of Memristors

- Spintronic Memristors
 - Makes use of spin of electron to change the magnetism of the material
 - The magnetism of the material then alters the resistance of the material

Other types of Memristors

- Spin Memristive Systems
 - Makes use of a ferromagnetic junction
 - Junction only allows electrons of certain spin to pass through the barrier other electrons are left behind
 - Electrons with nonselected spin build up at the barrier and cause a higher resistance as they let less current through.

Spin Memristive Systems

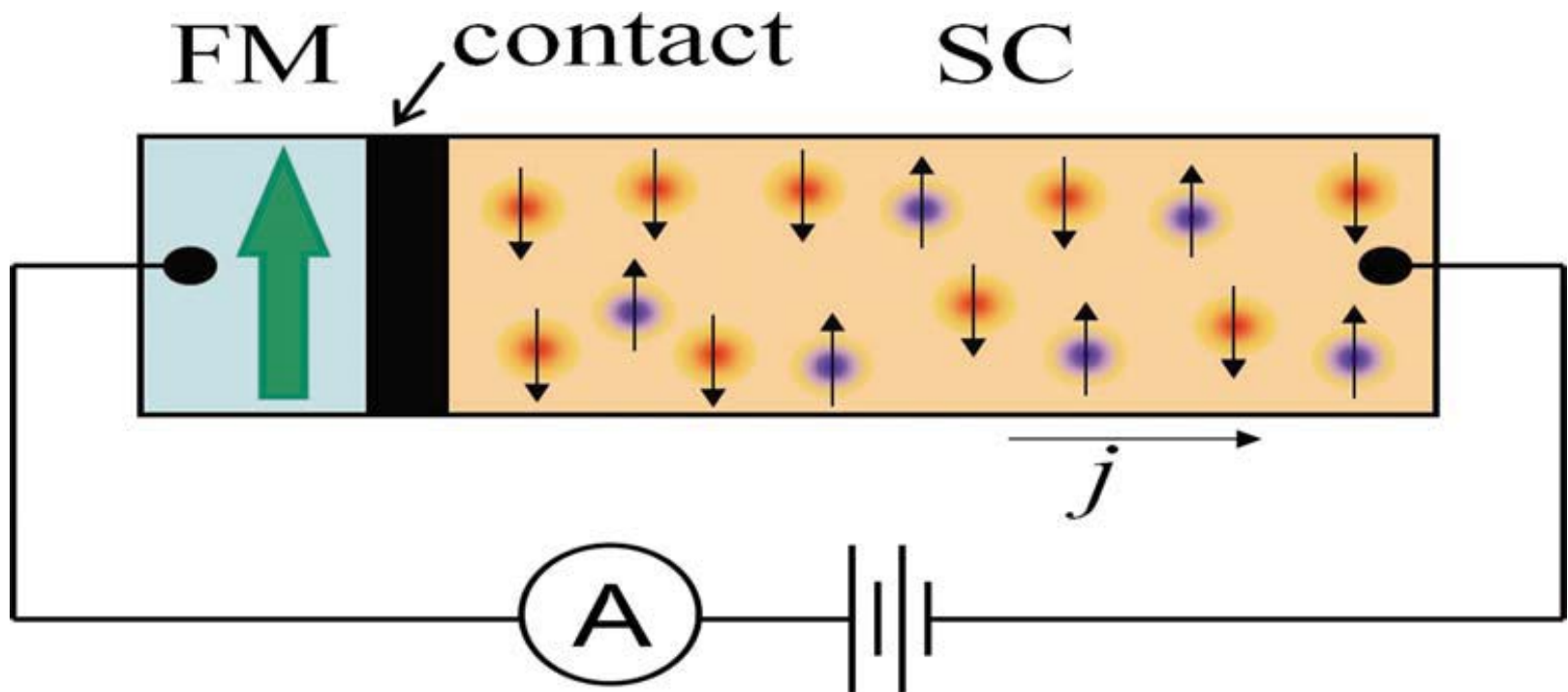


Image taken from PHYSICAL REVIEW B **78**, 113309 2008 **Spin memristive systems: Spin memory effects in semiconductor spintronics**

Logic Design with Memristors

- One of the more immediate uses of memristors is digital logic
- Functions as a switch that will not lose its position when the device is turned off

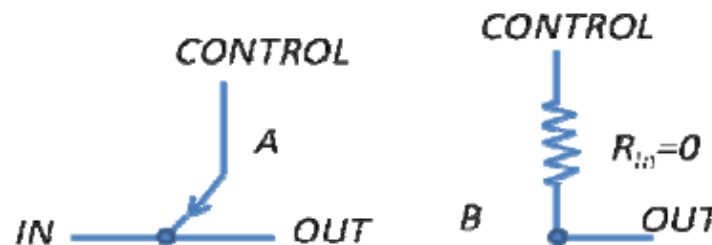


Fig. 4: Memristor as a logical state element. A) A closed memristor showing logic "0" and B) Equivalent circuit during readout.

Logic Design with Memristors

- A combination of these memristor logic switches can be used to make more complex logic

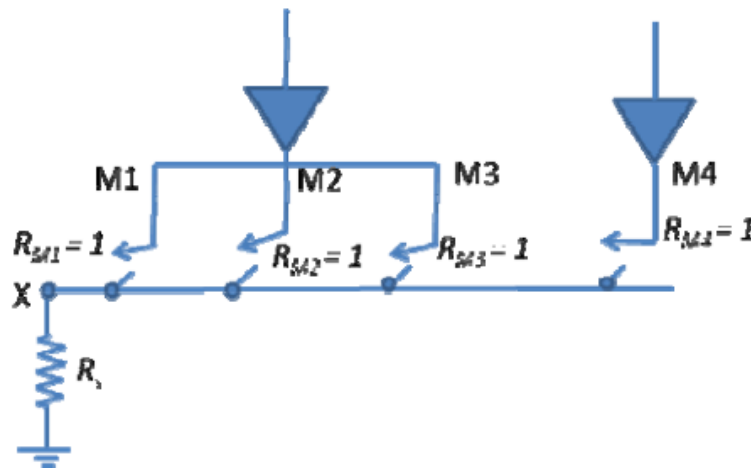


Figure 7: Wired-AND logic implementation. The memristors M1-M3 are connected in the Inverting configuration as shown. The output will be stored in RM4 which will be $(RM1.RM2.RM3)'$.

-The combination of these switches create a memristor wired and gate $M4 = (M1 M2 M3)'$

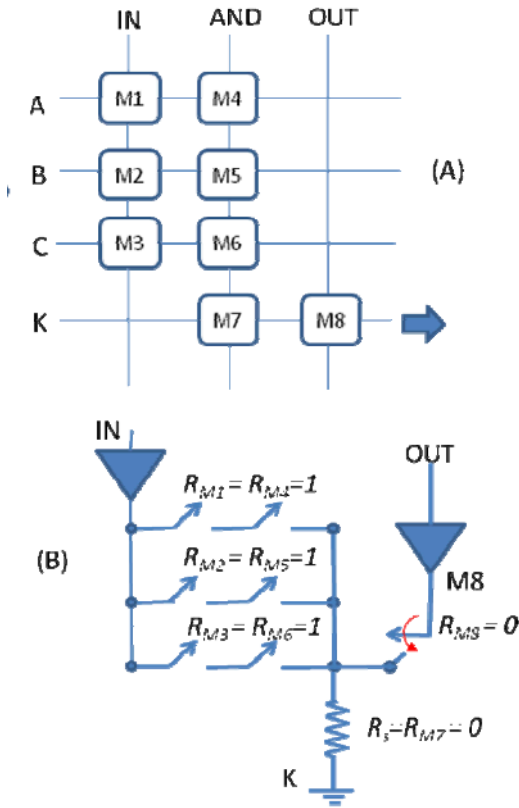
-This is implemented by the relative voltages at the input controls and the previous state of the memristor

Image from "Digital Logic Implementation in Memristor-Based Crossbars - A Tutorial," delta, pp.303-309, 2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications, 2010

Memristor Crossbar Array

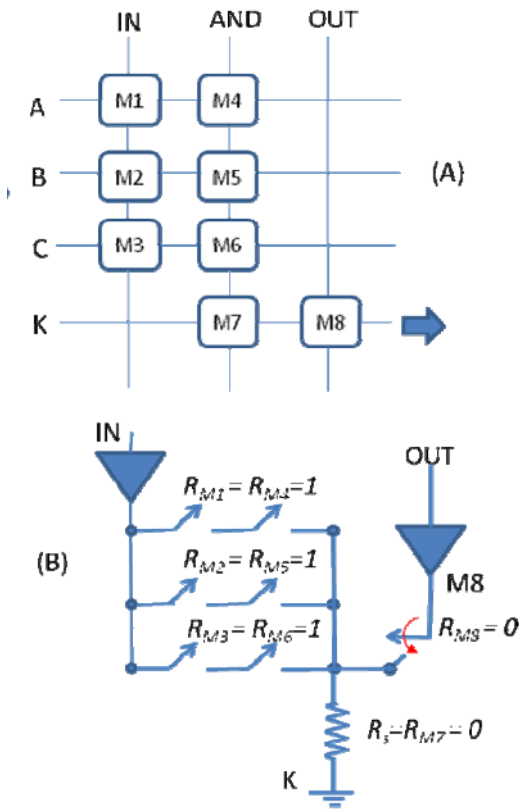
- By arranging the memristors in a crossbar array logic gates can be created.
 - Uses same technique currently used but replaces diodes and transistors with memristors
- A crossbar array consists of a grid of wires with memristors at the junctions. This controls the flow of current when certain voltages are provided creating logic.
- Crossbar arrays may be used for memory

Example NAND with Memristor



- Using several stages the logic can be use
 1. Latch Input – Put A ,B, C into M1 M2 M3
 2. Copy Input – apply voltage to AND and 0 voltage at IN. Also close M7 by applying no voltage at K

Example NAND with Memristor



3. Evaluate Logic Apply voltage at IN and OUT terminals to create equivalent circuit B with resembles the wired AND circuit.
4. Open AND– Apply large negative voltage to AND and open M4 – M7
5. Read – Apply 0 voltage to OUT and use the output of M8

Further and Future Applications

- Non-volatile memory applications
- Lower power and very small devices
- Neuromorphic circuits that mimic synapse

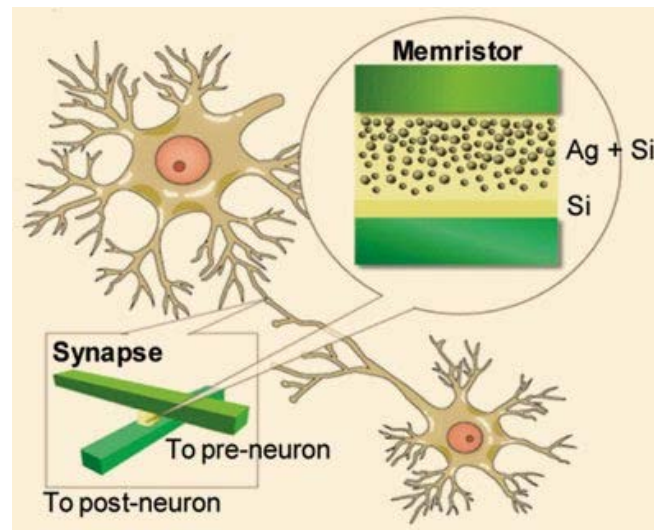


Image from <http://www.eetimes.com/electronics-news/4088605/Memristor-emulates-neural-learning>

Further Reading

- Tezaswi Raja, Samiha Mourad, "Digital Logic Implementation in Memristor-Based Crossbars - A Tutorial," *delta*, pp.303-309, 2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications, 2010
- Yu. V. Pershin and M. Di Ventra, Publisher's Note: Spin memristive systems: Spin memory effects in semiconductor spintronics [*Phys. Rev. B* 78, 113309 (2008)], *Phys. Rev. B* 78, 159905 (2008).
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- Chua, L.O. O. "Memristive devices and systems." *Proceedings of the IEEE* 64.2 (1976): 209-223.
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- http://www.hpl.hp.com/news/2008/apr-jun/memristor_faq.html