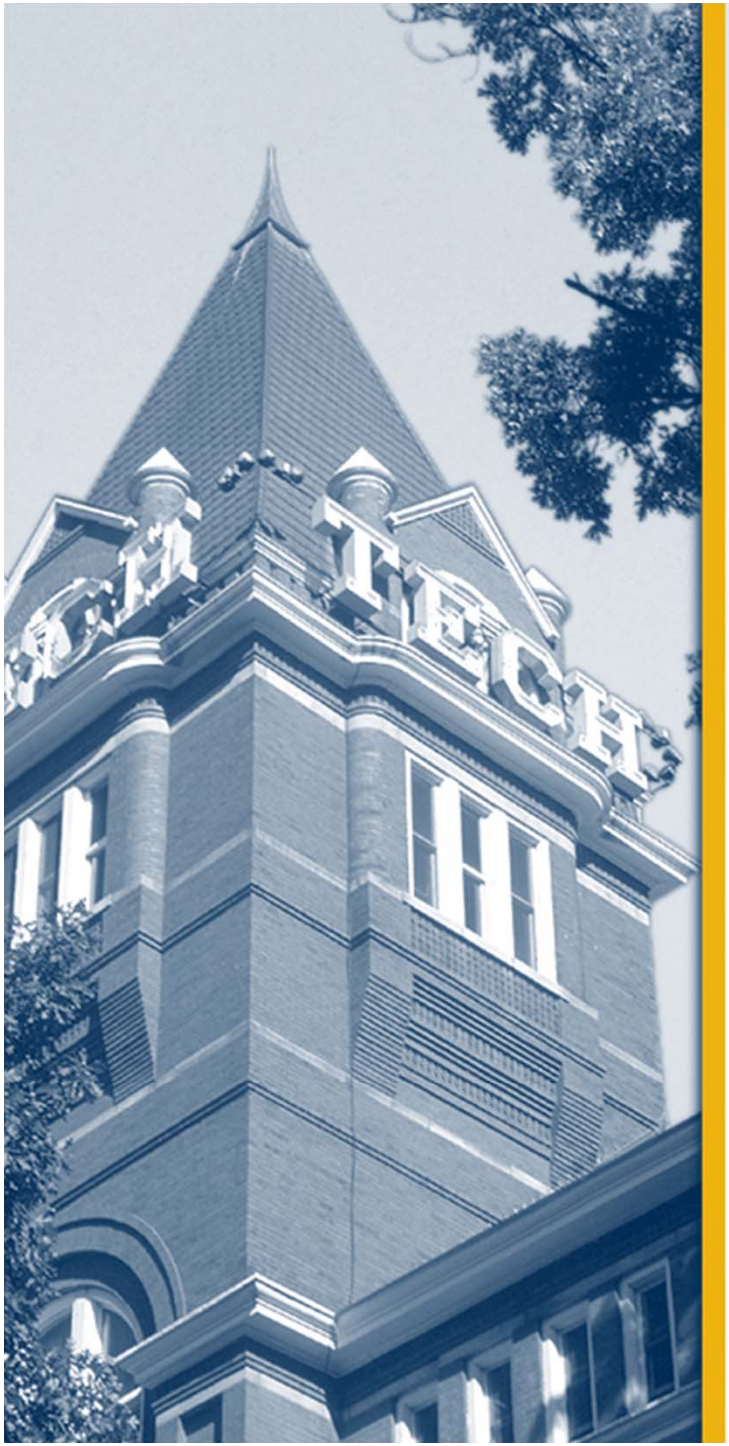

Power MOSFETs

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ECE 3080

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Georgia Institute of Technology

Introduction

- Power MOSFETs were first developed in the late 1970's, first being created by International Rectifier in 1978.
- While Power MOSFETs are voltage controlled, while Bi-polar transistors are current controlled.
- In these respects, power MOSFETs approach the characteristics of an “ideal switch”. They can be found in most power converters, power supplies and low-voltage controllers.

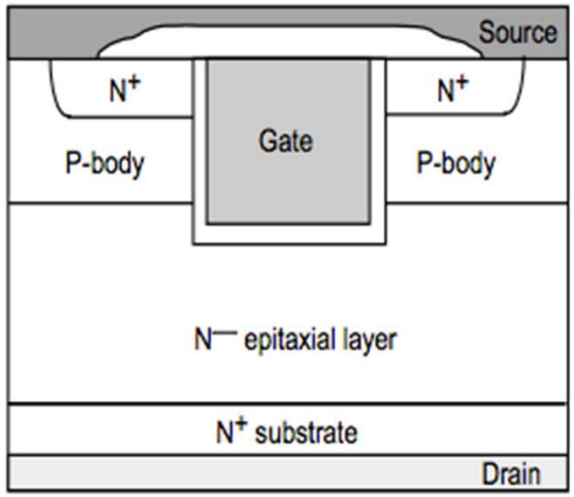
Advantages

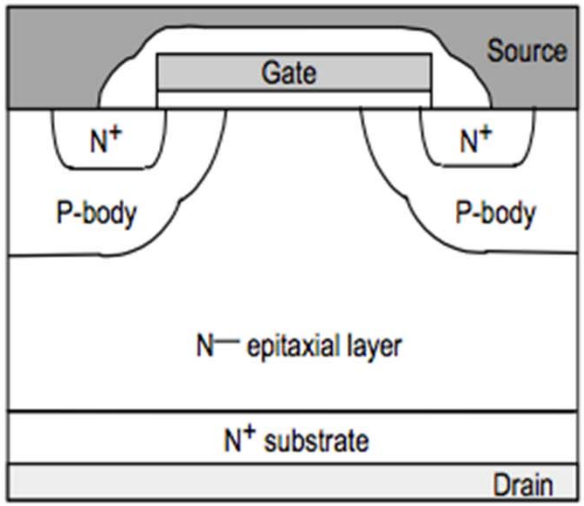
- Power MOSFETs are efficient at lower voltages, and are the most common low-voltage switches.
- Power MOSFETs utilize a vertical structure, which allows the transistor to sustain high current with high-blocking voltage.
- The drive circuit design is simple and less expensive.
- It has a wider SOA than the BJT because high voltage and current can be applied simultaneously for a short duration. This eliminates destructive device failure due to second breakdown.
- They have superior switching speed, have high input impedance, and they require very little gate drive power because of the insulated gate.
- Being a majority carrier device they do not suffer from minority carrier storage time effects, thermal runaway or second breakdown.

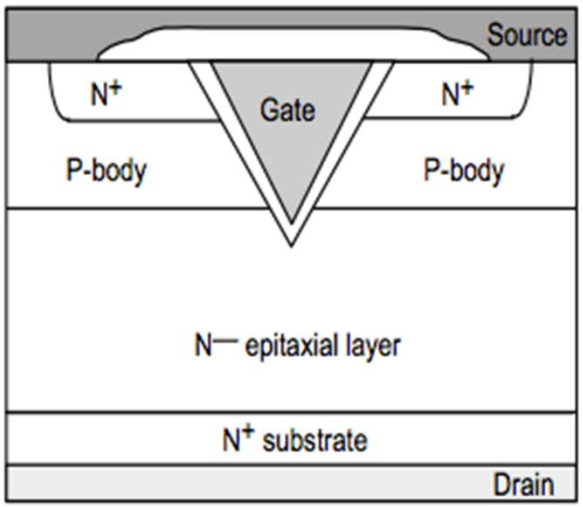
Disadvantages

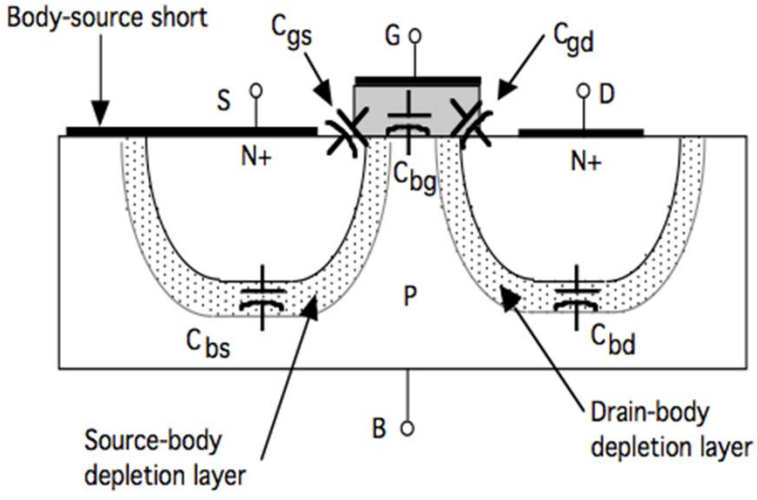
- The gate oxide is very thin (100 nm or less), so it can only sustain a limited voltage.
- The conduction loss of a MOSFET is larger than that of a BJT, which has the same voltage and current rating due to the on-state voltage drop.
- The drain current is limited by heating due to resistive losses in internal components such as bond wires.
- The packaging often limits the maximum junction temperature, which must stay under a specified maximum value for the device to function reliably.

The Structure of the Power MOSFET









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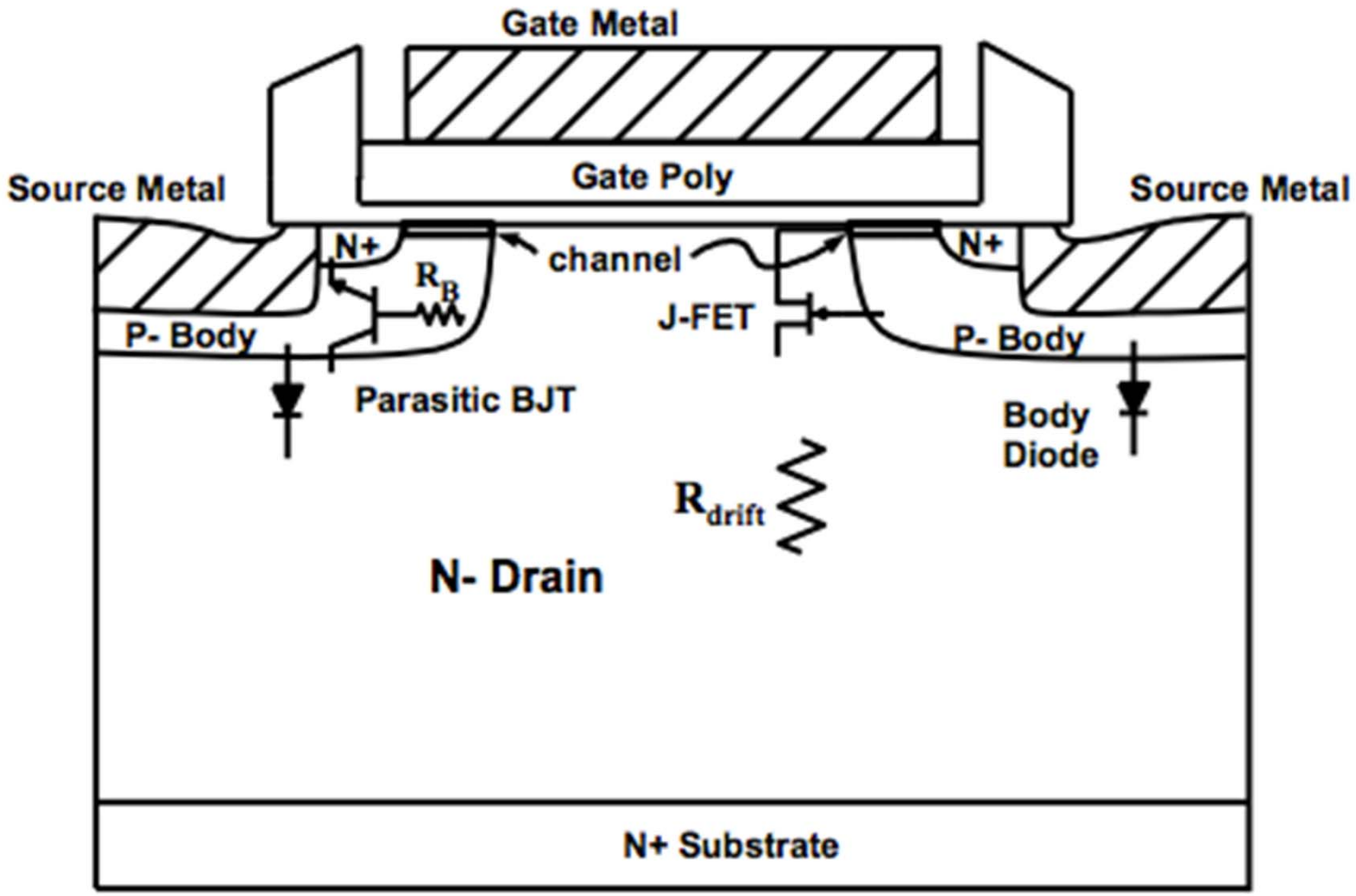
- **Lateral Channel Design**
- The drain, gate, and source terminal are placed on the surface of a silicon wafer. This is suitable for integration but not for obtaining high power ratings since the distance between source and drain must be large to obtain better voltage blocking capability. Also, the drain-to-source current is inversely proportional to the length.
- **Vertical Channel Design**
- The drain and source are placed on the opposite sides of a wafer. This is suitable for a power device, as more space can be used as source. As the length between the source and drain is reduced, it is possible to increase the drain-to-source current rating, and also increase the voltage blocking capability by growing the epitaxial layer (drain drift region).

Intrinsic and Parasitic Elements



Body Diode

- The body-drain p-n junction connected between the drain and source forms an intrinsic diode called the body diode.
- Reverse drain current cannot be blocked because the body is shorted to the source, providing a high current path through the body diode.
- Enhancing the device reduces conduction loss when reverse drain current flows because electrons flow through the channel in addition to electrons and minority carriers flowing through the body diode.
- The intrinsic body diode is convenient in circuits that require a path for reverse drain current (often called freewheeling current), such as bridge circuits in motor control applications.

Parasitic BJT

- The layered MOSFET structure also forms a parasitic NPN bipolar junction transistor (BJT). The body region serves as the base, the source as the emitter and the drain as the collector.

- It is important to keep this BJT OFF of all times by keeping the potential of the base as close to the emitter potential as possible. This is accomplished by shorting the body and the source part of the MOSFET.

- If the BJT were to turn on and saturate, it would result in a condition called latchup, where the MOSFET cannot be turned off except by externally interrupting the drain current. High power dissipation during latchup can destroy the device.

Parasitic JFET

- The parasitic JFET appearing between the two body implants restricts current flow when the depletion widths of the two adjacent body diodes extend into the drift region with increasing drain voltage.
- This JFET has a significant influence on $R_{DS(on)}$ and is part of the normal operation of the MOSFET.

Intrinsic Capacitances

$$C_{gs} = C_O + C_{N^+} + C_P$$

$$C_O = \frac{\varepsilon_I A_O}{t_O}$$

$$C_{N^+} = \frac{\varepsilon_{ox} A_{N^+O}}{t_{ox}} = C_{ox} A_{N^+O}$$

$$C_{gd(\text{per unit area})} = C_{ox}\left(1 - \frac{2W_{d(epi.)}}{X}\right)$$

$$W_{d(epi.)} = \sqrt{\frac{2k_s\varepsilon_o(V_{DS} + \phi_B)}{qC_B}}$$

$$C_{ds(\text{per unit area})} = \sqrt{\frac{qk_s\varepsilon_o C_B}{2(V_{DS} + \phi_B)}}$$

Input capacitance, $C_{iss} = C_{gs} + C_{gd}$

Output capacitance, $C_{oss} = C_{ds} + C_{gd}$

Reverse transfer capacitance, $C_{rss} = C_{gd}$

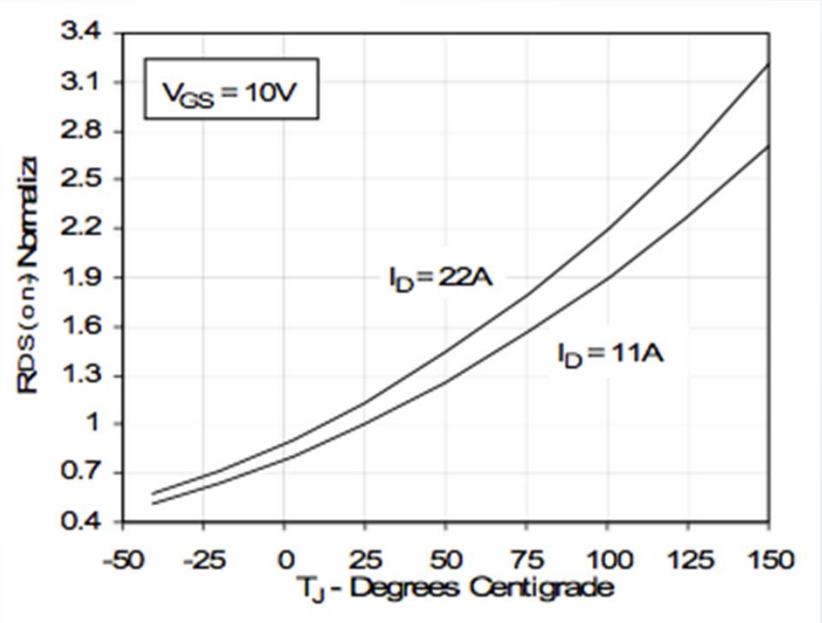
On-Resistance

- The on-resistance can be defined by,

$R_{DS(on)} = R_{Source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml}$

where

- R_{Source} = Source diffusion resistance
- R_{ch} = Channel resistance
- R_A = Accumulation resistance
- R_J = "JFET" component-resistance of the region between the two body regions
- R_D = Drift region resistance
- R_{sub} = Substrate resistance
- R_{wcml} = Sum of Bond Wire resistance, the Contact resistance between the source and drain metallization and leadframe contributions.

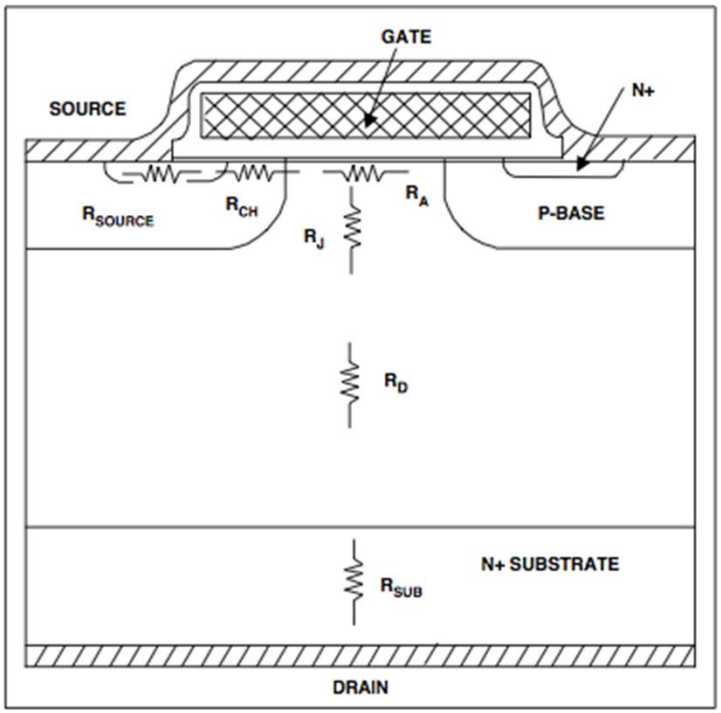


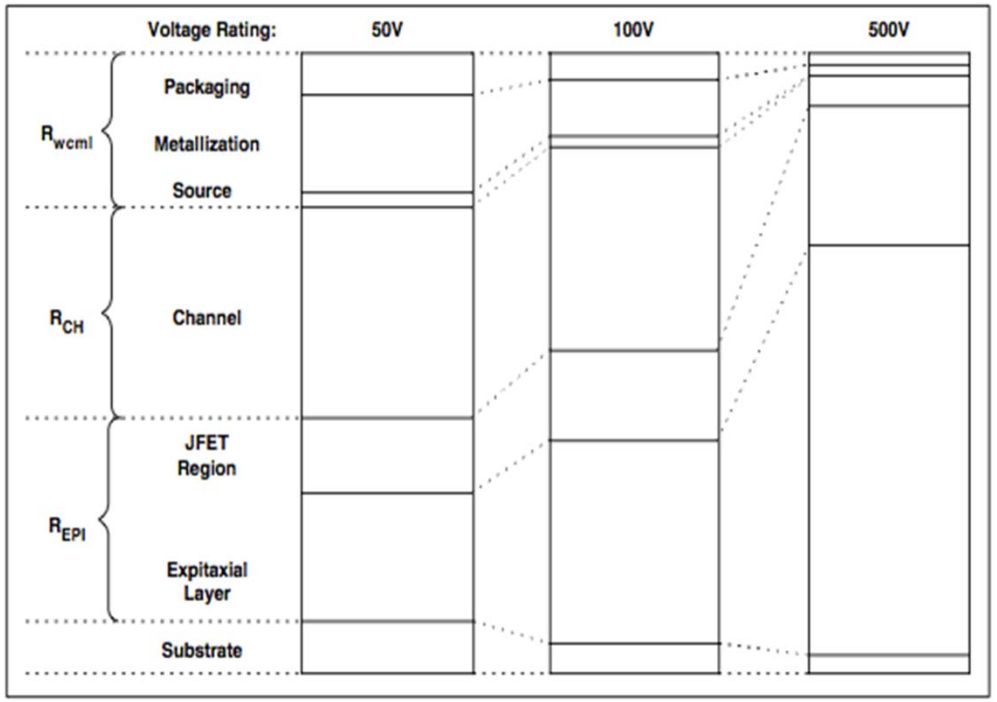
- The on-resistance $R_{DS(on)}$ determines the conduction power dissipation and (due to the bulk resistance of the N- silicon in the drain region) increases with increasing temperature.
- The temperature coefficient of $R_{DS(on)}$ is positive because of majority-only carrier movement; the mobility of the hole and electron decreases as the temperature rises. The $R_{DS(on)}$, at a given temperature of a p / n- channel power MOSFET, can be estimated with the following equation:

$$R_{DS(on)}(T) = R_{DS(on)}(25°C)\left(\frac{T}{300}\right)^{2.3}$$

where T: absolute temperature

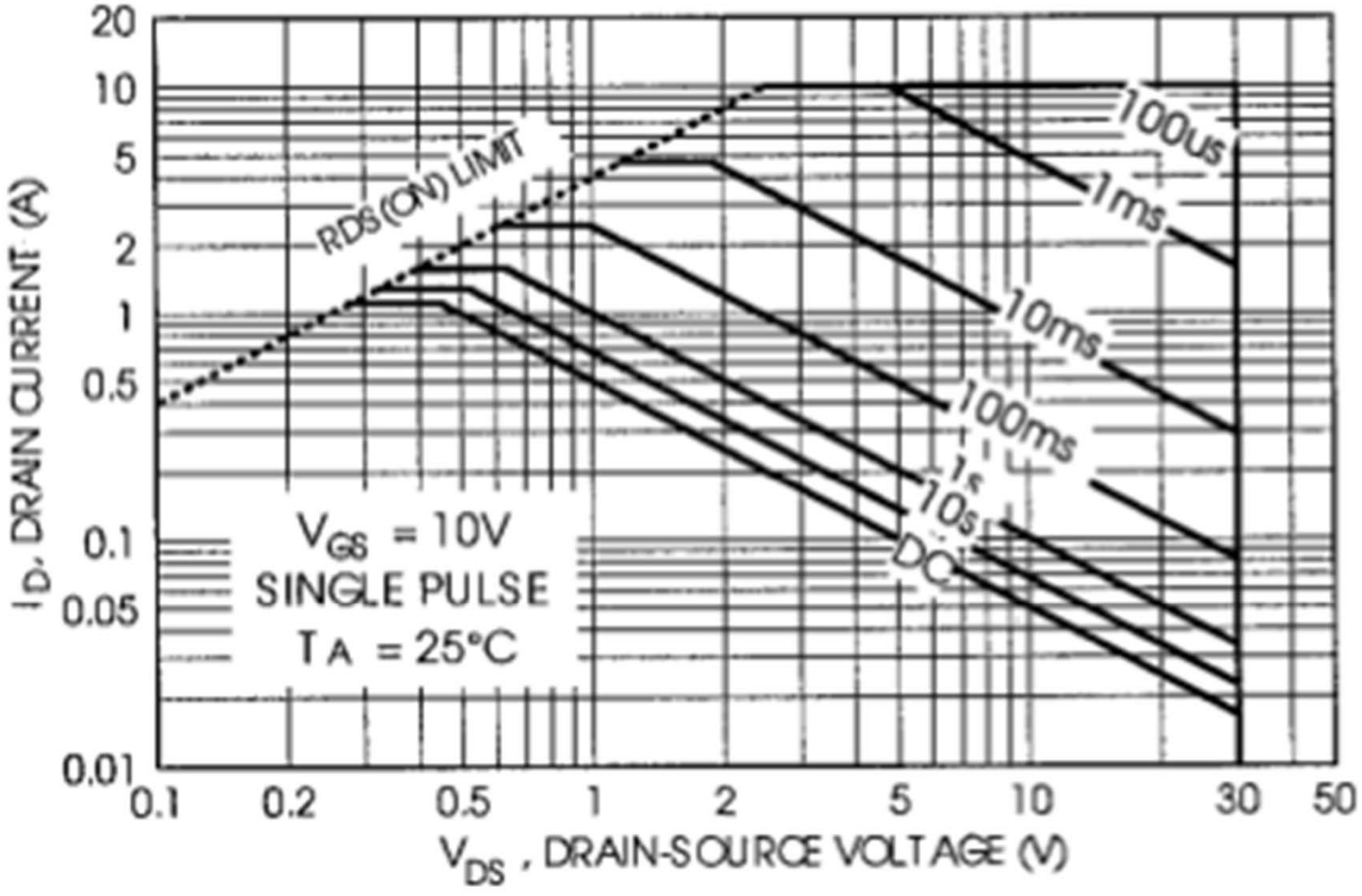
- It is a useful property, which ensures thermal stability when paralleling the devices.


GATE
SOURCE
N+
R_{SOURCE}
R_{CH}
R_J
R_A
P-BASE
R_D
N+ SUBSTRATE
R_{SUB}
DRAIN


Voltage Rating:
50V
100V
500V
R_{wcml}
Packaging
Metallization
Source
R_{CH}
Channel
R_{EPI}
JFET Region
Expitaxial Layer
Substrate

Safe Operating Area

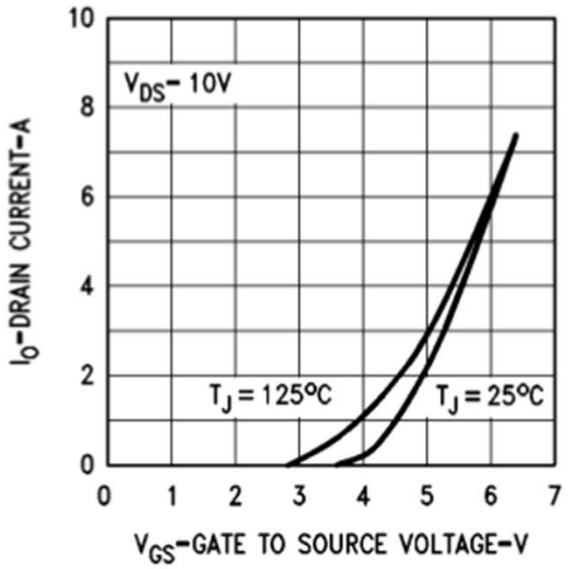
- The safe operating area defines the combined ranges of drain current and drain to source voltage the power MOSFET is able to handle without damage. It is represented graphically as an area in the plane defined by these two parameters.
- Both drain current and drain to source voltage must stay below their respective maximum values, but their product must also stay below the maximum power dissipation the device is able to handle. Thus the device cannot be operated at both its specified maximum drain current and maximum drain to source voltage.


20
10
5
2
1
0.5
0.1
0.05
0.01
I_D, DRAIN CURRENT (A)
RDS(ON) LIMIT
100us
1ms
10ms
100ms
1s
10s
DC
V_{GS} = 10V
SINGLE PULSE
T_A = 25°C
0.1
0.2
0.5
1
2
5
10
30
50
V_{DS}, DRAIN-SOURCE VOLTAGE (V)

Threshold Voltage

- Threshold voltage, $V_{gs(th)}$, is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions.
- It tells how many milliamps of drain current will flow at the threshold voltage, so the device is basically off but on the verge of turning on.
- The threshold voltage has a negative temperature coefficient, meaning the threshold voltage decreases with increasing temperature. The decrease rate increases when the gate oxide becomes thicker and the background doping level increases.
- This temperature coefficient affects turn-on and turn-off delay times and hence the dead-time requirement in a bridge circuit.

- High $V_{gs(th)}$: It is difficult to design gate drive circuitry for the power MOSFET because a high gate bias voltage is needed to turn it on. Also, it lengthens turn-on delay time.
- Low $V_{gs(th)}$: It is undesirable because there could be a spurious turn-on due to gate noise or the increasing gate voltage during high speed switching. Also, it requires thinner oxides which lowers gate oxide voltage rating.



Transconductance

- Transconductance, g_{fs}, is a measure of the sensitivity of drain current to changes in gate-source bias. This parameter is normally quoted for a V_{gs} that gives a drain current equal to about one half of the maximum current rating value and for a V_{ds} that ensures operation in the constant current region.

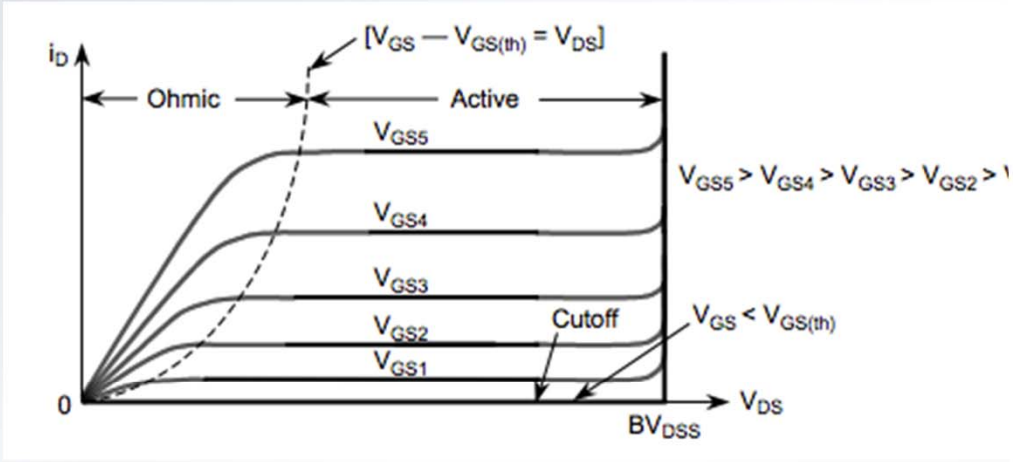
$$g_{fs} = \frac{dI_D}{dV_{gs}}\Big|V_{ds=constant}$$

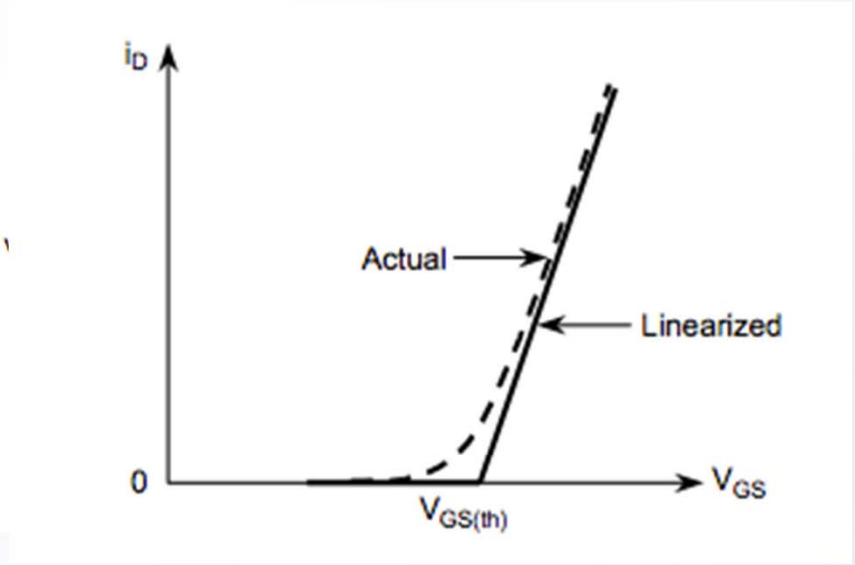
$$g_{fs}(T) = g_{fs}(25°C)\left(\frac{T}{300}\right)^{-2.3}$$

where T: absolute temperature

- Transconductance is influenced by the gate oxide thickness and the channel width/length.
- A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response.
- The reduction in the mobility with increasing temperature decreases transconductance of Power MOSFET.

Output and Transfer Characteristics





- Ohmic region: A constant on-resistance region defined by V_{ds}/I_{ds}. If the drain-to-source voltage is zero, the drain current also becomes zero regardless of gate–to-source voltage. Even if the drain current is very large, in this region the power dissipation is maintained by minimizing the $V_{DS(on)}$.
- Saturation region: A constant current region. Here, the drain current differs by the gate–to- source voltage, and not by the drain-to-source voltage. Hence, the drain current is called saturated.
- Cut-off region: It is called the cut-off region, because the gate-to-source voltage is lower than the $V_{GS(th)}$ (threshold voltage) and the device is an open-circuit or OFF.

$$I_{ds} = K \bullet (V_{gs} - V_{gs(th)})^2 = g_{fs} \bullet (V_{gs} - V_{gs(th)})$$

$$K = \mu_n C_{OX} \frac{W}{2L}$$

where μ_n: carrier mobility

C_{OX}: gate oxide capacitance per unit area

$C_{OX} = \varepsilon_{OX}/t_{OX}$

ε_{OX}: dielectric constant of the silicon dioxide

t_{OX}: thickness of the gate oxide

W: channel width

L: channel length

- When the drain voltage (V_{ds}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. The channel inversion layer charge decreases with increasing V_{ds} and ultimately, it becomes zero when the drain voltage equals to ($V_{gs} - V_{gs(th)}$). This point is called the channel pinch-off point where the drain current becomes saturated

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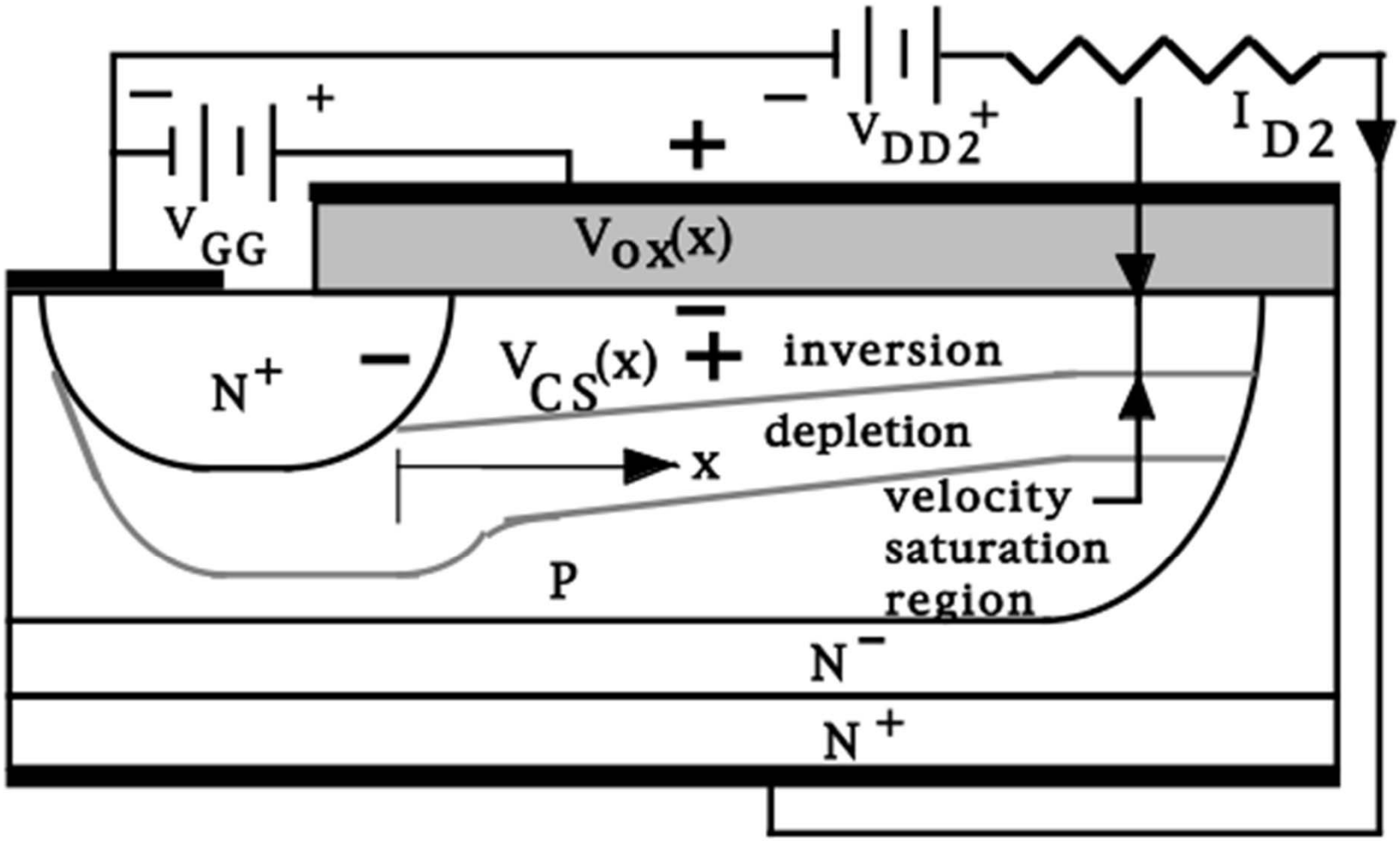
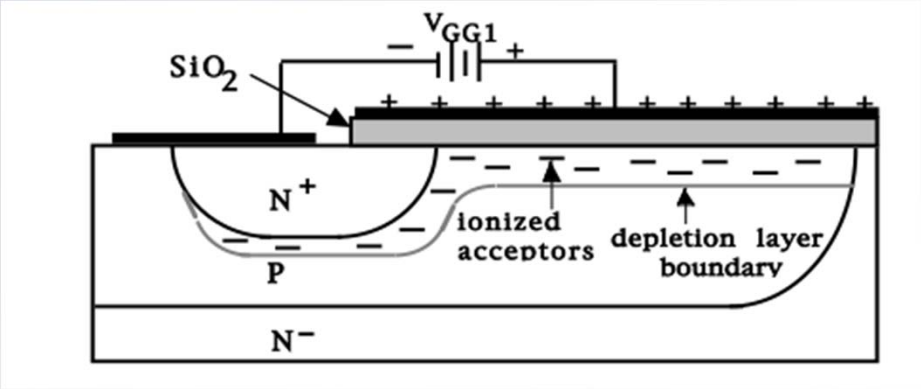
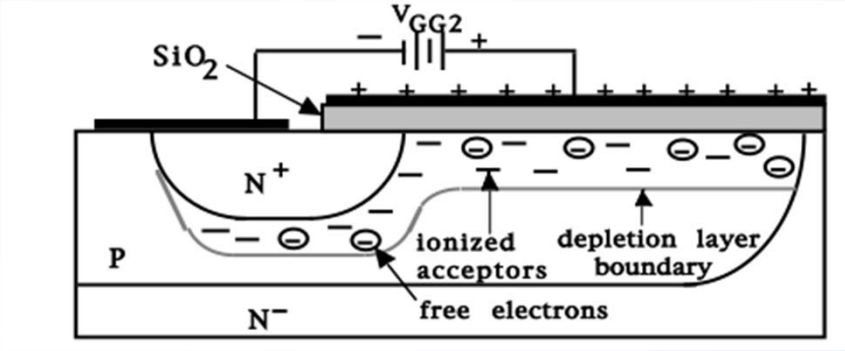
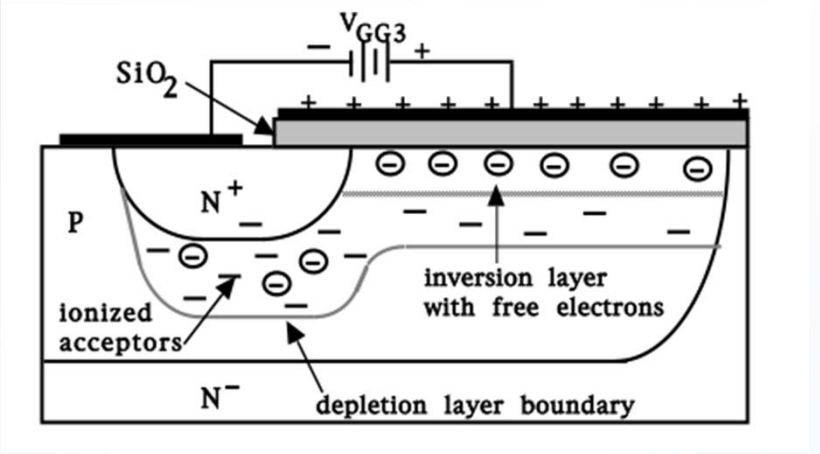

V_GG
V_DD2
I_D2
V_ox(x)
V_CS(x)
inversion
depletion
velocity
saturation
region
x
N+
P
N−
N+

The Process of Channel Formation







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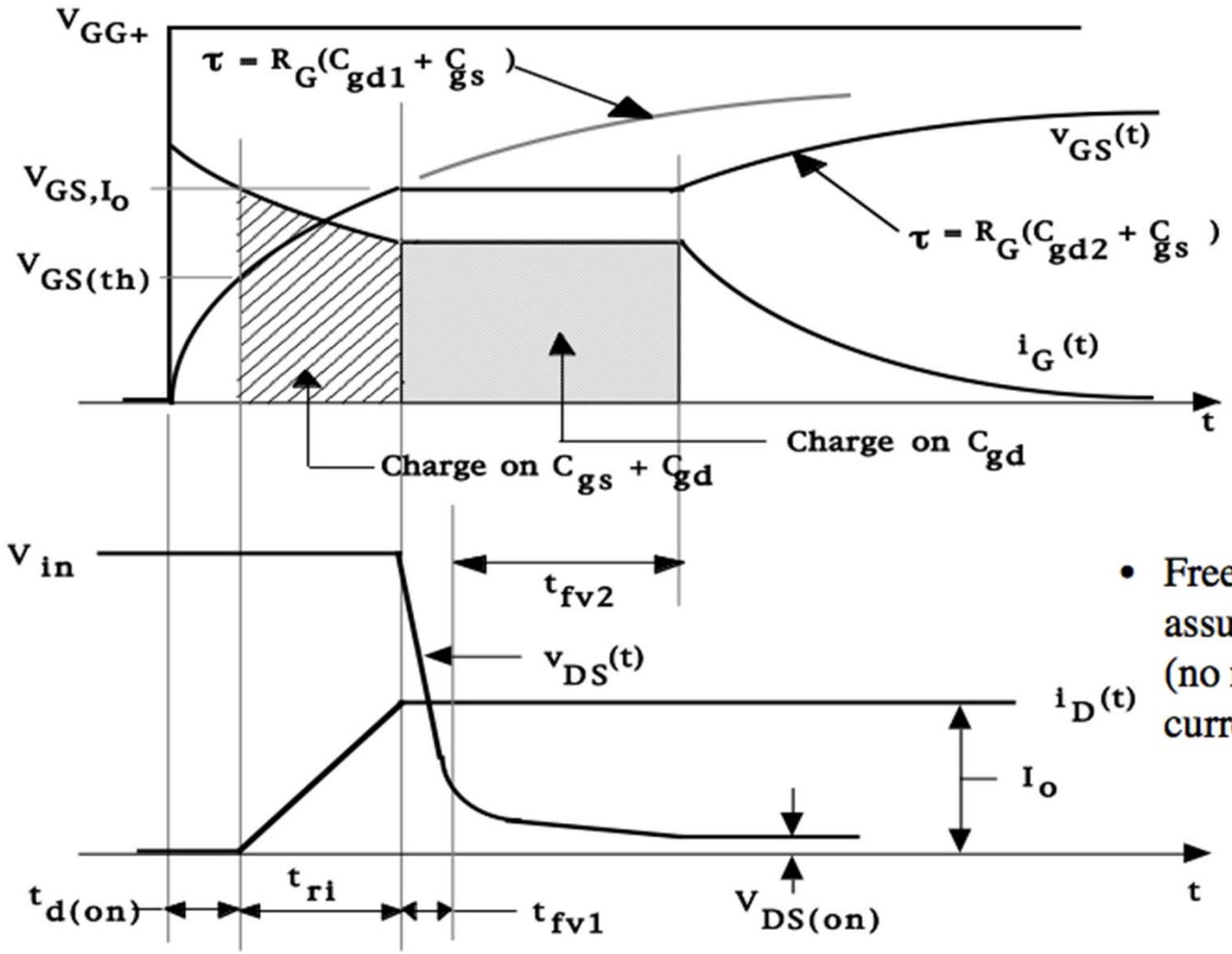
Turn-on Characteristics



- Free-wheeling diode assumed to be ideal. (no reverse recovery current).

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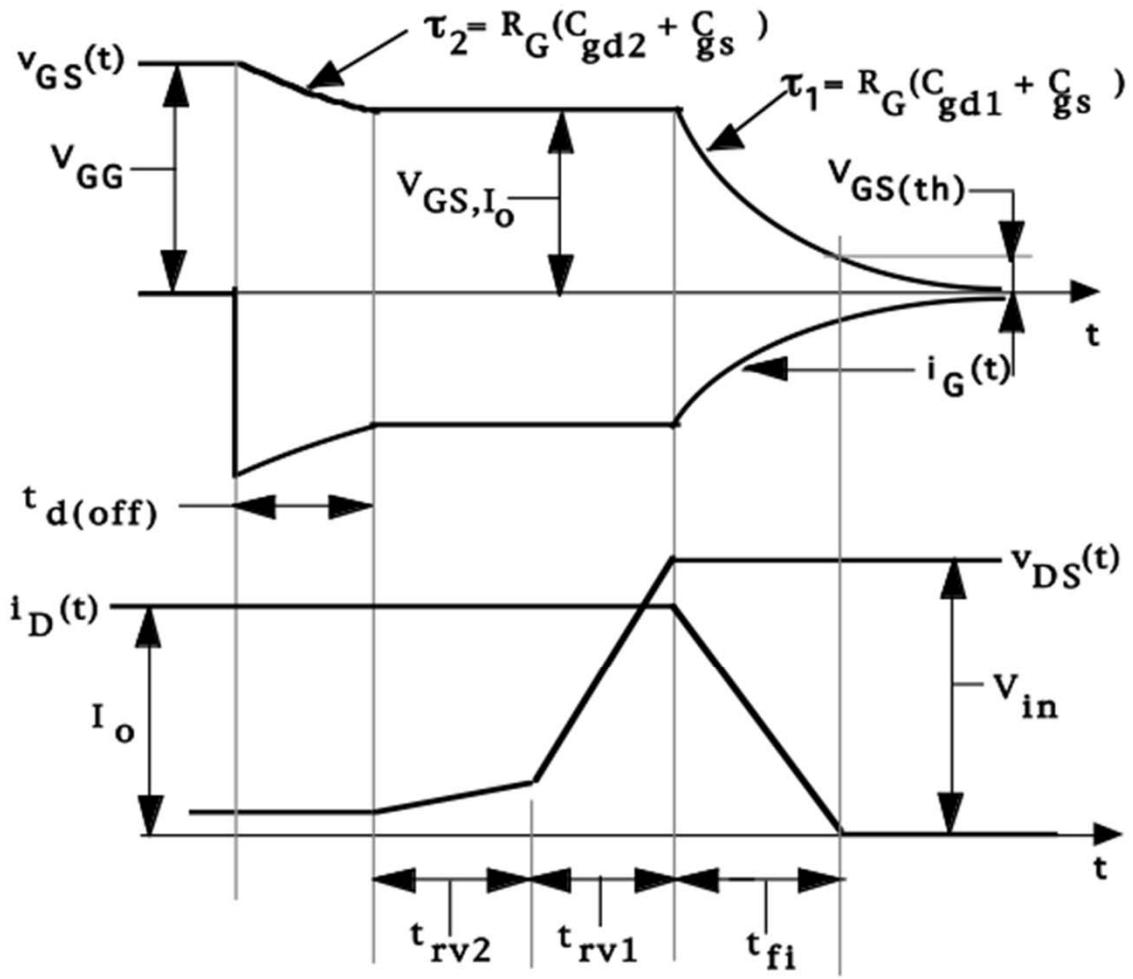
- When the gate is connected to the supply voltage, V_{gs} starts to increase until it reaches $V_{gs(th)}$, at which point the drain current starts to flow and the C_{gs} starts to charge.
- During the period t_1 to t_2, C_{gs} continues to charge, the gate voltage continues to rise and drain current rises proportionally.
- At time t_2, C_{gs} is completely charged and the drain current reaches the predetermined current I_D and stays constant while the drain voltage starts to fall. It can be seen that with C_{gs} fully charged at t_2, V_{gs} becomes constant and the drive current starts to charge the Miller capacitance, C_{gd}. This continues until time t_3.

- Charge time for the Miller capacitance is larger than that for the gate to source capacitance C_{gs} due to the rapidly changing drain voltage between t_2 and t_3 ($I = C\ dv/dt$).
- Once both of the capacitances C_{gs} and C_{gd} are fully charged, gate voltage (V_{gs}) starts increasing again until it reaches the supply voltage at time t_4.
- The gate charge ($Q_{gs} + Q_{gd}$) corresponding to time t_3 is the bare minimum charge required to switch the device on. Good circuit design practice dictates the use of a higher gate voltage than the bare minimum required for switching and therefore the gate charge used in the calculations is Q_g corresponding to t_4.

Turn-off Characteristics



- Assume ideal free-wheeling diode.
- Essentially the inverse of the turn-on process.
- Model quanitatively using the same equivalent circuits as for turn-on. Simply use correct driving voltages and initial conditions

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- Turn-off occurs in reverse order. The turn-off process is initiated by applying a step gate voltage of $-V_{GG}$.
- The V_{gs} must drop back close to the threshold value before $R_{DS(on)}$ will start to increase.
- As V_{ds} starts to rise, the Miller effect due to C_{gd} re-occurs and impedes the rise of V_{gs} as C_{gd} recharges to V_{CC}.
- On-state power dissipation

$$P_c = I_c^2 r_{ds}$$

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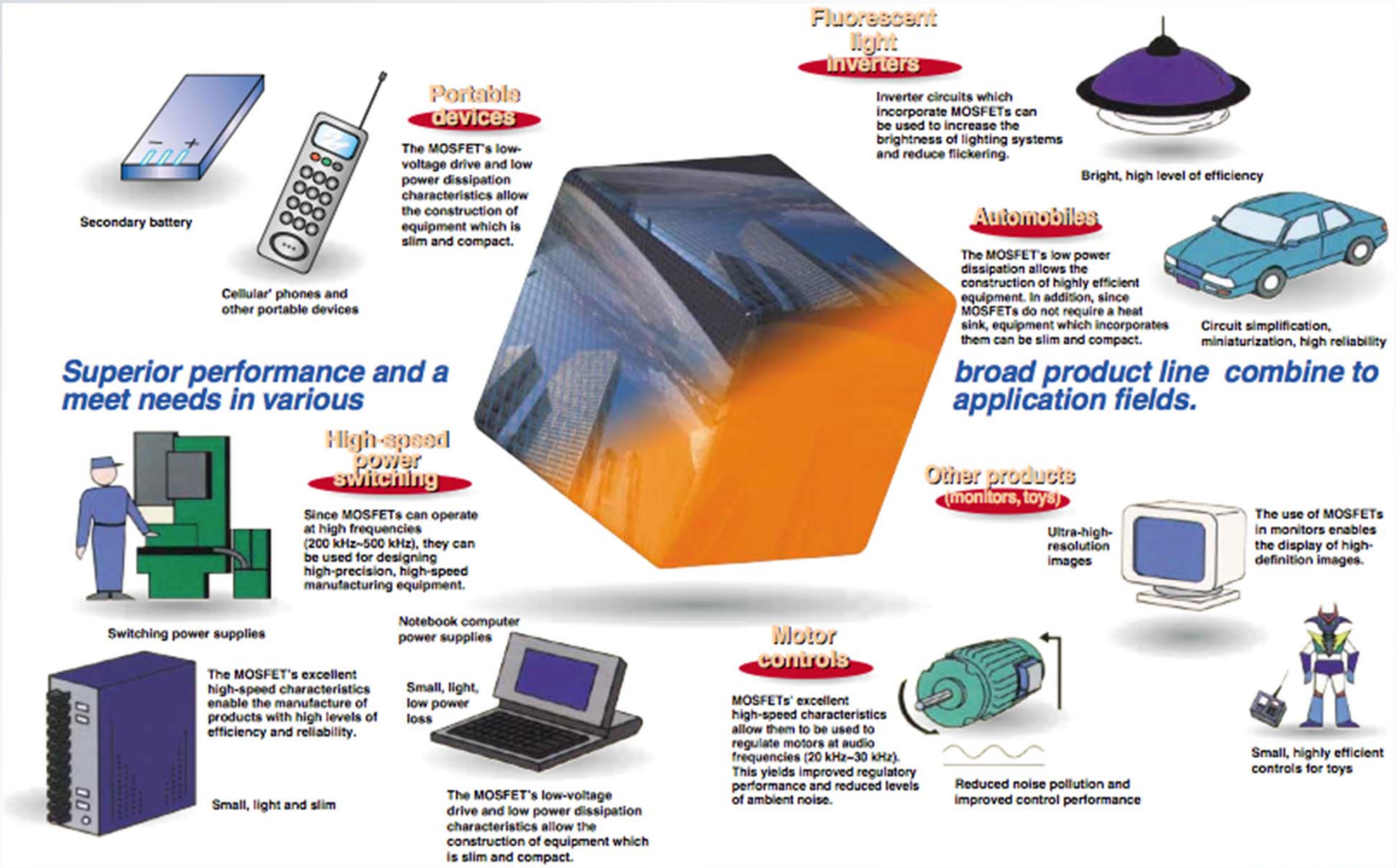
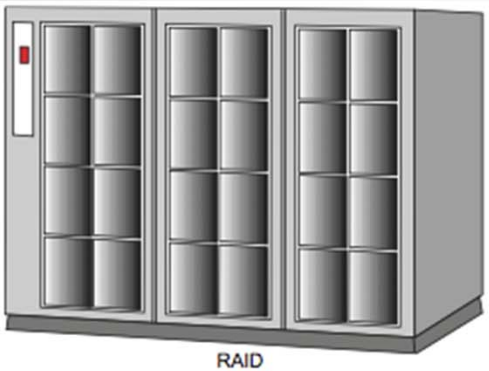
Drain-to-Source dv/dt Rating

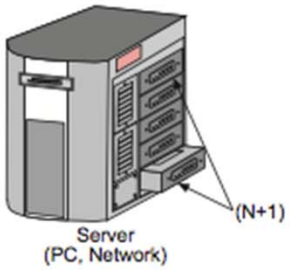
- If this rate is exceeded then the voltage across the gate-source terminals may become higher than the threshold voltage of the device, forcing the device into current conduction mode, and under certain conditions a catastrophic failure may occur.
- There are two possible mechanisms by which a dv/dt induced turn-on may take place.
  - Static
    - False turn-on
    - Parasitic BJT turn-on
  - Dynamic
    - A clamped inductive turn-off in high speed switching, the device is destroyed by concurrent stresses caused by high drain current, high drain-source voltage, and displacement current at the parasitic capacitance.

Applications



Example Power-Switching Application

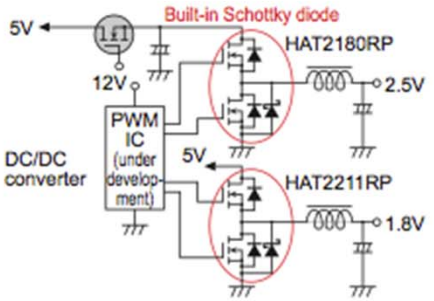


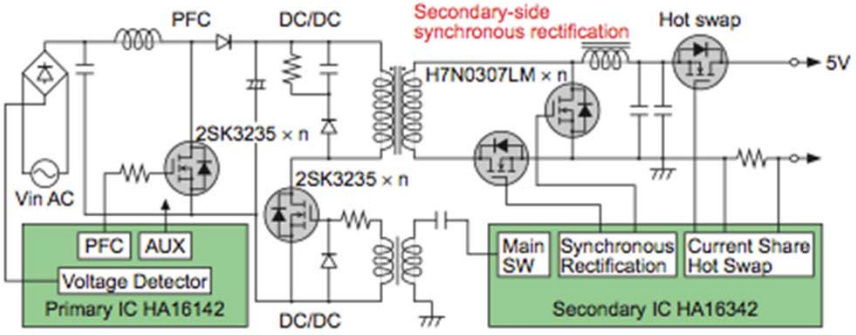


Application Blocks

Application	MOS FET	Control IC
PFC PFC+PWM	500V	HA16142 HA16158*
DC/DC	500V	HA16341 HA16342
Secondary-side synchronous rectification	30 to 60V	
Hot swap	20 to 30V	
VRM	20 to 30V	—

* : Under development





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