Power Device: SiC MOSFET

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Background

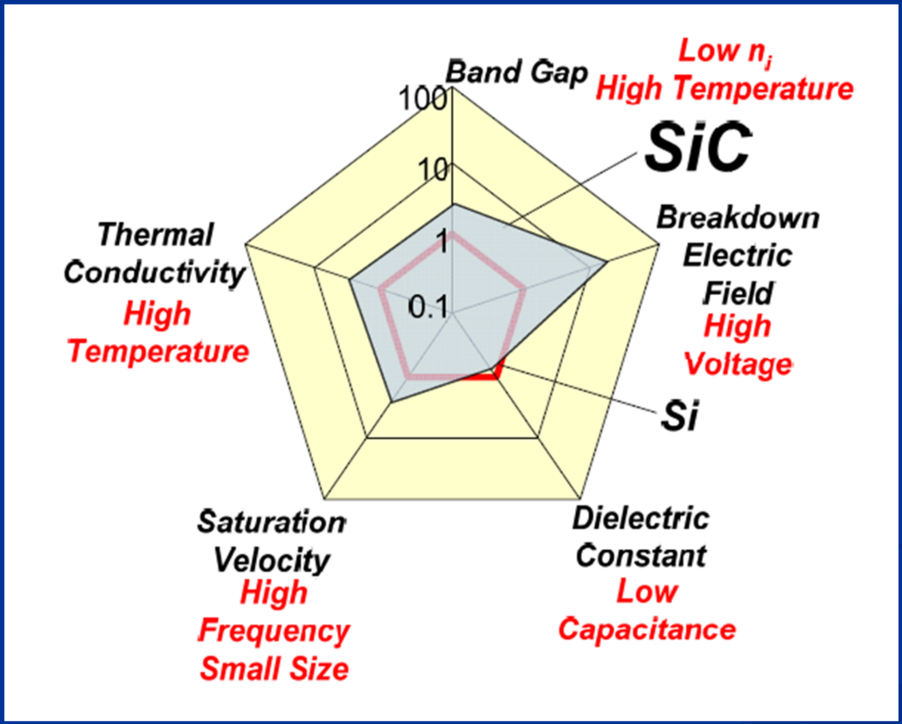
- What is a Power Device?
  - Essentially a Switch
  - Blocks current at “off” state
  - Conducts current at “on” state
  - Ideally want no energy loss when switching from on/off state
  - State is “on” when voltage reaches the breakdown voltage, V_{BD}

Background

- Applications
  - $V_{BD} < 1000$ V
    - – Switch-mode power supplies
    - –Uninterrupted power supply
  - $V_{BD} > 1000$ V
    - – Hybrid vehicles
    - – Motor drives
    - – Avionics (lower weight)
    - – Inverters/converters: alternative energy (solar, wind)
    - – Defense (Navy: electric ships)

SiC vs Si

- Why Silicon Carbide?



SiC MOSFET

- SiC MOSFETs perform well
  - Efficient Switching
  - High blocking voltage
  - High temperature
  - High frequency due to high Saturation Velocity

SiC MOSFET

- SiC MOSFETs have a big disadvantage over other SiC (or other materials such as Si) power devices.
  - Main Reason: High R_{DSON} (On-Resistance)
    - Ideally want Low On-resistance for no current loss during “on” state.

    $R_{DSON} = R_D + R_{CH} + R_{contacts} + \ldots$

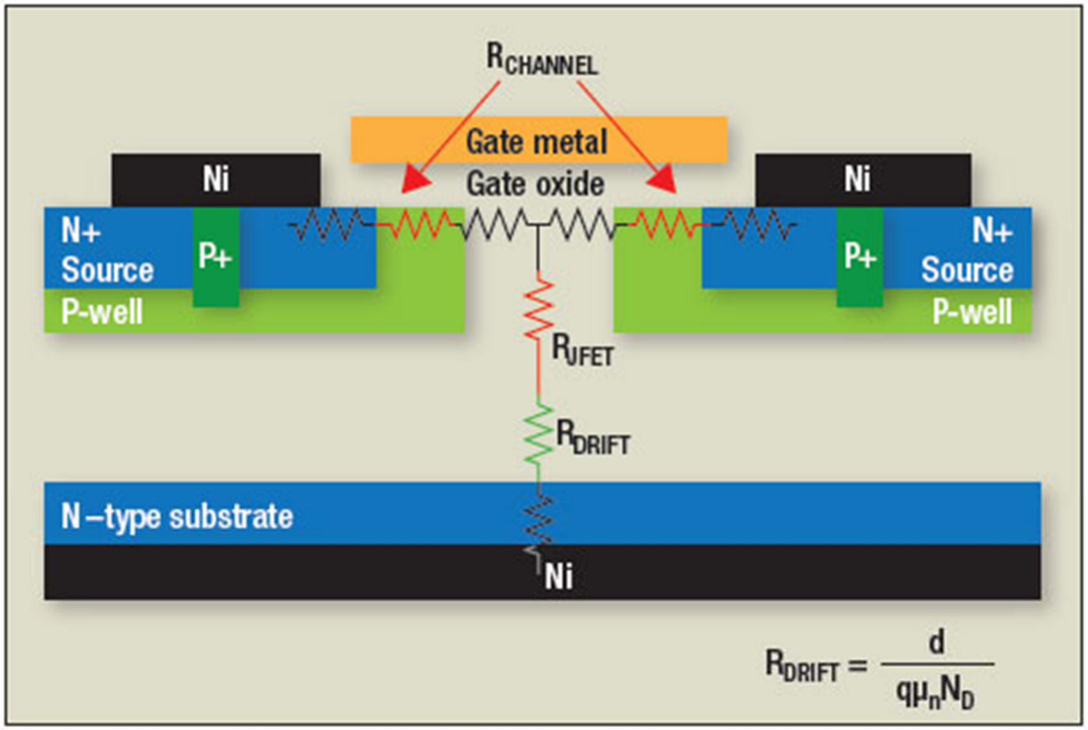


Fig. 1. *Cross-section of DMOSFET power transistor shows its resistive components: the channel resistance, the inherent JFET resistance and the drift resistance that combine to produce a relatively high on-resistance.*

Decreasing On-resistance

"The new generation of SiC MOSFETs cuts drift-layer thickness by nearly a factor of 10 while simultaneously enabling the doping factor to increase by the same order of magnitude. The overall effect results in a reduction of the drift resistance to 1/100th of its Si MOSFET equivalent."

"In light of recent silicon carbide (SiC) technology advances, commercial production of 1200-V 4H-SiC power MOSFETs is now feasible. There have been improvements in 4H-SiC <u>substrate quality and epitaxy, optimized device designs and fabrication processes, plus increased channel mobility with nitridation annealing</u>"

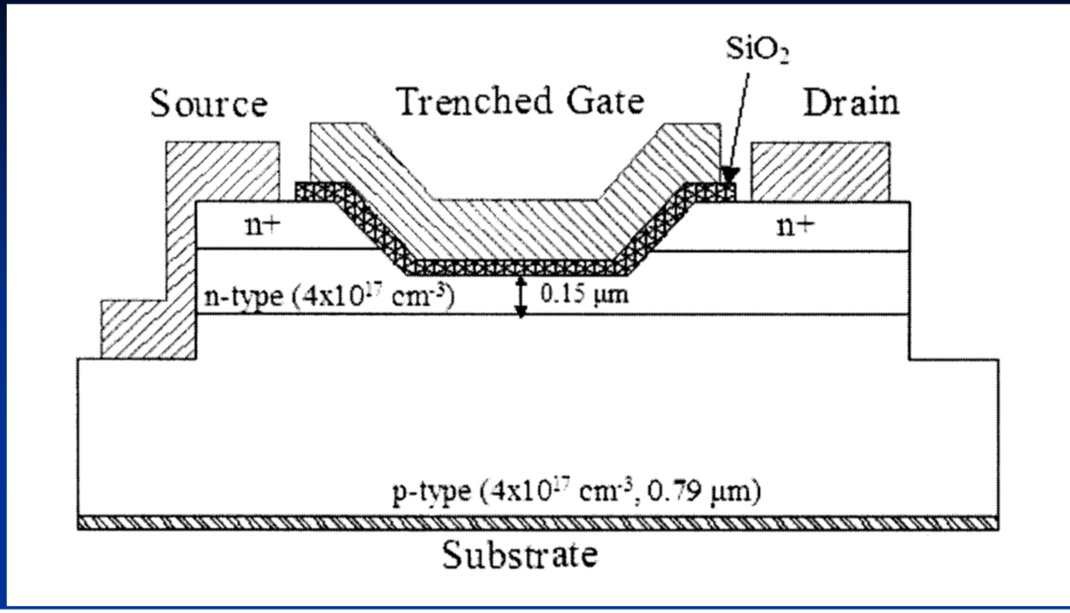
The EPILAYER

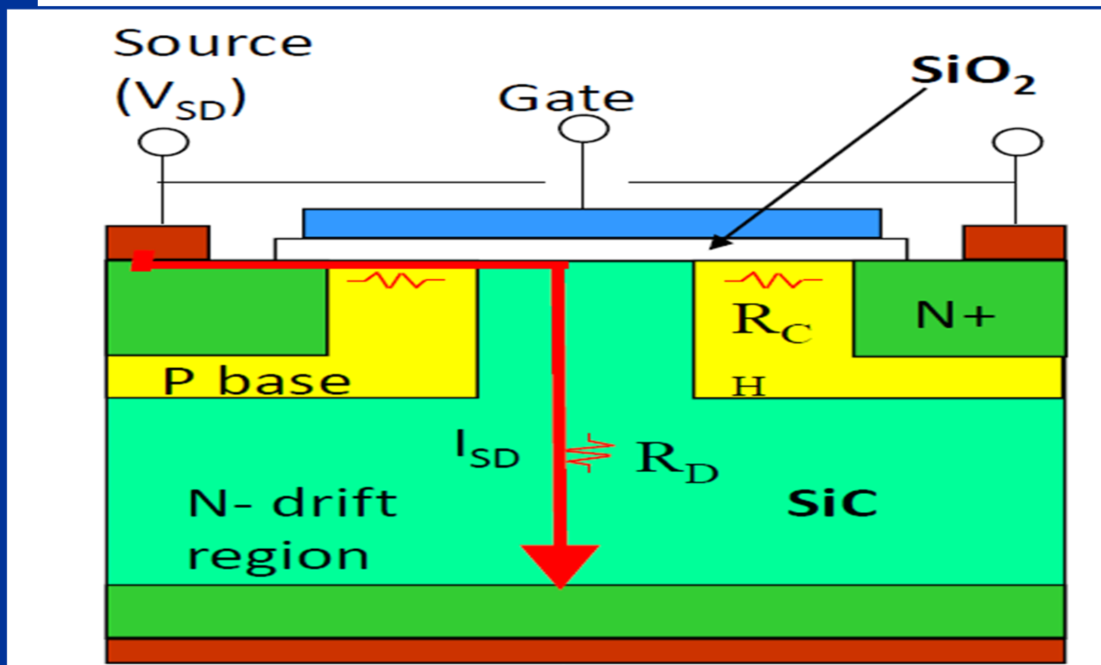
One of the solutions to decreasing High on-resistance:

- Highly Doped Epilayer
  - Epilayer?
    - → a.k.a. Epitaxial Layer
  - Epitaxy!!
  - Depositing a monocrystalline film on a monocrystalline substrate

The Trenched 4H-SiC MOSFET

- Electrons getting trapped in the SiC/SiO_2 causes low channel mobility.
- Buried a highly doped n-type Epitaxial layer into MOSFET using inductively-coupled plasma (ICP) etching.
- Keeps electrons away from the inferior SiC/SiO_2 interface layer.
- Attempts to prevent near-interface traps.
- Still not enough!


SiO2
Source
Trenched Gate
Drain
n+
n+
n-type (4x10^17 cm^-3)
0.15 µm
p-type (4x10^17 cm^-3, 0.79 µm)
Substrate

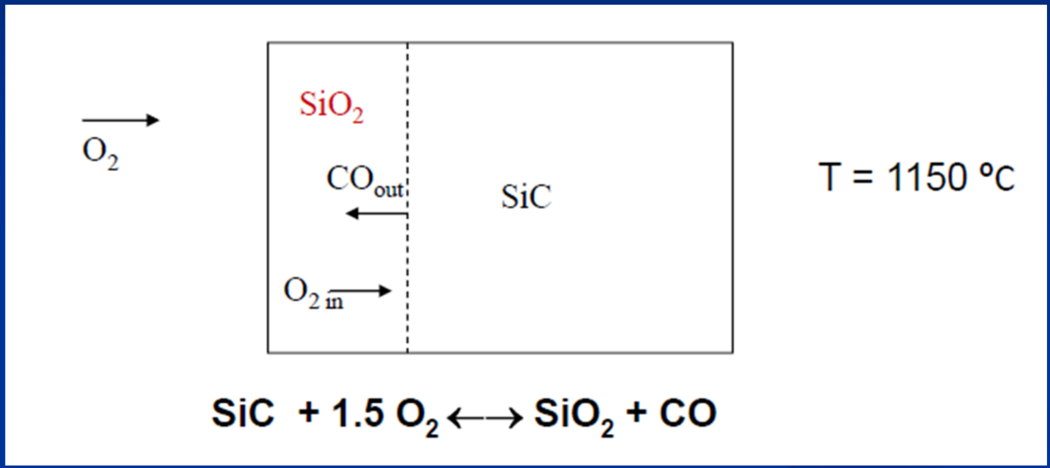

Source
(V_SD)
Gate
SiO2
N+
R_C
H
P base
I_SD
R_D
N- drift
region
SiC

Nitridation Annealing

- The trench model above also was annealed in NO.
- Annealing – heat treatment of semiconductor

    – Nitridation annealing proved to increase channel mobility
- NO annealing passivates the SiC/SiO_2 by creating S and N bonds.
- Gets rid of Oxide traps (90%)

Unsolved Problem
Oxidation – Near interface traps



- – Transport of molecular oxygen gas to the oxide surface.
- – In-diffusion of oxygen through the oxide film.
- – Reaction with SiC at the oxide/SiC interface.
- – Removal of C from interface as CO.
- – Out-diffusion of CO through the oxide film i.e removal of C.
- – C may form defects in the oxide and at the interface or may diffuse into SiC.

Unsolved Solutions

- Near interface traps created during Oxidation still remains a problem

The Future

- Cree has reported the feasibility of 1200-V 4H-SiC[1] power MOSFET.
- However....

Property	Si	4H-SiC	6H-SiC
Band gap (eV)	1.1	3.26	3.0
Thermal Conductivity ($W\ cm^{-1}\ s^{-1}$)	1.5	4.5	4.5
SiC Electron Mobility ($cm^2\ V^{-1}\ s^{-1}$)	1350	850	370
Channel Electron Mobility ($cm^2\ V^{-1}\ s^{-1}$)	820	30-50	40

Even after the improvements such as nitridation annealing and the trenched gate model, the channel electron mobility is still too low!

Summary

- SiC is the most promising materials for making power devices.
- MOSFETs are needed as high voltage and temperature switch.
- SiC MOSFETs are defective due to trapping (low channel mobility)
- Improvements in fabrication processes, design, and material quality have been made