Lecture 12

MOS Field Effect Devices

How do they work? (math included for completeness but skipped in lectures as this should be a review of ECE 3040 material – Needed for advanced FET Device discussion)

Reading:

(Cont’d) Notes and Anderson^2 Chapter 7

MOS Capacitor

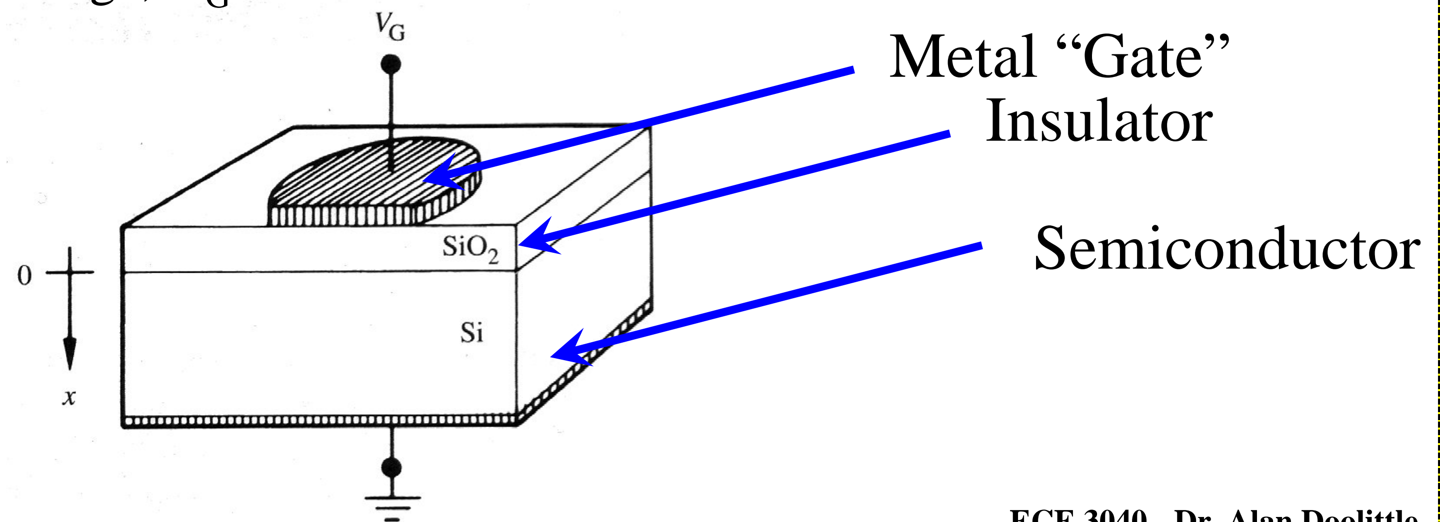
"MOS" = Metal- Oxide- Semiconductor

"MOS" actually refers to "Metal"– Silicon Dioxide – Silicon

Other material systems have similar "MIS" structures formed by Metal – Insulator – Semiconductor

The capacitor itself forms the basis of digital logic circuits, and DRAM storage units (storing charge) or can simply supply a capacitance for an analog integrated circuit. It will also be the building block for the most common transistor produced – the MOS transistor.

The substrate is normally taken to be grounded and the "Gate" electrode can be biased with a voltage, V_G



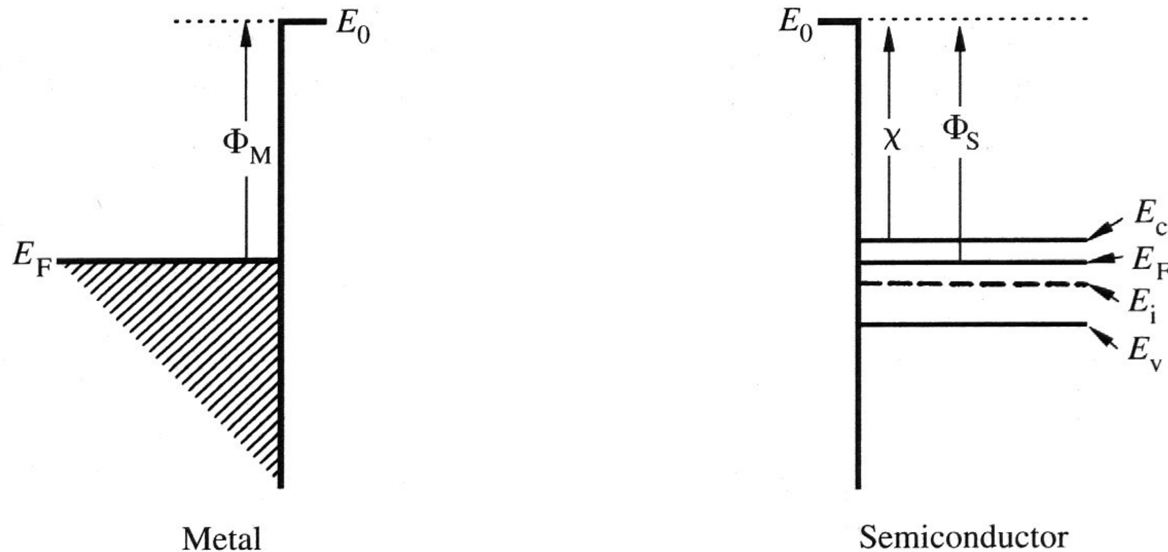
MOS Capacitor

Key assumptions:

1) Metal is an equipotential region.
2) Oxide is a perfect insulator with zero current flow.
3) Neither oxide nor oxide-semiconductor interface have charge centers.
4) Semiconductor is uniformly doped.
5) An ohmic contact has been established on the back side of the wafer.
6) Analysis will be one-dimensional.
7) The semiconductor is thick enough to have a quasi-neutral region (where electric field is zero and all energy bands are flat).
8) Certain energy relationships exist:

$$\Phi_M = \Phi_S = \chi + (E_C - E_F)_{FB}$$ (terms defined in next few slides)

MOS Capacitor



E_O= Vacuum Energy Level. The minimum energy an electron must have to free itself from the material.

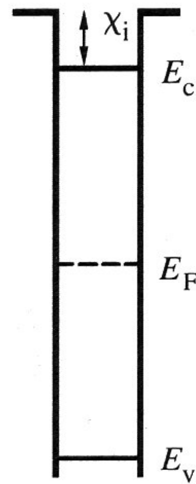
Φ_M = "Work function" of the metal. This is the energy difference from the fermi energy (average energy) of an electron in the metal to the vacuum energy level.

Φ_S = "Work function" of the semiconductor. This is the energy difference from the fermi energy (average energy) of an electron in the semiconductor to the vacuum energy level. Note that this energy depends on doping since E_F depends on doping

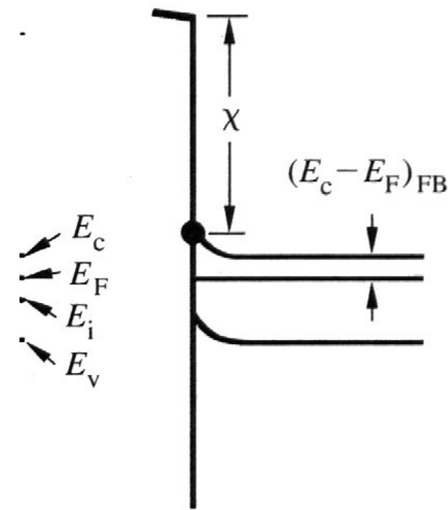
χ = Electron Affinity of the semiconductor. This is the energy difference from the conduction band minimum in the semiconductor to the vacuum energy level. Note that this energy does NOT depend on doping

$(E_C - E_F)_{FB} = \Phi_S - \chi$ in the quasi-neutral region where the bands are not bent or are in "flat band"

MOS Capacitor



Insulator

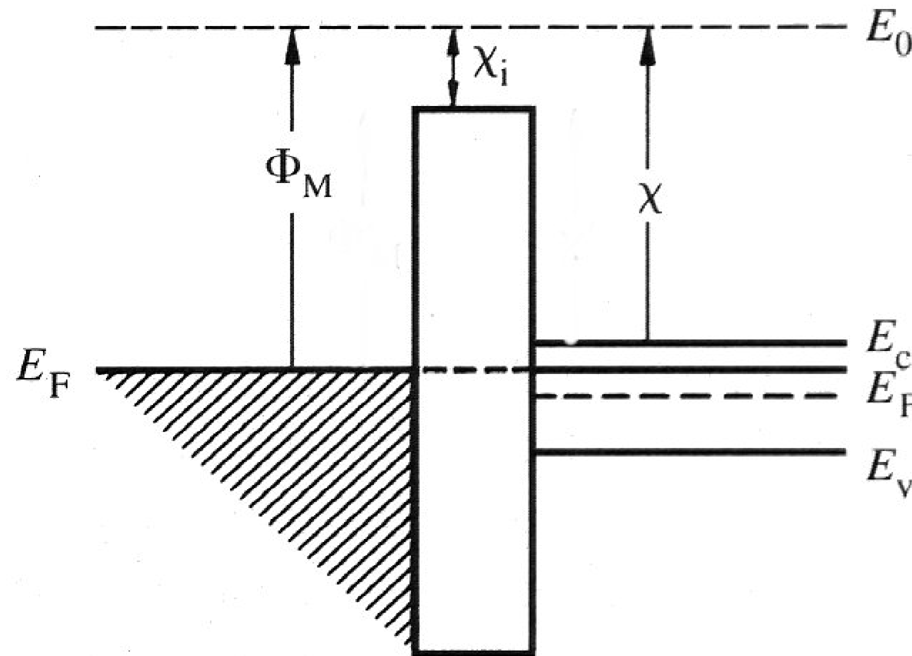


Semiconductor with band bending

The insulator is simply a very wide bandgap, intrinsically doped semiconductor characterized by an electron affinity, χ_i .

The semiconductor can have an electric field near the insulator that forces the energy bands to bend near the insulator-semiconductor interface.

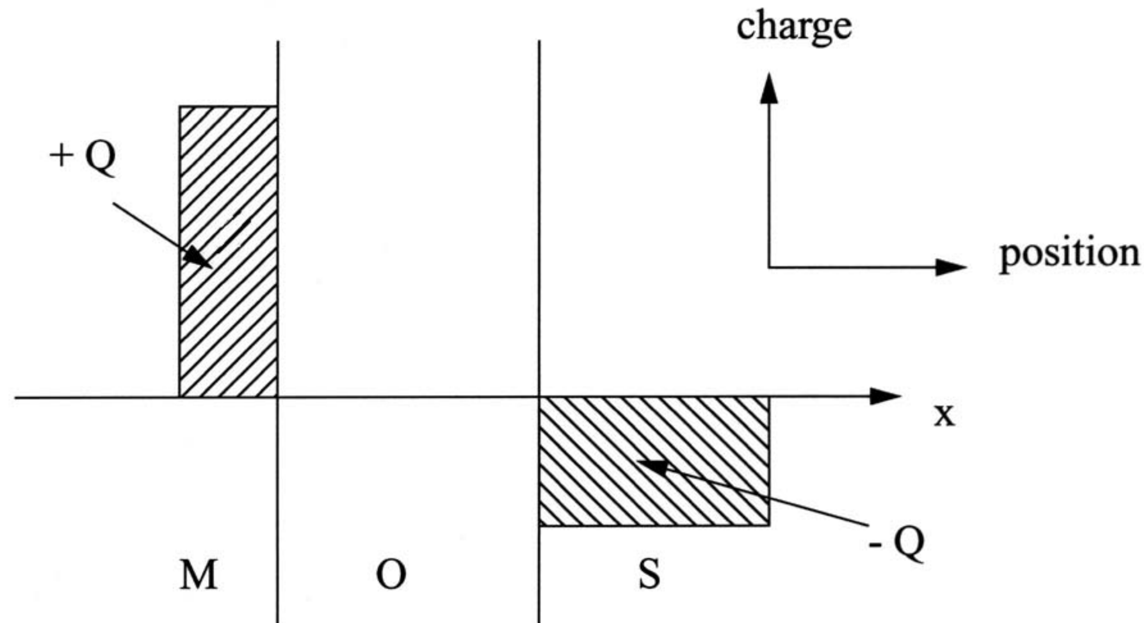
MOS Capacitor



Since the insulator prevents any current from flowing, when we bring the materials together, the fermi-energy must be flat.

Likewise, if no charges are stored on the “plates” (metal and semiconductor regions near the insulator) of the capacitor, the bands are not bent in the insulator nor semiconductor. Note the assumption of an equipotential surface in the metal simply states that a perfect conductor can not support and electric field (electrostatics).

MOS Capacitor
Capacitor under bias



A positive voltage on the gate puts positive charge on the gate electrode. Gauss's law forces an equal negative charge to form near the semiconductor-insulator interface.

Charge separated by a distance implies an electric field across the insulator.

MOS Capacitor

Capacitor under bias

If V_G = bias voltage applied to the gate (metal).

For all V_G the Fermi level *in the each layer* remains flat due to zero current through the structure.

The applied bias separates the Fermi levels at the metal and semiconductor ends by qV_G

$$E_F(\text{metal}) - E_F(\text{semiconductor}) = -qV_G$$

If the semiconductor is grounded (fixed at any constant potential we can call ground):

- metal side Fermi level moves downward if $V_G > 0$
- metal side Fermi level moves upward if $V_G < 0$

Applying Poisson's equation to the oxide, since there are no charges in the oxide,

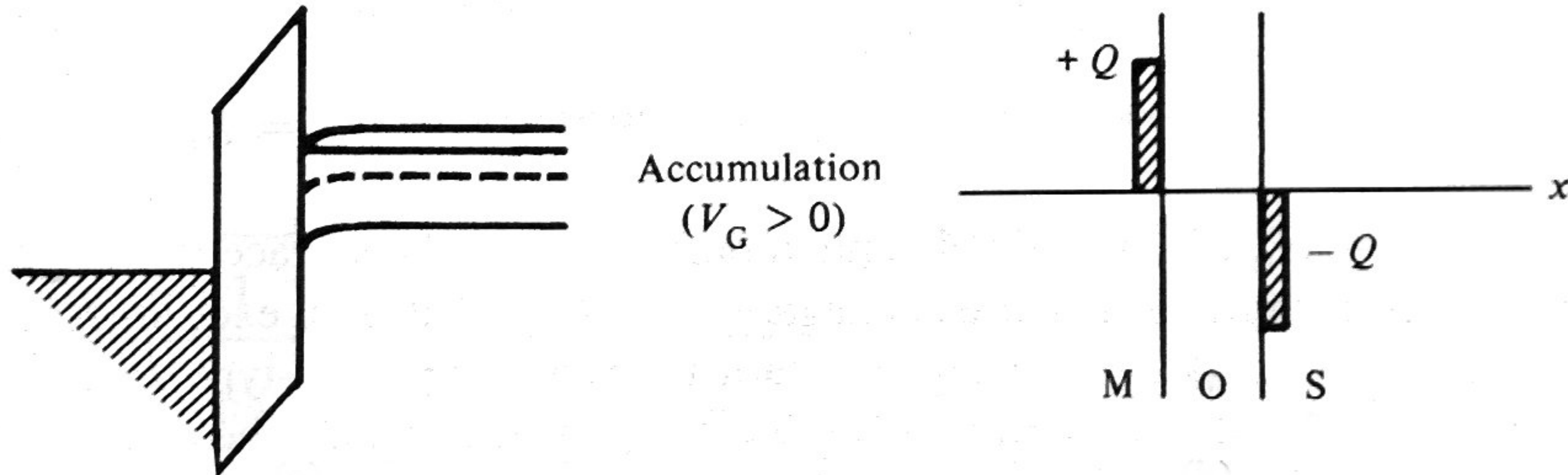
$$\frac{dE_{oxide}}{dx} = \rho = 0 \quad \Rightarrow \quad E_{oxide} = Constant$$

$$V = \int E_{oxide} dx \Rightarrow Potential \text{ varies linearly with x}$$

Since the potential varies linearly with x, so does the energy bands

MOS Capacitor

Capacitor under bias



For an n-type semiconductor.

•When $V_G > 0$ the metal fermi-energy is lowered (E=-qV), the insulator has an electric field across it that terminates almost immediately in the near perfectly conducting metal, but terminates over a finite distance in the semiconductor of "finite resistivity".

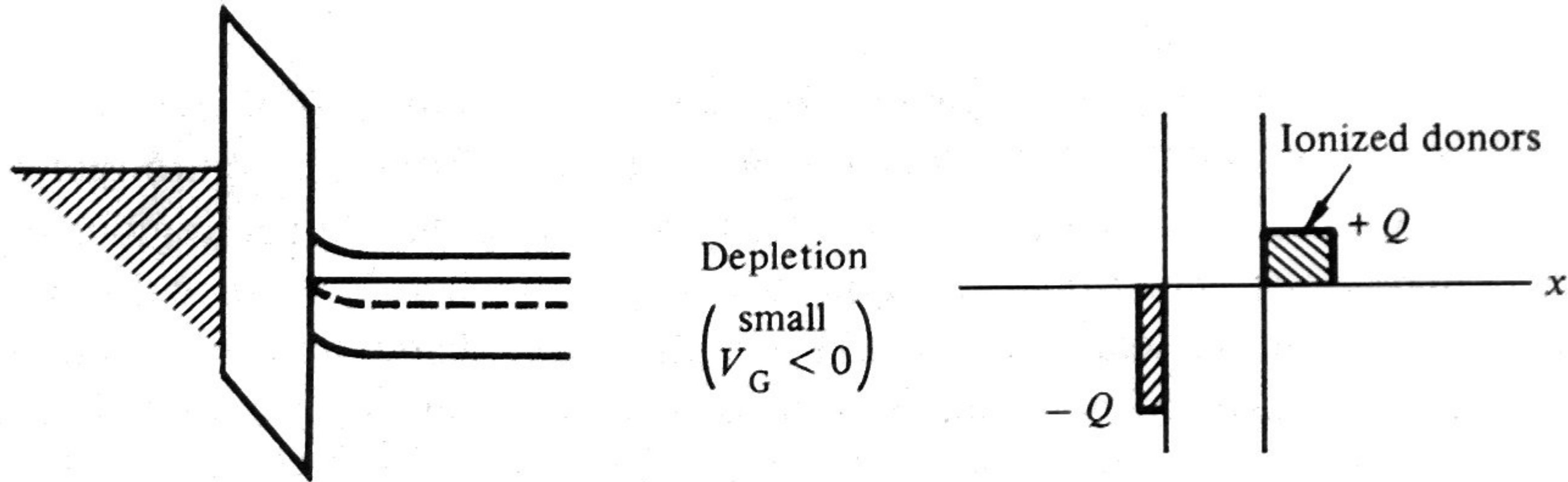
•The charge model indicates that negative charge must be created in the semiconductor near the interface. This charge is in the form of electrons.

•Since $n = n_i \exp[(E_F - E_i)/ kT]$, the electron concentration in the semiconductor near interface increases.

•This is called ***accumulation***

MOS Capacitor

Capacitor under bias



For an n-type semiconductor.

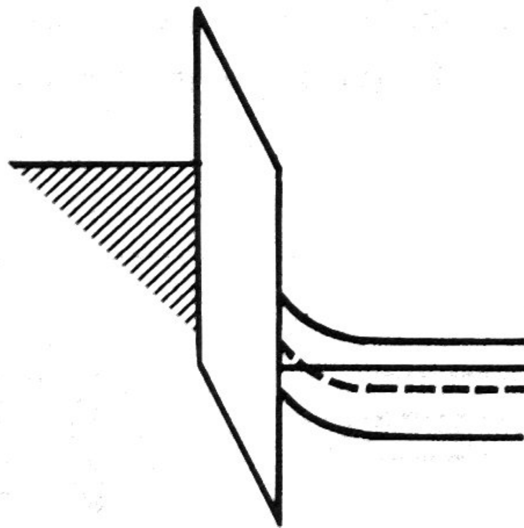
•When $V_G < 0$ the metal fermi-energy is **raised** (E=-qV), the insulator has an electric field across it that terminates almost immediately in the near perfectly conducting metal, but terminates over a finite distance in the semiconductor of "finite resistivity".

•The charge model indicates that positive charge must be created in the semiconductor near the interface. This charge is in the form of ionized donors.

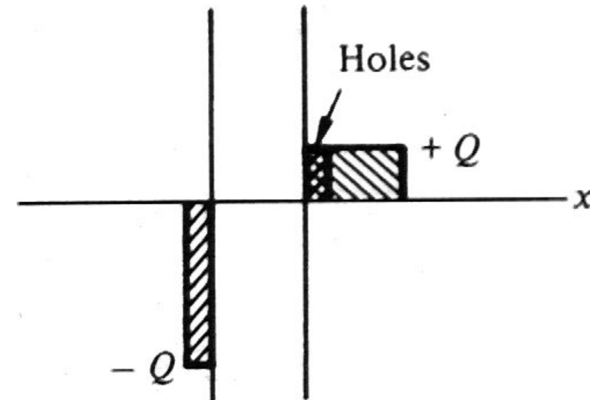
•Since $n = n_i \exp[(E_F - E_i)/ kT]$, the electron concentration in the semiconductor near interface decreases.

•This is called ***depletion***.

MOS Capacitor
Capacitor under bias



Onset of inversion ($V_G = V_T$)



For an n-type semiconductor.

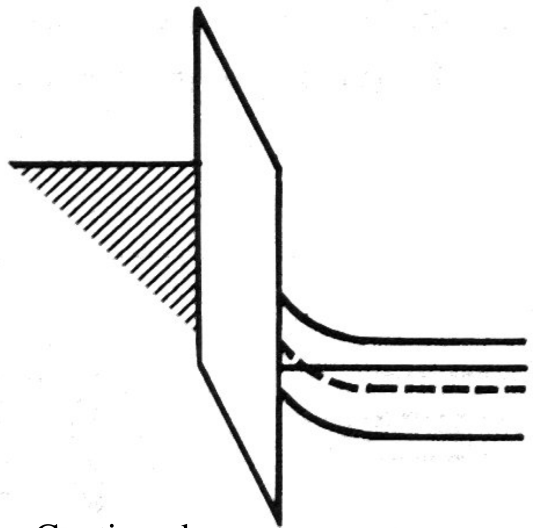
•For higher magnitudes of bias ($V_G < 0$) the fermi-energy near the interface crosses-the intrinsic energy and the "type" of material swaps from n-type to p-type (only locally near the interface).

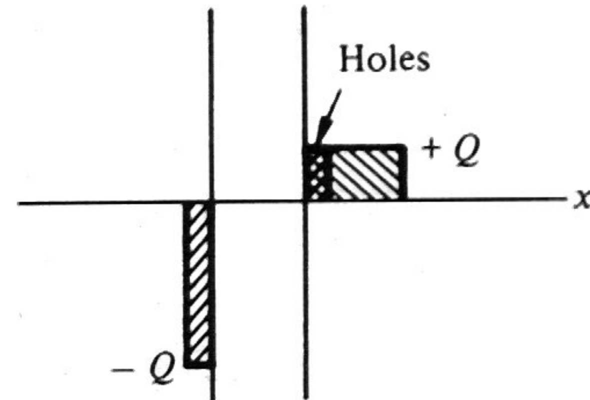
•The charge model indicates that positive charge must be created in the semiconductor near the interface. This charge is in the form of ionized donors and holes.

Inversion continued on next slide…

MOS Capacitor

Capacitor under bias





Onset of inversion ($V_G = V_T$)

Inversion Continued…

- The hole concentration near the interface must equal the donor concentration. Thus,

$$p_{interface} = N_D$$

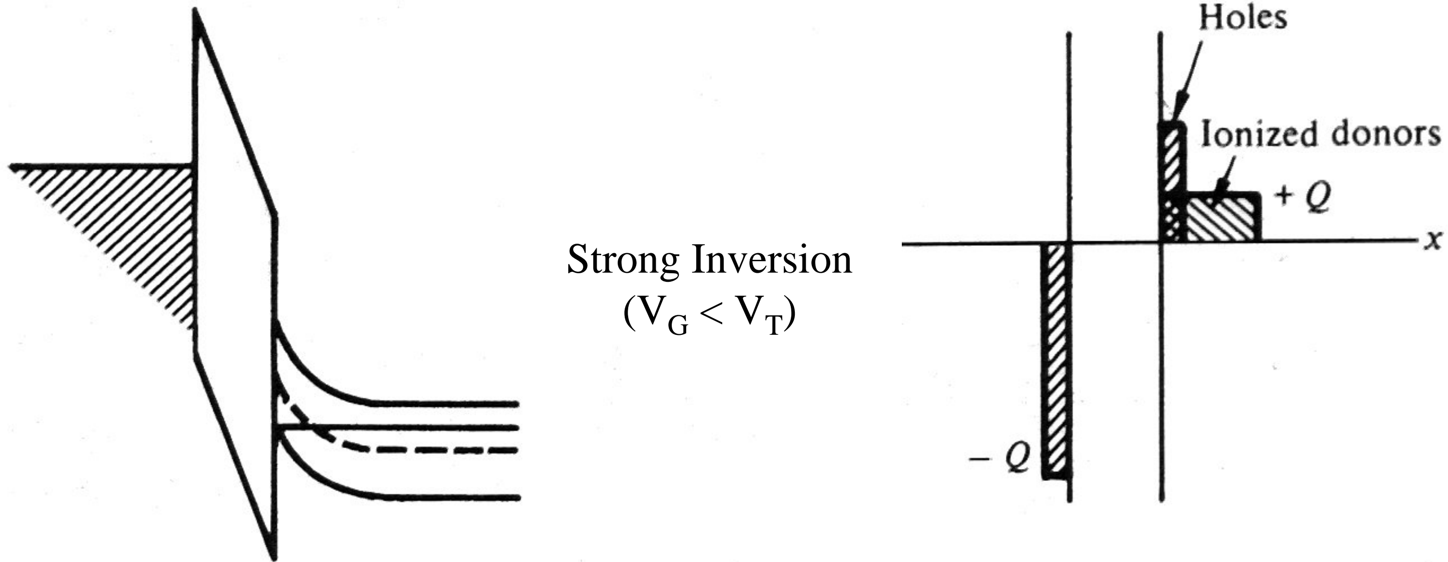
$$p_{interface} = n_i \exp[(E_{i\text{-INTERFACE}} - E_F)/ kT] = n_i \exp[(E_F - E_{i\text{-BULK}})/ kT]$$

- This is called ***inversion***.
- The onset of inversion occurs for a voltage called the ***threshold voltage V_T*** (not thermal voltage)
- Detailed calculations taking into account the charge distribution as a function of position in the semiconductor indicates that inversion occurs when,

$$E_{i\text{-INTERFACE}} - E_{i\text{-BULK}} = 2\,(E_F - E_{i\text{-BULK}})$$

MOS Capacitor

Capacitor under bias



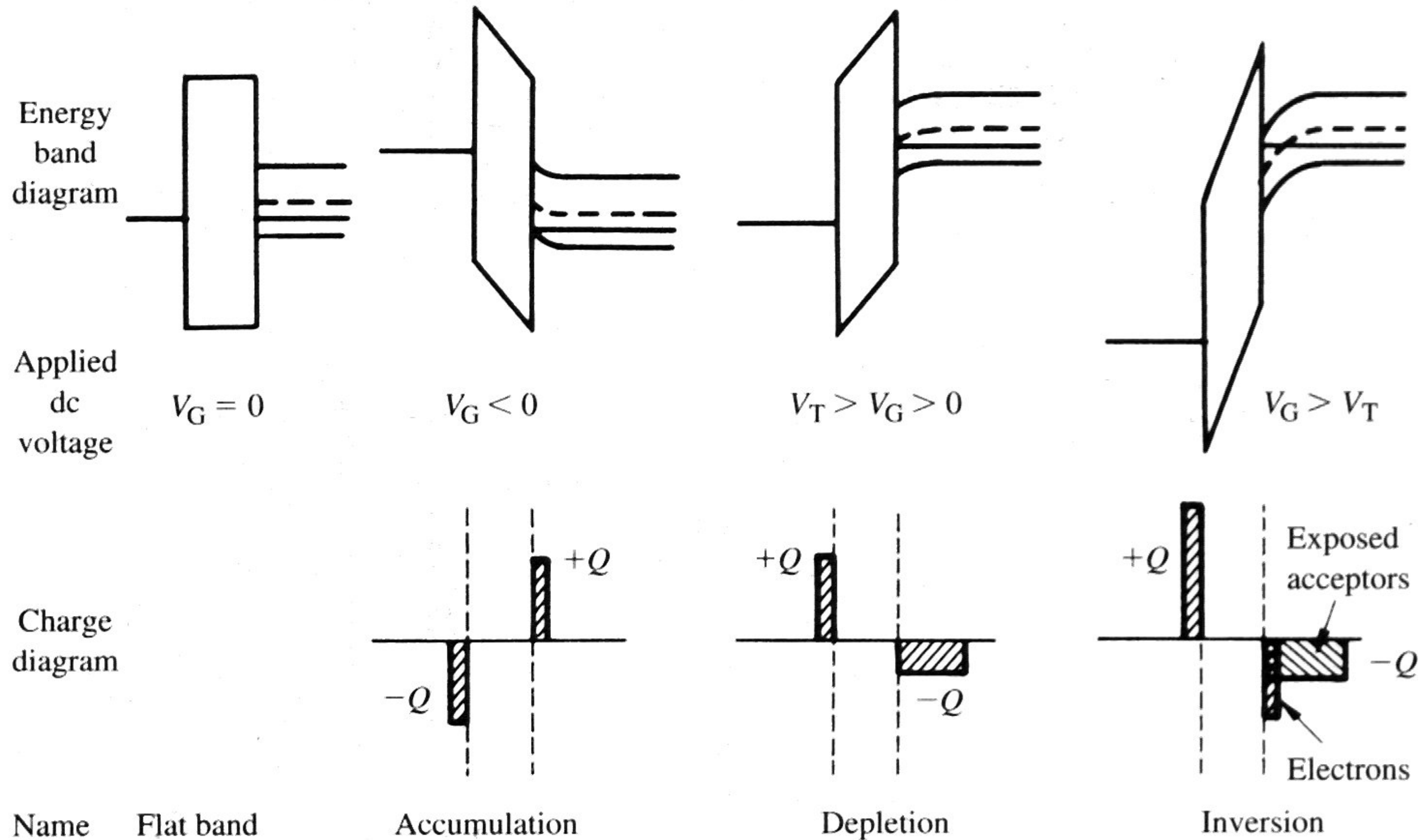
For an n-type semiconductor.

•For still higher magnitudes of bias ($V_G < 0$) the hole concentration continues to increase resulting in a very high concentration of holes near the interface.

•This is known as strong inversion.

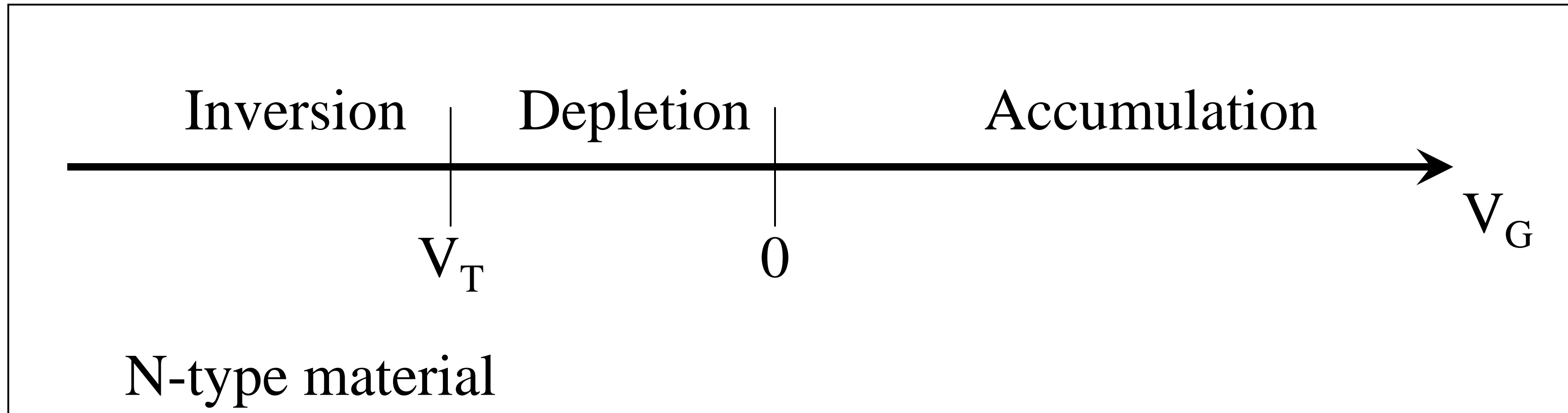
MOS Capacitor

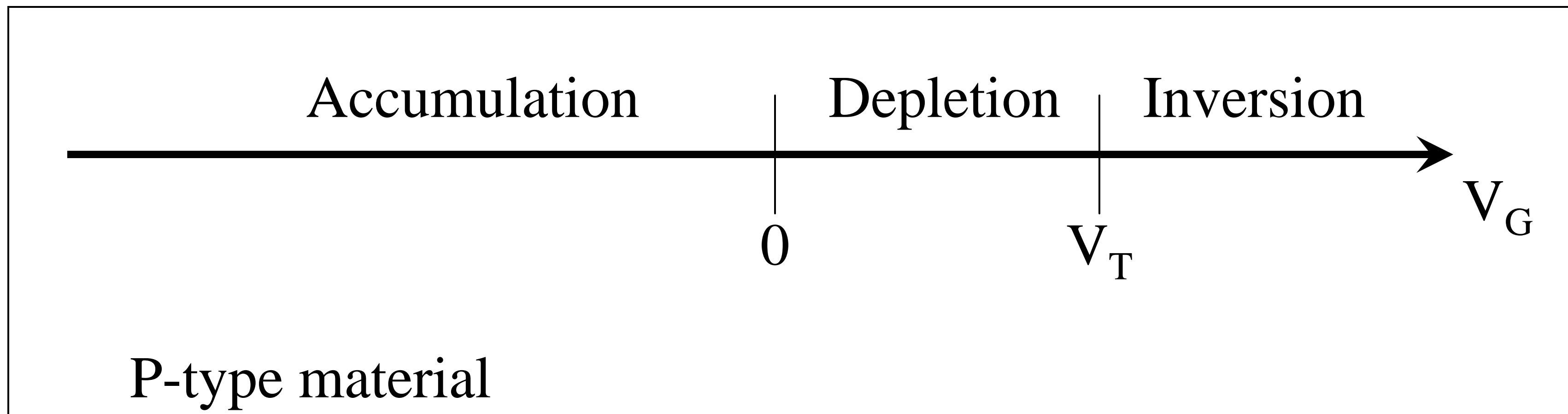
Capacitor under bias for P-type material



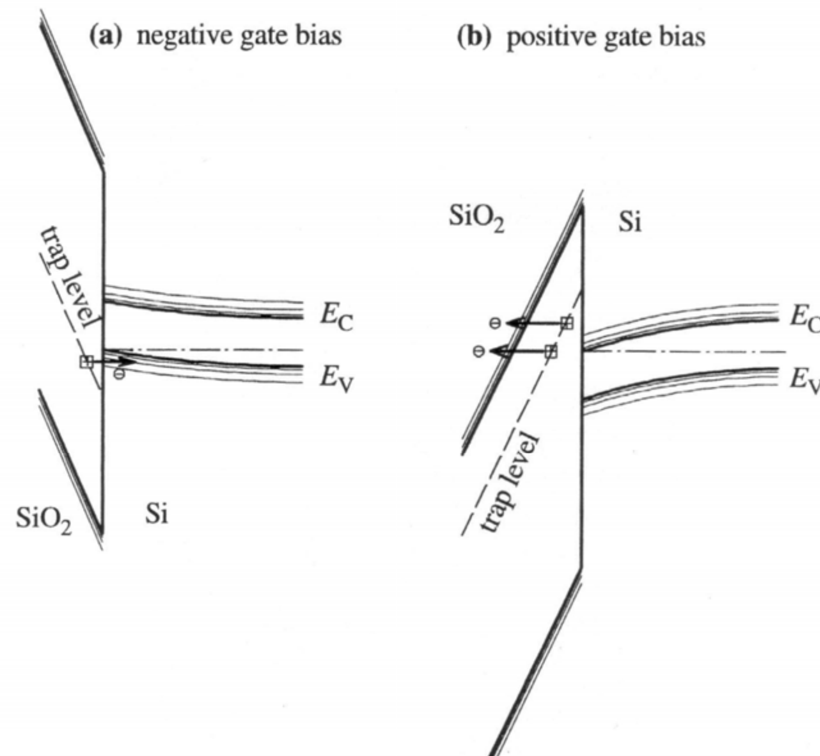
MOS Capacitor

Capacitor under bias Summary





Advanced Devices: Charge Storage
FLASH Memory Devices



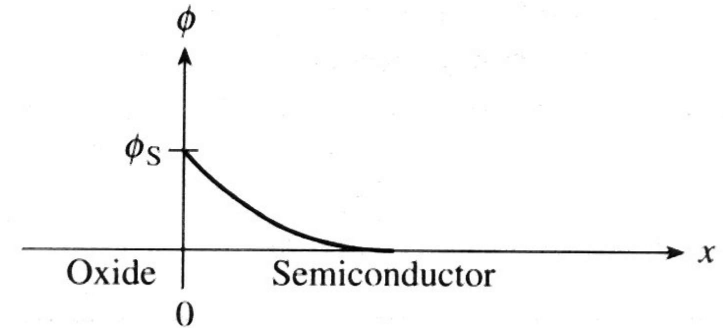
Either positive or negative charge can be stored in the oxide (often this is an Silicon oxy-nitride created to enhance trapped charge and allow higher leakage – two things normally considered bad in normal MOS structures).

The stored oxide charge looks to the semiconductor as if a static voltage exists on the gate. Implementing a "stored value" on the capacitor without the need for static voltage or power.

MOS Capacitor

Quantitative Solution

Let $\phi(x)$ = electrostatic potential inside the semiconductor at a depth x (measured from the oxide interface)



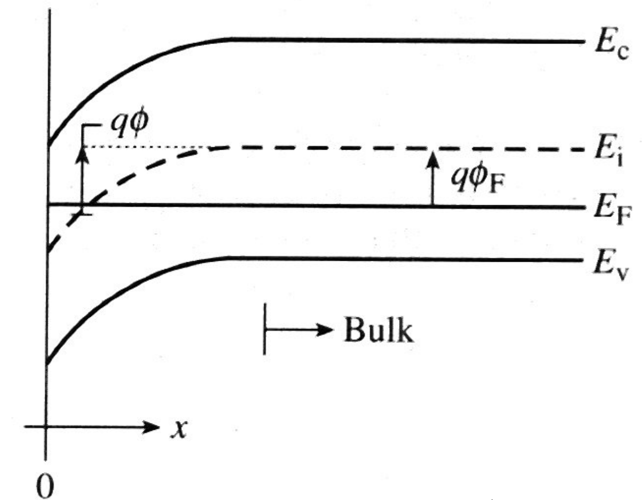
$$\phi(x) = \frac{1}{q}\left[E_{i-BULK} - E_i(x)\right] \equiv \text{electrostatic potential}$$

and

$$\phi_S = \frac{1}{q}\left[E_{i-BULK} - E_{i-INTERFACE}\right] \equiv \textit{surface potential}$$

along with,

$$\phi_F = \frac{1}{q}\left[E_{i-BULK} - E_F\right]$$



P-type Example

MOS Capacitor

Quantitative Solution

Since,

$$p_{BULK} = n_i e^{\left(E_{i-BULK} - E_F\right)/kT} = N_A \quad and \quad n_{BULK} = n_i e^{\left(E_F - E_{i-BULK}\right)/kT} = N_D$$

$$\phi_F = \begin{cases} \dfrac{kT}{q}\ln\left(\dfrac{N_A}{n_i}\right) & \text{for a p-type semiconductor} \\ -\dfrac{kT}{q}\ln\left(\dfrac{N_D}{n_i}\right) & \text{for a n-type semiconductor} \end{cases}$$

Thus,

$$\phi_S = 2\phi_F \quad \text{at the depletion-invertion transition point, } V_G = V_T$$

MOS Capacitor
Quantitative Solution

Since the MOS-Capacitor is symmetric (equal charge on metal as is in the semiconductor) and has no charge in the oxide, we can solve for the electrostatic variables using only the semiconductor section of material.

Things to note:

Charge due to accumulation bias and inversion bias results in a very narrow charge distribution near the interface.

Charge due to depletion bias results in a wide "depletion width", W

MOS Capacitor
Quantitative Solution

Once again, if we apply the "Depletion Region Approximation" (neglect all charges but those due to ionized dopants) and assume p-type material,

$$\rho = q\left(p - n + N_D - N_A\right) \cong -qN_A \quad \text{for } (0 \le x \le W) \quad \text{where W is the depletion width}$$

And from Poisson's equation using a boundary condition that the electric field goes to zero at the depletion region edge,

$$\frac{dE}{dx} = \frac{-qN_A}{K_S \varepsilon_o} \quad \Rightarrow \quad \boxed{E(x) = -\frac{d\phi}{dx} = \frac{qN_A}{K_S \varepsilon_o}\left(W - x\right)}$$

And finally, the electrostatic potential can be found by integrating using a boundary condition that the electrostatic potential goes to zero at the depletion region edge,

$$\boxed{\phi = \frac{qN_A}{2K_S \varepsilon_o}\left(W - x\right)^2}$$

MOS Capacitor
Quantitative Solution

The depletion width, W, can be found by noting that $\phi = \phi_S$ at x=0

$$W = \sqrt{\frac{K_S \varepsilon_o}{q N_A} \phi_S}$$

The depletion width at the inversion-depletion transition, W_T, can be found by noting that $2\phi_F = \phi_S$

$$W_T = \sqrt{\frac{K_S \varepsilon_o}{q N_A} 2\phi_F} = \sqrt{\frac{K_S \varepsilon_o 2kT}{q^2 N_A} \ln\left(\frac{N_A}{n_i}\right)}$$

NOTE: To obtain the equations for n-type substrates, we simply repeat the above procedure replacing N_A with $-N_D$

MOS Capacitor
Quantitative Solution

How is the gate voltage V_G distributed throughout the structure?

$$V_G = \phi_S + \phi_{oxide} \quad \text{(no drop in the metal)}$$

From before, we said,

$$\frac{dE_{oxide}}{dx} = \rho = 0 \quad \Rightarrow \quad E_{oxide} = Constant = -\frac{d\phi_{oxide}}{dx}$$

$$\phi_{oxide} = \int_{-x_{oxide\ thickness}}^{0} E_{oxide}\, dx = \left(x_{oxide\ thickness}\right) E_{oxide}$$

But, Gauss's Law states that the electric displacement,

$D = \varepsilon E$ must be continuous in the direction normal to the interface.

Thus,

$$\frac{E_{oxide}}{E_{Semiconductor\ at\ the\ Interface}} = \frac{K_S\, \varepsilon_o}{K_{ox}\, \varepsilon_o} = \frac{K_S}{K_{ox}}$$

where K_S and K_{ox} are the relative dielectric constants in the semiconductor and the oxide

Thus,

$$\phi_{oxide} = \frac{K_S}{K_{ox}}\left(x_{oxide\ thickness}\right)E_{Semiconductor\ at\ the\ Interface}$$

And using the previous expressions,

$$V_G = \phi_S + \frac{K_S}{K_{ox}}\left(x_{oxide\ thickness}\right)E_{Semiconductor\ at\ the\ Interface}$$

but using $W = \sqrt{\frac{K_S\varepsilon_o}{qN_A}\phi_S}$ *and* $E(x) = \frac{qN_A}{K_S\varepsilon_o}(W - x)$ at x = 0

$$E_{Semiconductor\ at\ the\ Interface} = \sqrt{\frac{2qN_A}{K_S\varepsilon_o}\phi_S}$$

Thus,

$$V_G = \phi_S + \frac{K_S}{K_{ox}}\left(x_{oxide\ thickness}\right)\sqrt{\frac{2qN_A}{K_S\varepsilon_o}\phi_S} \quad \text{for } 0 \le \phi_S \le 2\phi_F$$

Relates the applied gate voltage to the surface potential!

MOS Capacitor
Quantitative Solution

But what about in inversion and accumulation?

For inversion and accumulation we can not invoke the depletion approximation due to a significant amount of charge near the interface due to sources other than just ionized dopants (these charges are the electrons and holes).

In inversion and accumulation , the vast majority of the gate voltage is dropped across the oxide

In inversion, the depletion width remains ~ constant

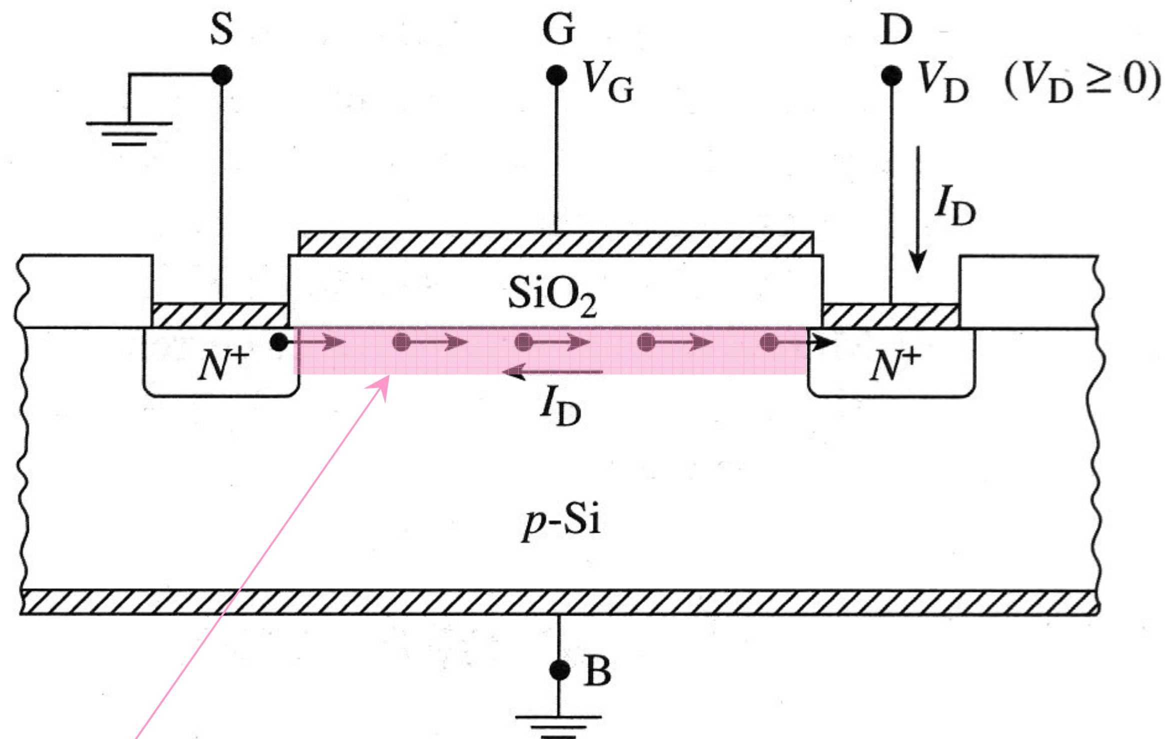
Thus, ϕ_S can not be much less (greater) than 0 for p-type (n-type)

Thus, ϕ_S can not be much greater (less) than $2\phi_F$ for p-type (n-type)

See discussion centered around figure 16.10 in Pierret if interested in more detail.

MOS Transistor
Qualitative Description

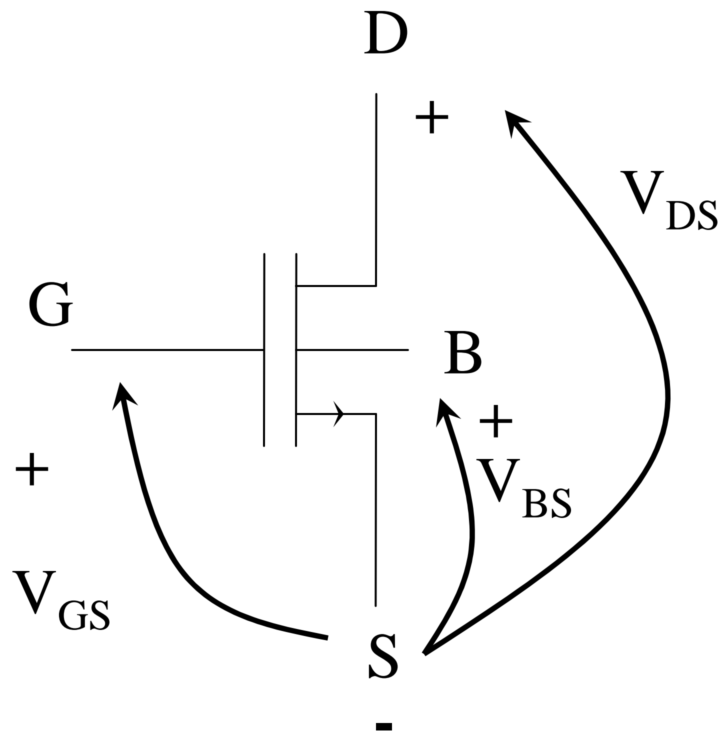
Flow of current from "Source" to "Drain" is controlled by the "Gate" voltage.



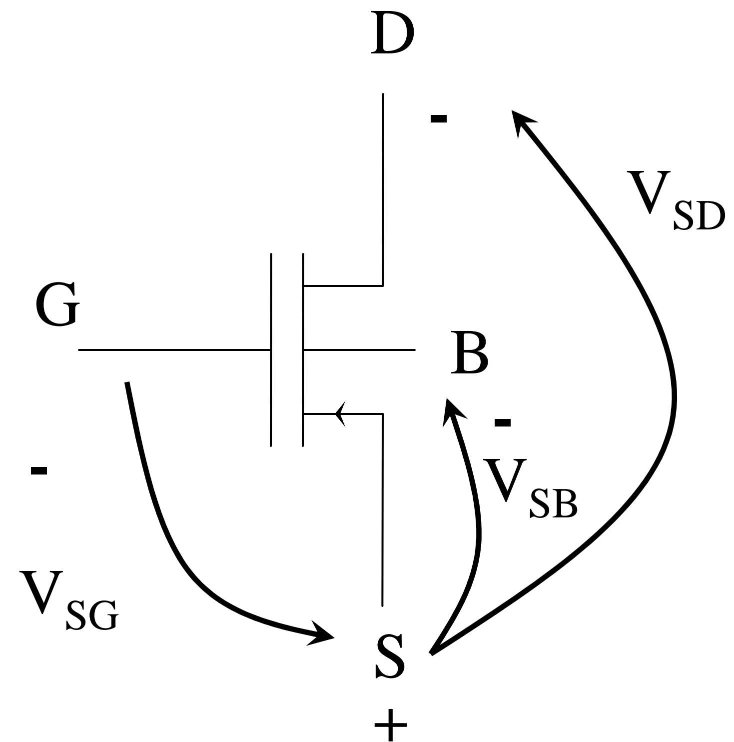
Control by the Gate voltage is achieved by modulating the conductivity of the semiconductor region just below the gate. This region is known as the channel

MOS Transistor
Qualitative Description

n-channel MOS Transistor



p-channel MOS Transistor



Note: All voltages are shown in their "positive " direction.
Obviously, V_{YX}=-V_{XY} for any voltage

G=Gate, D=Drain, S=Source, B=Body (substrate, but to avoid confusion with substrate, B is used)

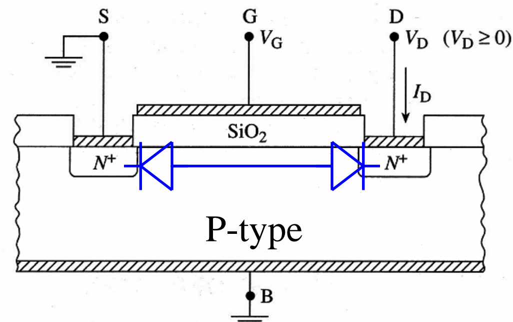
MOS Transistor

Qualitative Description

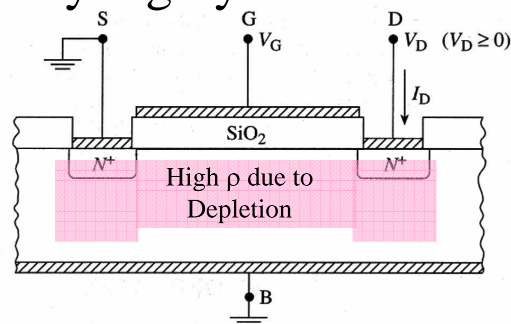
Assume an n-channel (receives it's name from the "type" of channel present when current is flowing) device with its source and substrate grounded (i. e., $V_S=V_B=0$ V).

For any value of V_{DS}:

- when V_{GS} <0 (accumulation), the source to drain path consists of two back to back diodes. One of these diodes is always reverse biased regardless of the drain voltage polarity.



- when V_{GS} <V_T (depletion), there is a deficit of electrons and holes making the channel very highly resistive. => No Drain current can flow.

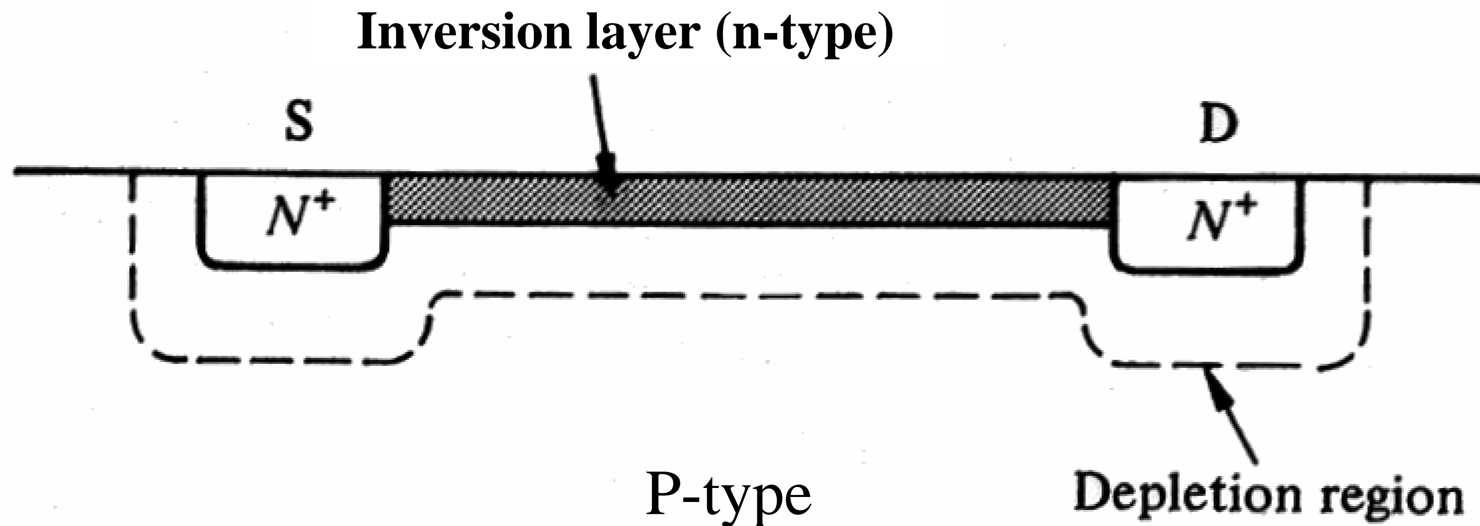


MOS Transistor
Qualitative Description

Consider now the Inversion case:

First, $V_{DS} = 0$:

- when $V_{GS} > V_T$, an induced n- type region, an "inversion layer", forms in the channel and "electrically connects" the source and drain.

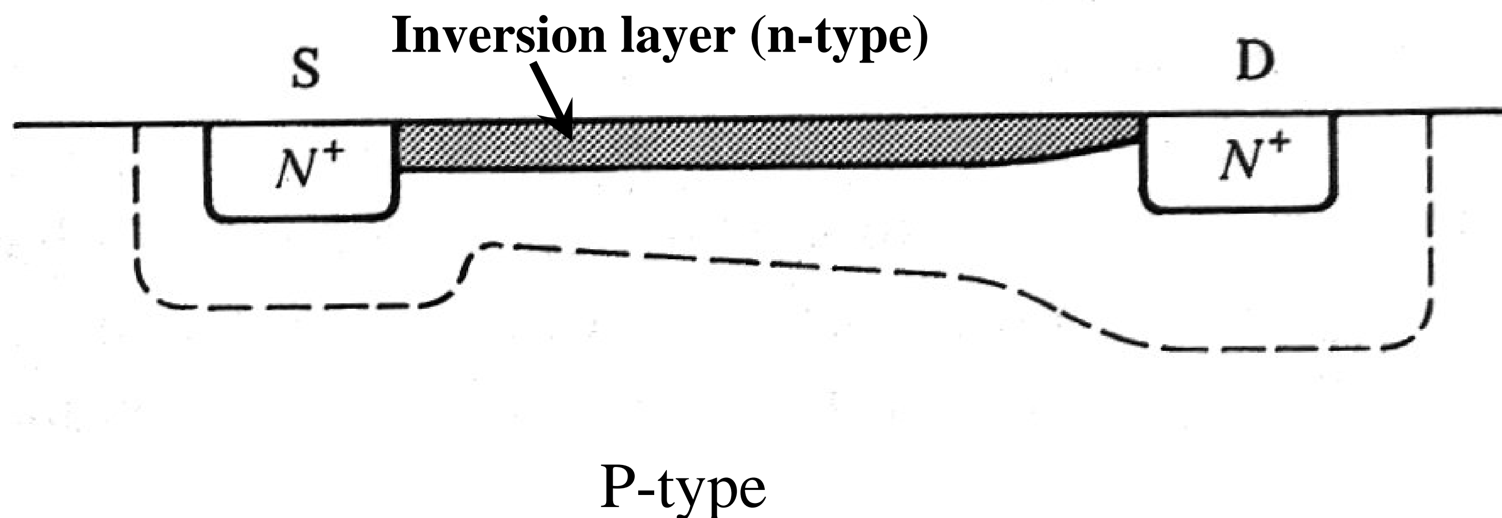


MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

When $V_{DS} > 0$, the induced n- type region allows current to flow between the source and drain. The induced channel ast like a simple resistor. Thus, this current, I_D, depends linearly on the Drain voltage V_D. This mode of operation is called the linear or "triode"* region.



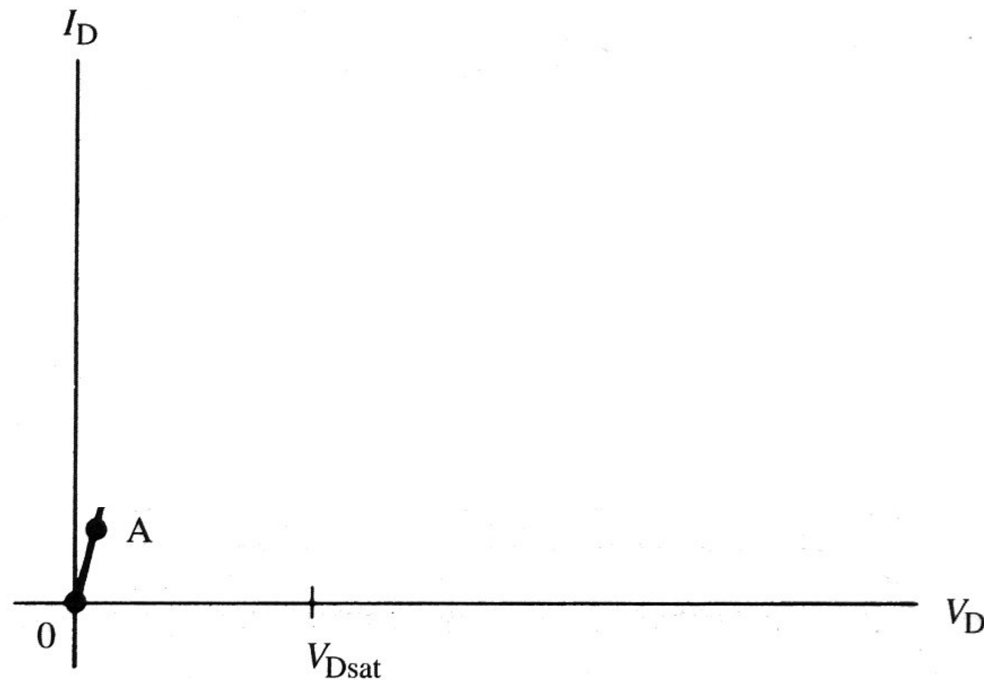
P-type

* "Triode" is a historical term from vacuum tube technology.

MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

Drain current verses drain voltage when in the linear or "triode"* region.



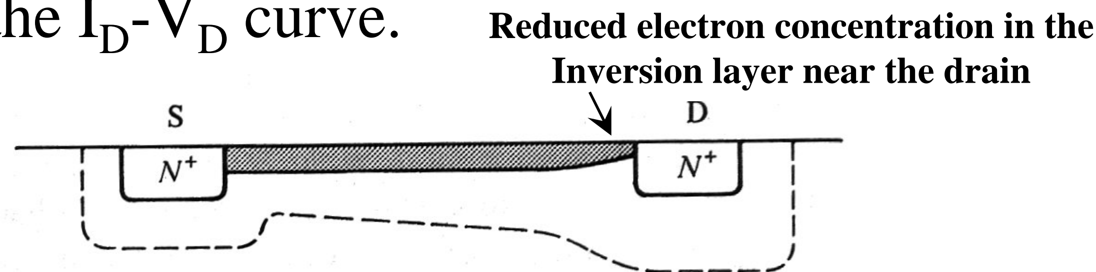
MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

When V_{DS} increases a few tenths of a volt (>0):

- The depletion region near the drain widens (N+ drain is positively biased – I.e. reverse biased with respect to the substrate).
- The electron concentration in the inversion layer near the drain decreases as they are "sucked out" by the Drain voltage.
- Channel conductance decreases resulting in a drop in the slope of the I_D-V_D curve.

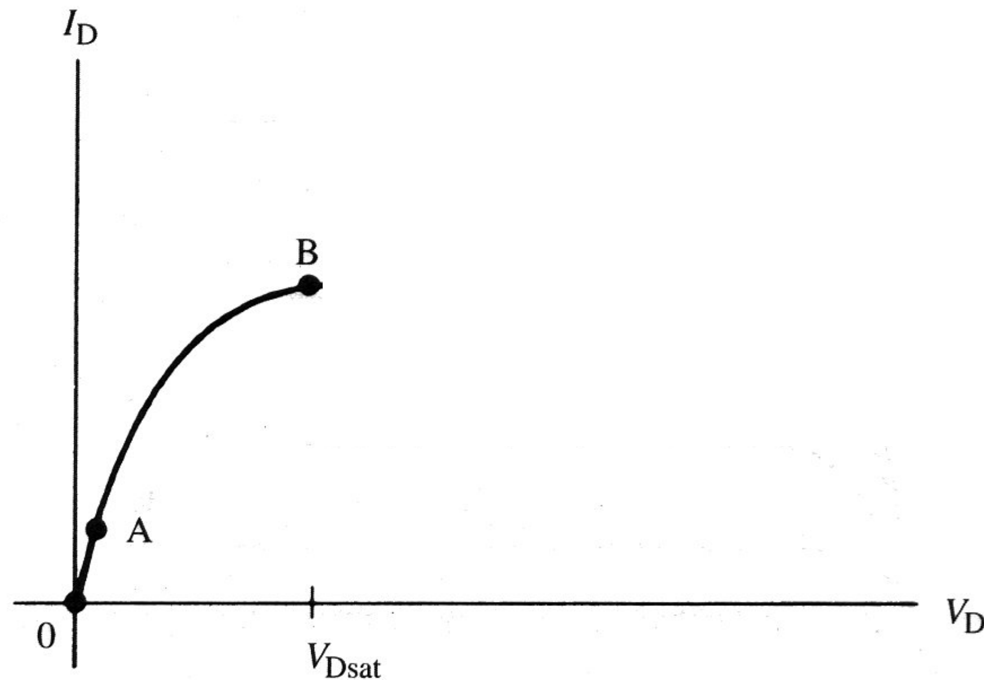


P-type

MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

Drain current verses drain voltage for increasing V_{DS} (still in the "linear" or triode region).



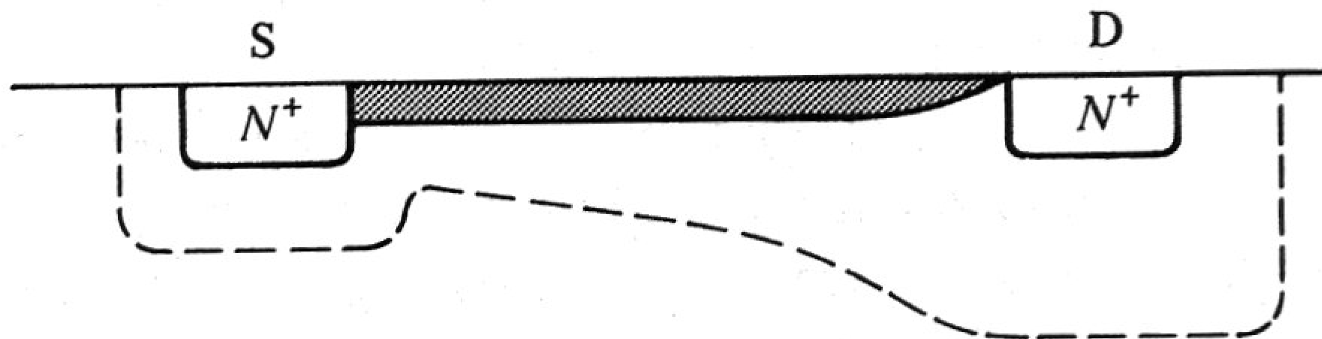
MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T(continued)}$:

The inversion layer eventually vanishes near the drain end of the channel.

This is called "Pinch-Off" and results in a Flat I_D-V_{DS} curve

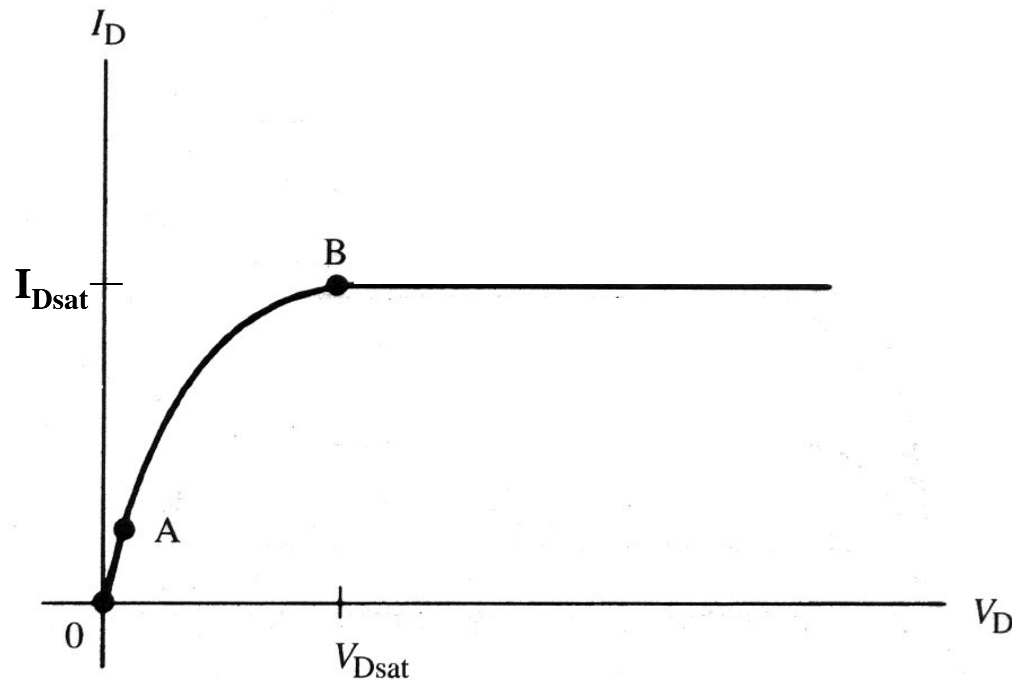


MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

I_D-V_{DS} curve for the "Saturation Region"

The drain-source voltage, V_{DS}, at which this occurs is called the saturation voltage, V_{sat} while the current is called the saturation current, I_{Dsat}.

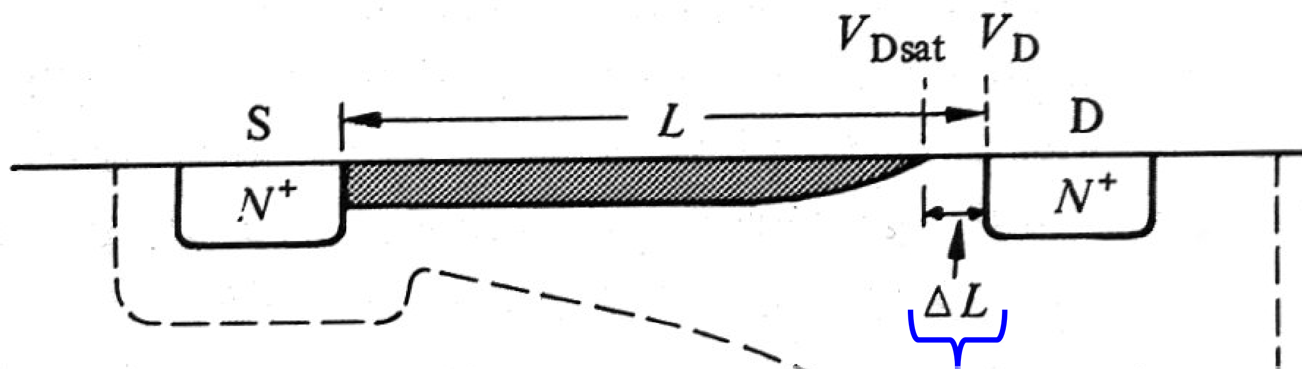


MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T(continued)}$:

For $V_{DS}>V_{sat}$ the channel length, L, effectively changes by a value ΔL.

The region of the channel, ΔL is depleted and thus, is high resistivity. Accordingly, almost all voltage increases in $V_{DS}>V_{sat}$ are "dropped across" this portion of the channel.



High electric fields in this region act similarly to the collector-base junction in a BJT in active mode, "stripping" or "collecting" carriers from the channel.

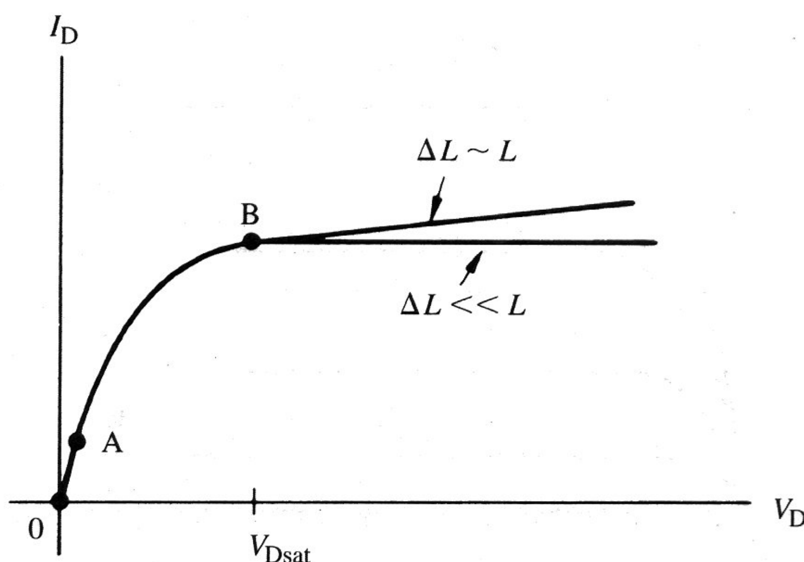
MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T(continued)}$:

If $\Delta L << L$, the voltage at the end of the channel will be constant (V_{sat}) for all $V_{DS} > V_{sat}$. I_D will be constant.

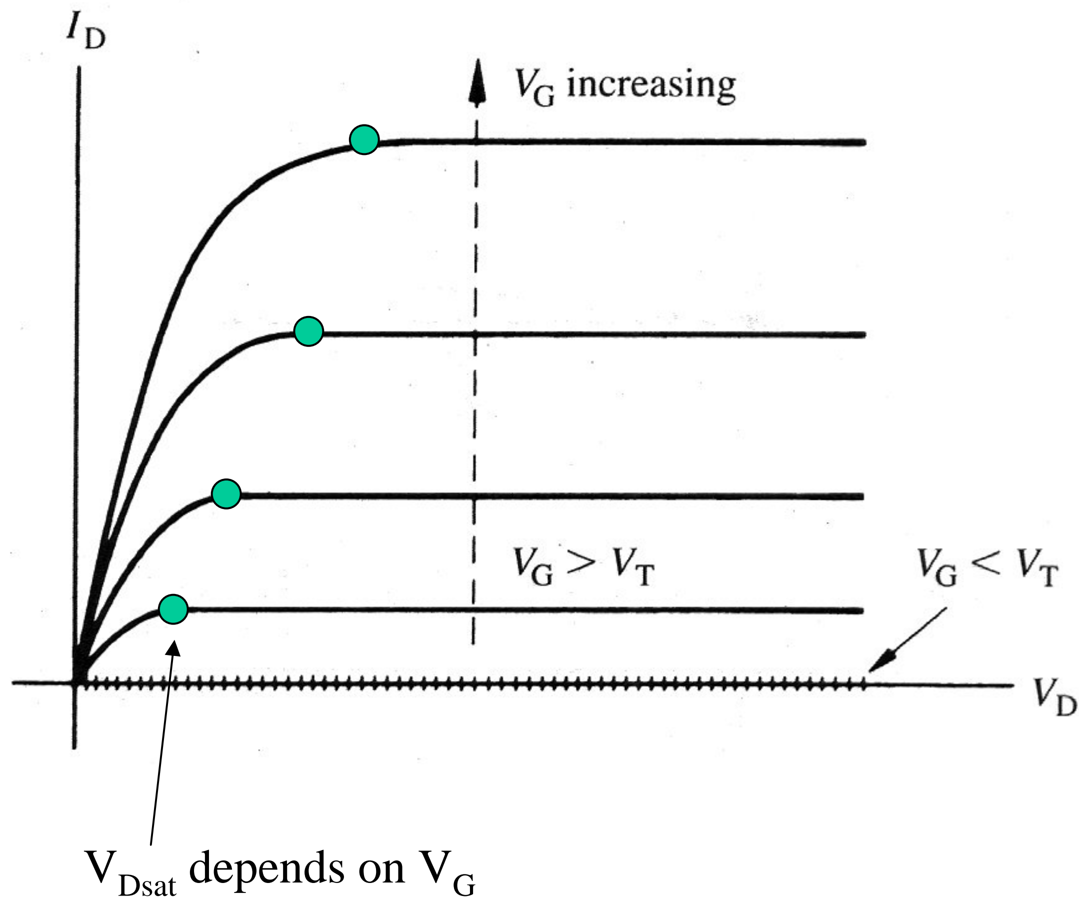
If $\Delta L \sim L$, the voltage dropped across the the channel (V_{SAT}) varies greatly with V_{DS} due to large modulations in the electric field across the pinched off region ($E=[V_{DS}-V_{SAT}]/[\Delta L]$). In this case, I_D increases slightly with V_{DS}.



MOS Transistor
Qualitative Description

Finally,

I_D-V_{DS} curves for various V_{GS}:



MOS Transistor I-V Derivation

With our expression relating the Gate voltage to the surface potential and the fact that $\phi_S=2\phi_F$ we can determine the value of the threshold voltage

$$V_T = 2\phi_F + \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_S}(2\phi_F)} \quad \text{(for n - channel devices)}$$

$$V_T = 2\phi_F - \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_D}{\varepsilon_S}(-2\phi_F)} \quad \text{(for p - channel devices)}$$

where,

$$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}} \quad \text{is the oxide capacitance per unit area}$$

Where we have made use of the use of the expression,

$$\varepsilon_S = K_S \varepsilon_o$$

MOS Transistor I-V Derivation

Coordinate Definitions for our "NMOS" Transistor

x=depth into the semiconductor from the oxide interface.

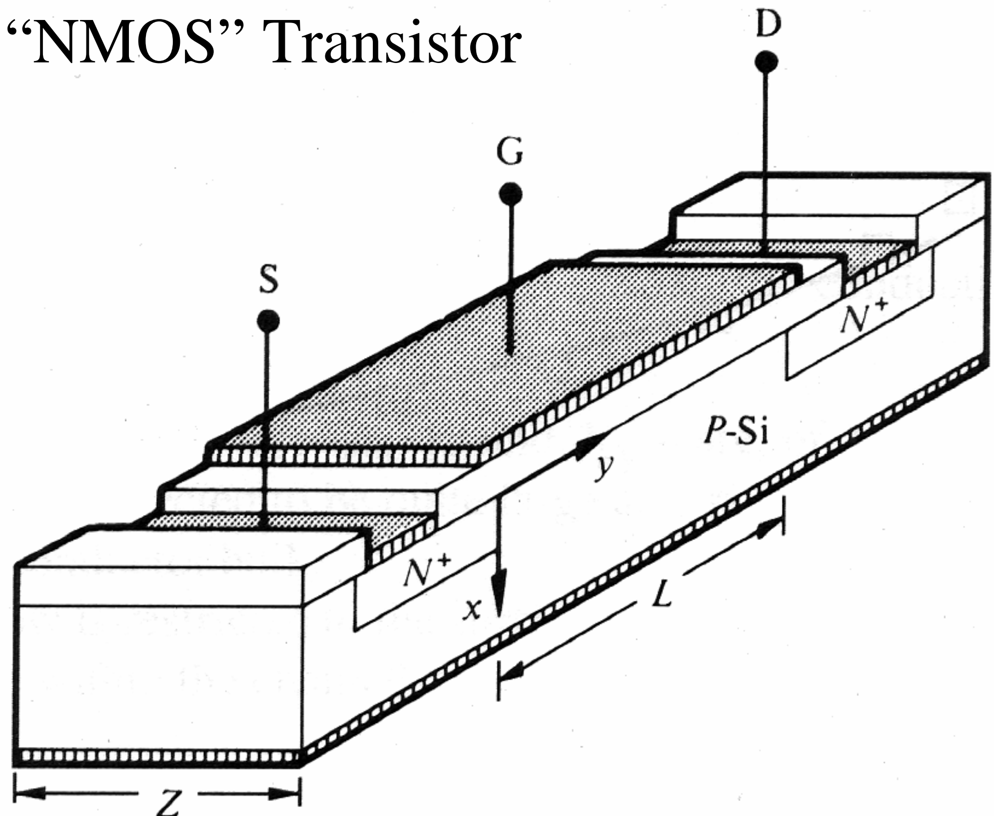
y=length along the channel from the source contact

z=width of the channel

$x_c(y)$ = channel depth (varies along the length of the channel).

n(x,y)= electron concentration at point (x,y)

μ_n(x,y)=the mobility of the carriers at point (x,y)



Device width is Z

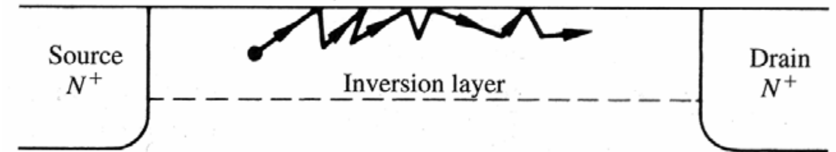
Channel Length is L

Assume a "Long Channel" device (for now do not worry about the channel length modulation effect)

MOS Transistor I-V Derivation

Concept of Effective mobility

The mobility of carriers near the interface is significantly lower than carriers in the semiconductor bulk due to interface scattering.



Since the electron concentration also varies with position, the average mobility of electrons in the channel, known as the effective mobility, can be calculated by a weighted average,

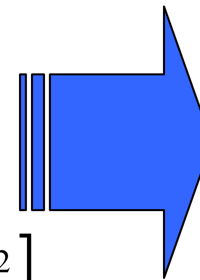
$$\overline{\mu_n} = \frac{\int_{x=0}^{x=x_c(y)} \mu_n(x,y)n(x,y)dx}{\int_{x=0}^{x=x_c(y)} n(x,y)dx}$$

or defining,

$$Q_N(y) = -q\int_{x=0}^{x=x_c(y)} n(x,y)dx \quad [charge/cm^2]$$

$$\overline{\mu_n} = \frac{-q}{Q_N(y)}\int_{x=0}^{x=x_c(y)} \mu_n(x,y)n(x,y)dx$$

Empirically



$$\overline{\mu_n} = \frac{\mu_o}{1+\theta\left(V_{GS}-V_T\right)}$$

where, μ_o *and* θ are constants

Drain Current-Voltage Relationship

In the Linear Region, $V_{GS}>V_T$ and $0<V_{DS}<V_{dsat}$

$$J_N = q\mu_n nE + qD_N \nabla n$$

Neglecting the diffusion current, and recognizing the current is only in the y-direction,

$$J_N \cong J_{Ny} \cong q\mu_n nE_y \cong -q\mu_n n \frac{d\phi}{dy}$$

Drain Current-Voltage Relationship

In the Linear Region, $V_{GS}>V_T$ and $0<V_{DS}<V_{dsat}$

$$I_D = -\int\int J_{Ny}\,dx\,dz = Z\int_{x=0}^{x=x_c(y)} J_{Ny}\,dx$$

$$= \left(-Z\frac{d\phi}{dy}\right)\left(-q\int_{x=0}^{x=x_c(y)} \mu_n(x,y)n(x,y)\,dx\right)$$

$$= -Z\overline{\mu_n}Q_N\frac{d\phi}{dy}$$

$$\int_{y=0}^{y=L} I_D\,dy = -Z\overline{\mu_n}\int_{\phi=0}^{\phi=V_{DS}} Q_N\,d\phi$$

$$I_D L = -Z\overline{\mu_n}\int_{\phi=0}^{\phi=V_{DS}} Q_N\,d\phi$$

$$I_D = \frac{-Z\overline{\mu_n}}{L}\int_{\phi=0}^{\phi=V_{DS}} Q_N\,d\phi$$

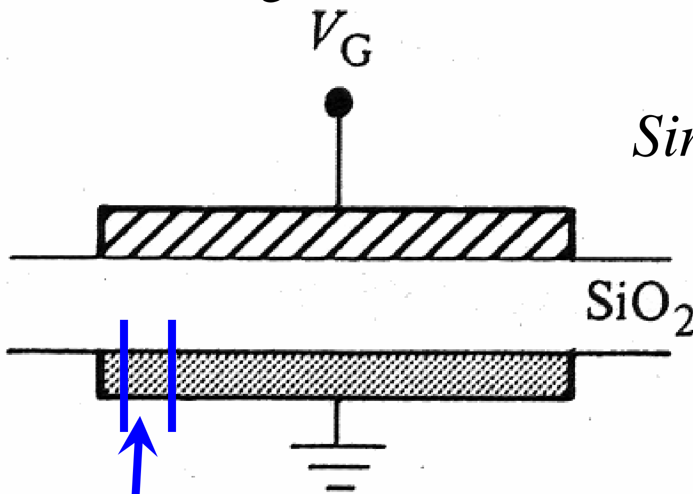
To find I_D, we need an expression relating ϕ and Q_N

"Capacitor-Like" Model for Q_N

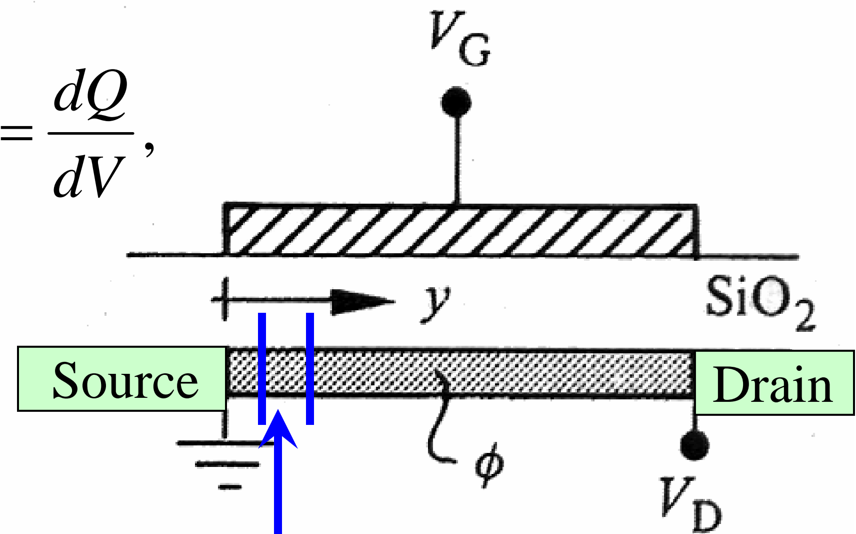
Assumptions:

•Neglect all but the mobile inversion charge

•For the MOSFET, the charge in the semiconductor is a linear function of position along the semiconductor side of the plate. Thus, ϕ varies from 0 to V_{DS}



$$Since \quad C_{ox} = \frac{dQ}{dV},$$



MOS Capacitor

Only voltages above threshold create inversion charge

$$Q_N \cong -C_{ox}(V_{GS} - V_T) \quad \text{for } V_{GS} \geq V_T$$

Neglect the depletion region charge

MOS Transistor

$$Q_N \cong -C_{ox}(V_{GS} - V_T - \phi)$$

for $V_{GS} \geq V_T$

Note: Assuming a linear variation of potential along the channel leads to an underestimation of current but is a good estimate for hand calculations.

MOS Transistor I-V Derivation

Using "Capacitor-Like" Model for Q_N we can estimate I_D as:

$$I_D = \frac{-Z\overline{\mu_n}}{L}\int_{\phi=0}^{\phi=V_{DS}} Q_N \, d\phi$$

$$I_D = \frac{-Z\overline{\mu_n}}{L}\int_{\phi=0}^{\phi=V_{DS}} -C_{ox}\left(V_G - V_T - \phi\right) d\phi$$

$$I_D = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad 0 \le V_{DS} \le V_{Dsat} \quad and \quad V_{GS} \ge V_T$$

This is known as the "square law" describing the Current-Voltage characteristics in the "Linear" or "Triode" region.

Note the linear behavior for small V_{DS} (can neglect V_{DS}^2 term). Note the negative parabolic dependence for larger V_{DS} but still $V_{DS}<V_{Dsat}$ (can NOT neglect V_{DS}^2 term).

"Capacitor-Like" Model for Q_N

But what about the saturation region?

For $V_{DS}>V_{dsat}$ the voltage drop across our channel is V_{Dsat} with the remaining voltage ($V_{DS}-V_{Dsat}$) dropped across the pinch-off region

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS}-V_T)V_{Dsat} - \frac{V_{Dsat}^2}{2}\right] \qquad V_{Dsat} \le V_{DS}$$

But the charge at the end of the channel is zero due to the pinched off channel,

$$Q_N(y=L) \cong -C_{ox}(V_{GS}-V_T-V_{Dsat}) = 0$$

$$or$$

$$\boxed{V_{GS}-V_T = V_{Dsat}}$$

Thus,

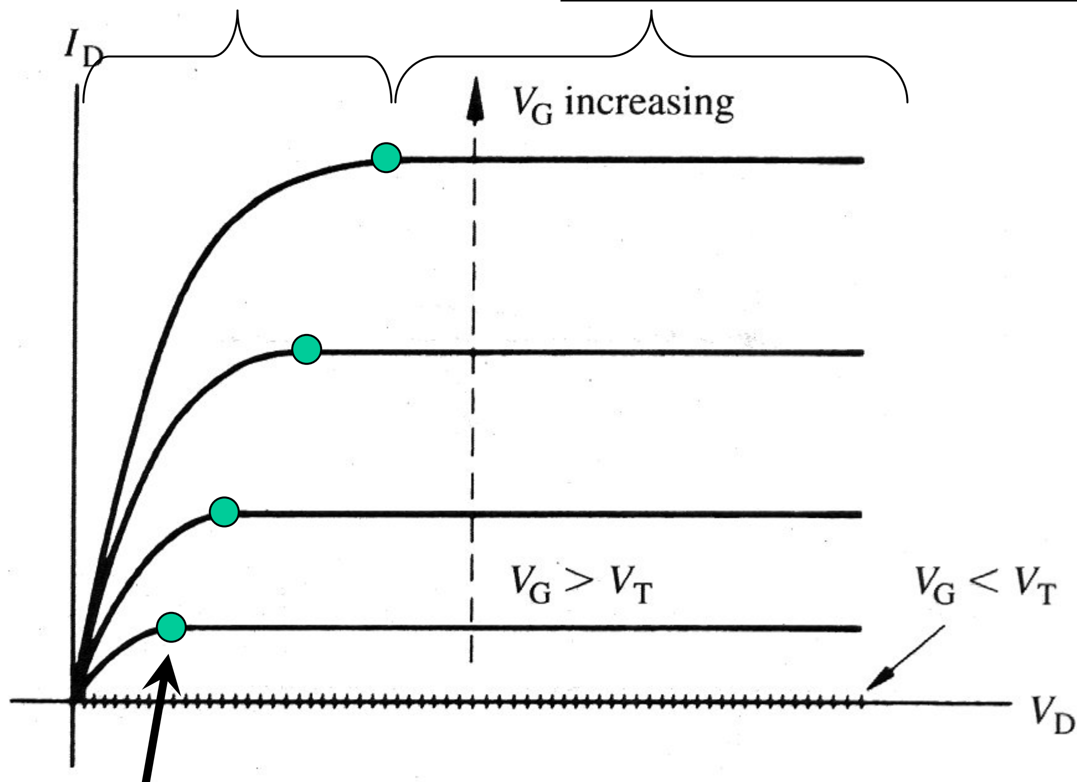
$$\boxed{I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS}-V_T)^2\right] \qquad V_{Dsat} \le V_{DS}}$$

MOS Transistor I-V Derivation
Summary of MOSFET IV Relationship

$$I_D = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

$$0 \le V_{DS} \le V_{Dsat} \quad and \quad V_{GS} \ge V_T$$

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS}-V_T)^2\right] \qquad V_{Dsat} \le V_{DS}$$

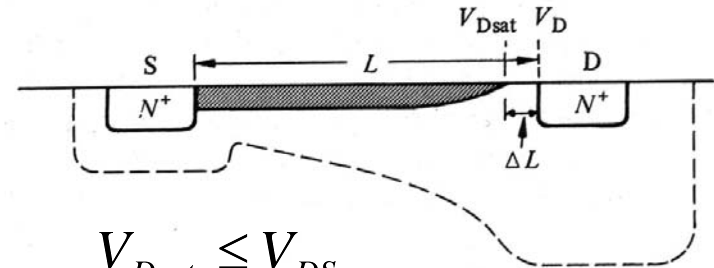


$$V_{Dsat} = V_{GS} - V_T$$

MOS Transistor: Deviations From Ideal

Channel Length Modulation Effect

Above "pinch-off" (when $V_{DS}>V_{Dsat}=V_{GS}-V_T$) the channel length reduces by a value ΔL.



Thus, the expression for drain current,

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS}-V_T)^2\right] \qquad V_{Dsat} \le V_{DS}$$

Becomes,

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2(L-\Delta L)}\left[(V_{GS}-V_T)^2\right] \qquad V_{Dsat} \le V_{DS}$$

$$\text{or since* } \Delta L \langle\langle L, \quad \frac{1}{L-\Delta L} \cong \frac{1}{L}\left(1+\frac{\Delta L}{L}\right)$$

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS}-V_T)^2\right]\left(1+\frac{\Delta L}{L}\right) \qquad V_{Dsat} \le V_{DS}$$

*In many modern devices, this assumption does not hold. Thus, the channel length modulation parameter we are deriving does not describe the IV expressions well.

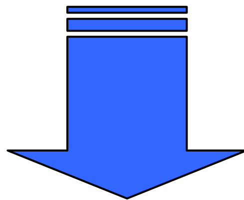
MOS Transistor: Deviations From Ideal

Channel Length Modulation Effect

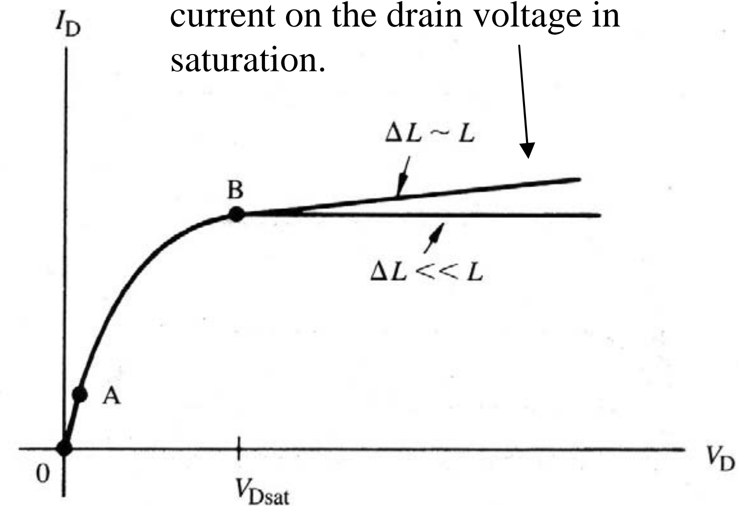
But the fraction of the channel that is pinched off depends linearly on V_{DS} because the voltage across the pinch-off region is (V_{DS}-V_{Dsat}) so,

$$\frac{\Delta L}{L} = \lambda V_{DS}$$

where λ is known as the ***Channel-Length Modulation parameter*** and is typically: $0.001\ V^{-1} < \lambda < 0.1\ V^{-1}$



Channel Length Modulation causes the dependence of drain current on the drain voltage in saturation.

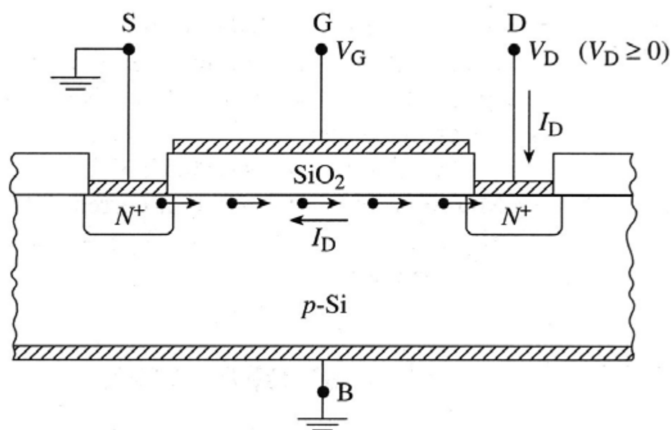


$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS} - V_T)^2\right](1 + \lambda V_{DS}) \qquad V_{Dsat} \le V_{DS}$$

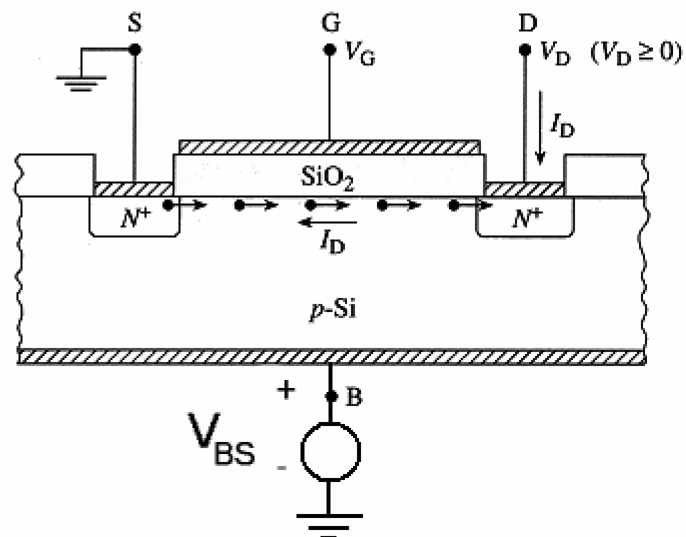
MOS Transistor: Deviations From Ideal

Body Effect (Substrate Biasing)

Until now, we have only considered the case where the substrate (Body) has been grounded….



…but the substrate (Body) is often intentionally biased such that the Source-Body and Drain-Body junctions are reversed biased.



The body bias, V_{BS}, is known as the ***backgate bias*** and can be used to modify the threshold voltage.

Note that now our channel potential has an offset equal to V_{BS}, ….

MOS Transistor:

Enhancement Mode verses Depletion Mode MOSFET

We have been studying the "enhancement mode" MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor). It is called "enhancement" because conduction occurs only after the channel conductance is "improved" or "enhanced". In this case,

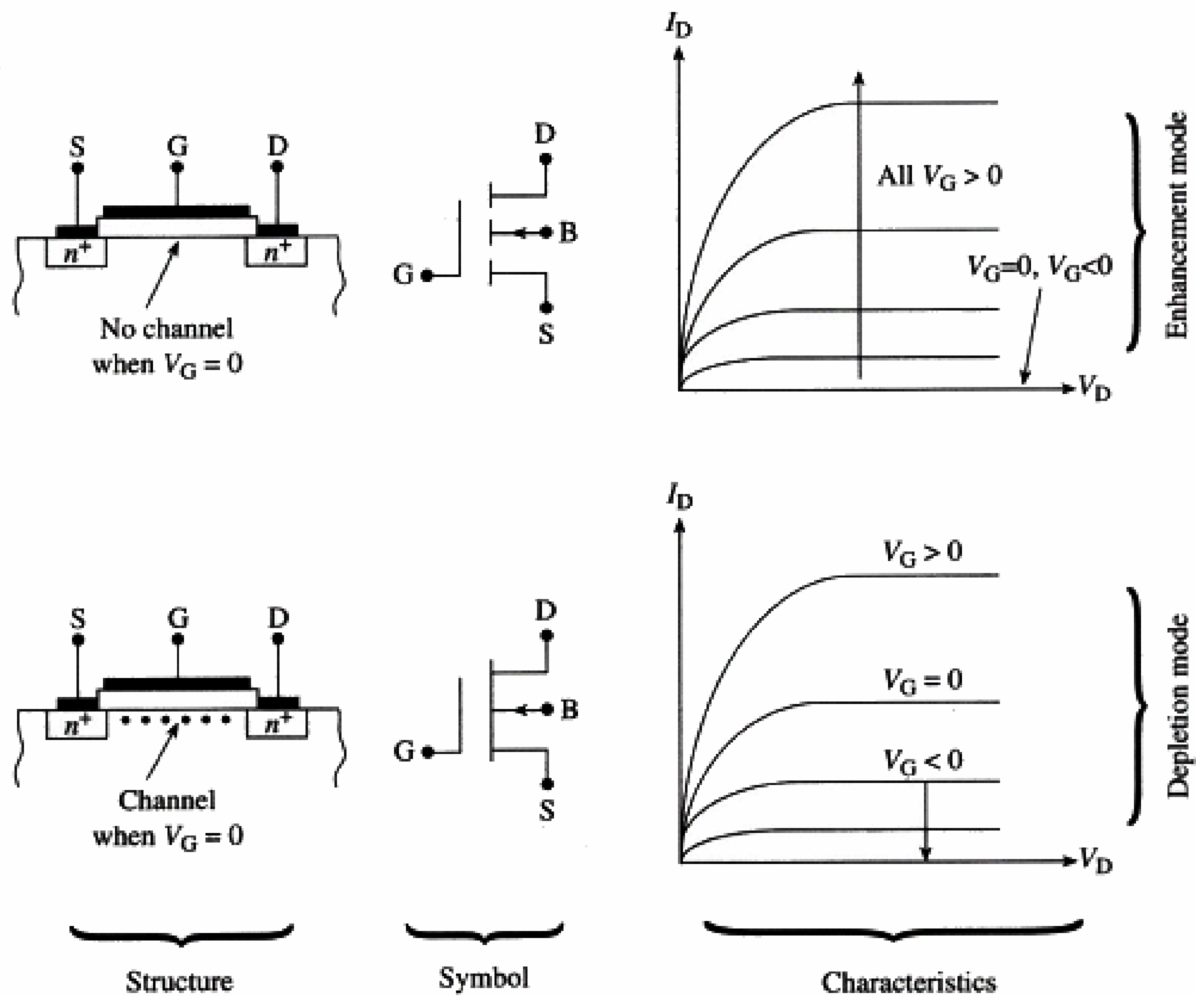
$V_{TN}>0$ and $V_{TP}<0$

Transistors can be fabricated such that: $V_{TN} \leq 0$ and $V_{TP} \geq 0$

These transistors have conduction for $V_{GS}=0$ due to a channel already existing without the need to "invert the near surface region". To modulate currents, a field must applied to the gate that depletes the channel. Thus, transistors of this nature are called "Depletion mode MOSFETs".

MOS Transistor:

Enhancement Mode verses Depletion Mode MOSFET



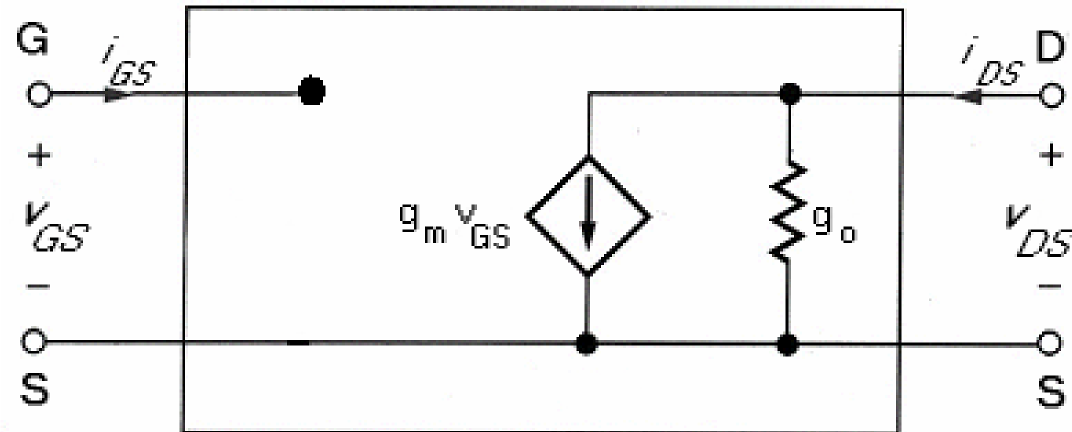
MOSFET operational modes. $V_G = 0$ channel status, circuit symbol, and I_D–V_D characteristics of n-channel enhancement-mode and depletion-mode MOSFETs.

MOS Transistor: Summary

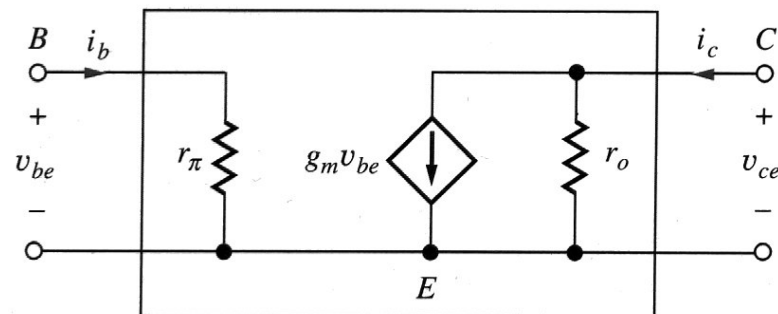
	NMOS	PMOS
Regardless of Mode	$K_n = K_n^{'} \frac{W}{L} = \overline{\mu_n}\, C_{ox} \frac{W}{L}$ (Note : W = Z in Pierret)	$K_p = K_p^{'} \frac{W}{L} = \overline{\mu_n}\, C_{ox} \frac{W}{L}$ (Note : W = Z in Pierret)
Cutoff	$i_{DS} = 0 \quad for\ v_{GS} \le V_{TN}$	$i_{DS} = 0 \quad for\ v_{SG} \le -V_{TP}$
Linear	$i_{DS} = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(v_{GS} - V_{TN})v_{DS} - \frac{v_{DS}^2}{2}\right]$ $v_{GS} - V_{TN} \ge v_{DS} \ge 0$	$i_{SD} = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(v_{SG} - V_{TP})v_{SD} - \frac{v_{SD}^2}{2}\right]$ $v_{SG} + V_{TP} \ge v_{SD} \ge 0$
Saturation	$i_{DS} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(v_{GS} - V_{TN})^2\right](1 + \lambda\ v_{DS})$ $for \quad v_{DS} \ge v_{GS} - V_{TN} \ge 0$	$i_{DS} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(v_{SG} + V_{TP})^2\right](1 + \lambda\ v_{SD})$ $for \quad v_{SD} \ge v_{SG} + V_{TP} \ge 0$
Threshold Voltage	$V_{TN} = V_{TO} + \gamma\left(\sqrt{(2\phi_F - v_{BS})} - \sqrt{2\phi_F}\right)$	$V_{TP} = V_{TO} - \gamma\left(\sqrt{(2\phi_F + v_{BS})} - \sqrt{2\phi_F}\right)$
V_T for Enhancement Mode	$V_{TN} > 0$	$V_{TP} < 0$
V_T for Depletion Mode	$V_{TN} \le 0$	$V_{TP} \ge 0$

MOSFET Small Signal Model and Analysis

Putting the mathematical model into a small signal equivalent circuit

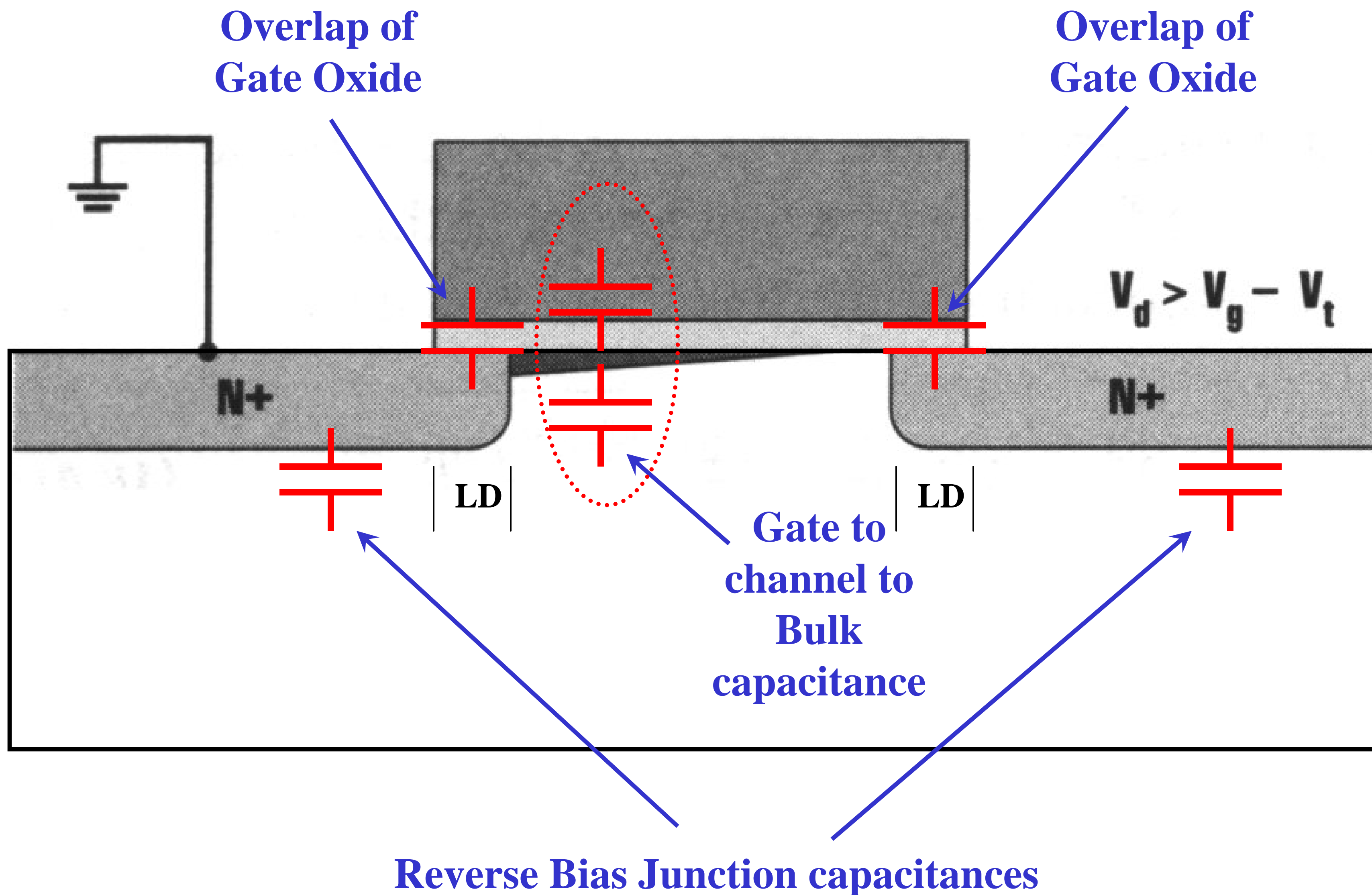


Compare this to the BJT small signal equivalent circuit



MOSFET Small Signal Model and Analysis

Add in capacitances



MOSFET Small Signal Model and Analysis

Complete Model of a MOSFET