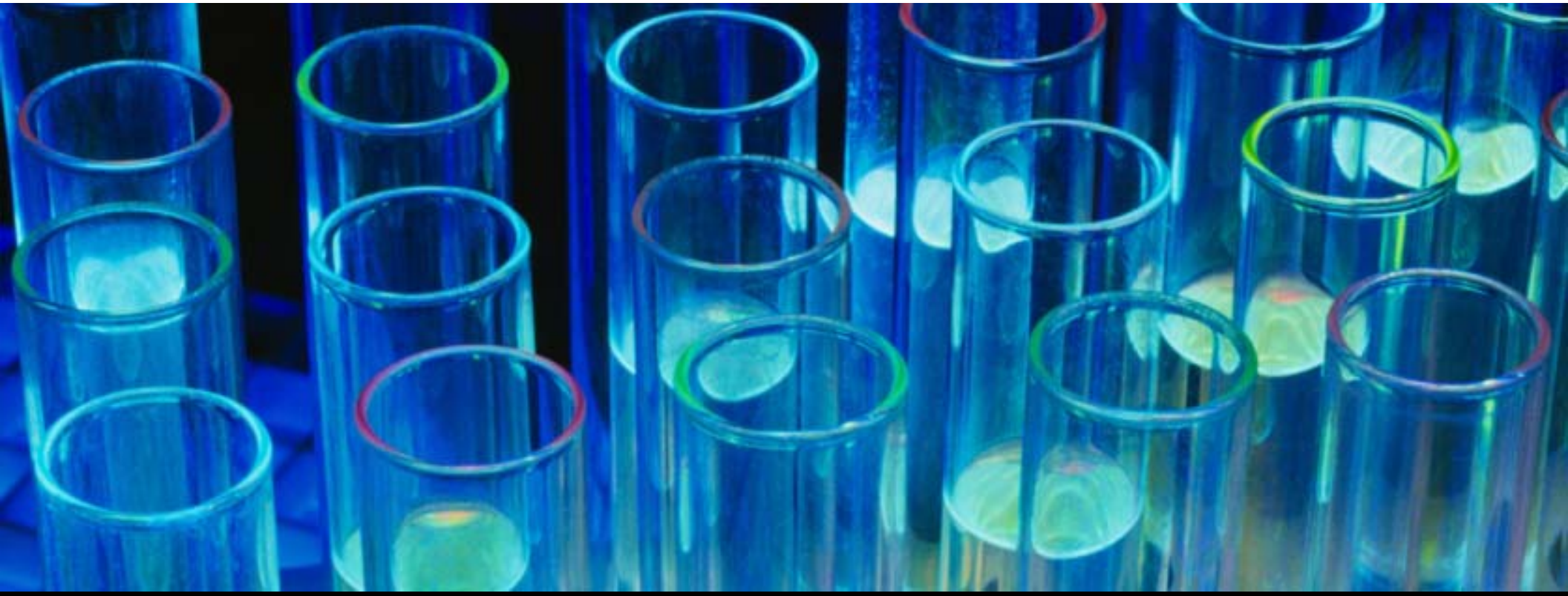

Power MOSFETs

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Introduction

- Power MOSFETs were first developed in the late 1970's, first one was created by International Rectifier in 1978.
- They are majority carrier devices with no minority carrier injection, superior to Power Bipolar Junction Transistor (BJTs) and Insulated Gate Bipolar Transistors (IGBTs) in high frequency applications where switching power losses are dominant.

Overview

- Basic Device Structure
- Breakdown Voltage
- On-state Characteristic
- Capacitance,
- Gate charge, Gate Resistance
- Power Dissipation
- Package Limitation

Basic Device Structure

- Most power MOSFETs features a vertical structure with Source and Drain on opposite sides of the wafer in order to support higher current and voltage. On the next slide there is a figure of simplified vertical Power MOSFET with four layer of n+pn-n+ structure which is defined as N-Channel Enhancement-Mode Power MOSFET.
- Below is the figure which shows the basic device structures of Trench and Planar MOSFETs.

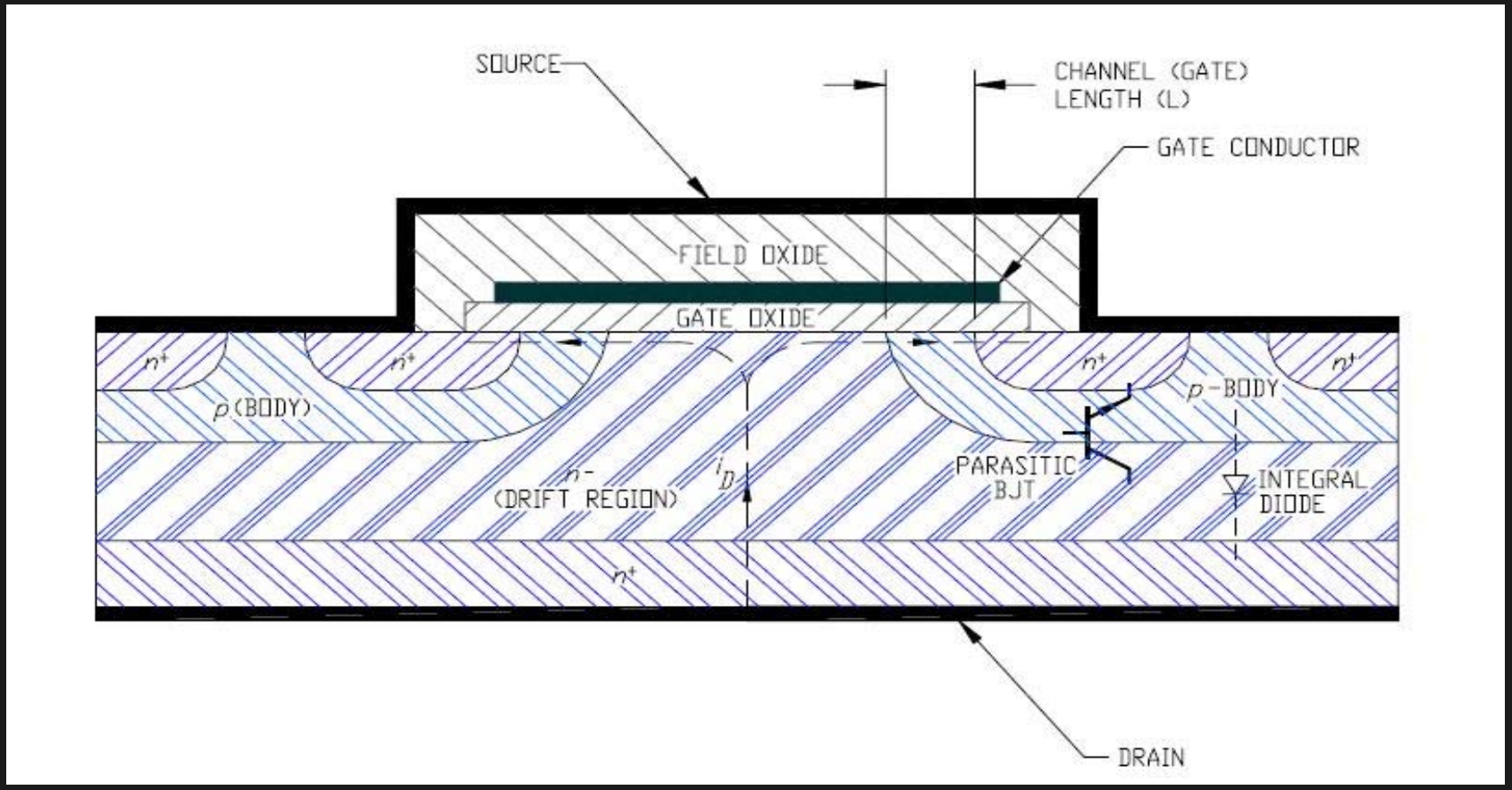

Figure [1]. N-Channel Enhancement-Mode Power MOSFET Structure

Trench MOSFET Structure

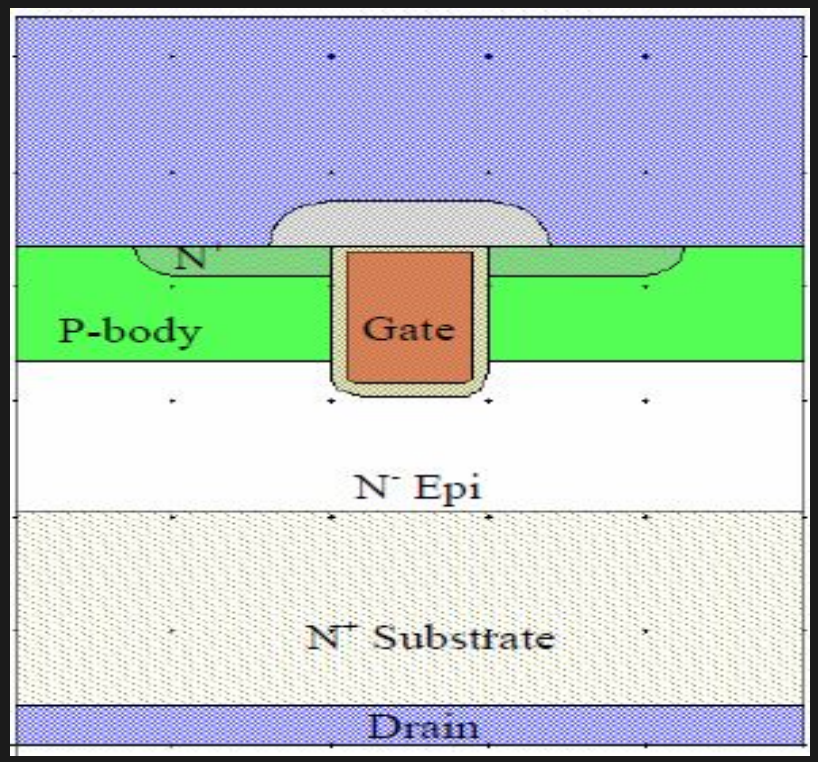

Figure [2 a]. Trench MOSFET

Planar MOSFET Structure

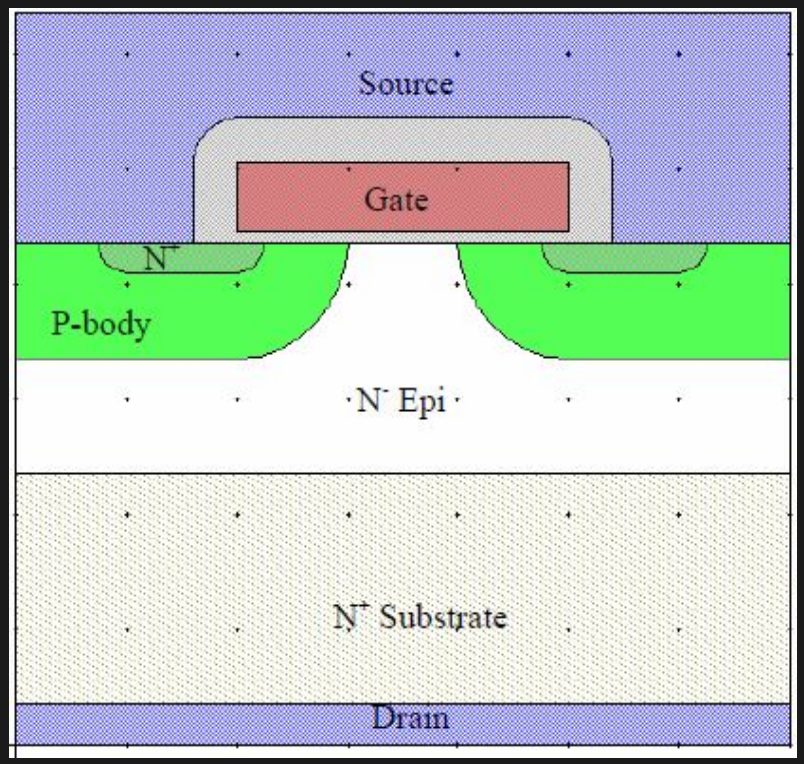

Figure [2 b]. Planar MOSFET

- Trench MOSFETs are mainly used for <200V voltage rating due to their higher channel density and thus lower on-resistance.
- Planar MOSFETs are good for higher voltage ratings since on-resistance is dominated by epi-layer resistance and high cell density is not beneficial.
- The basic MOSFET operation is the same for both structures.
- In this slides we will be discussing about N-channel trench MOSFET.

Breakdown Voltage - I

- In most power MOSFETs the N^+ source and P-body junction are shorted through source metallization to avoid accidental turn-on of the parasitic bipolar transistor.
- When no bias is applied to the Gate, the Power MOSFET is capable of supporting a high Drain voltage through the reverse-biased P-body and N^- epitaxial junction.
- In high voltage devices, most of the applied voltage is supported by the lightly doped epitaxial layer.
- A thicker and more lightly doped epitaxial supports higher breakdown voltage but with increased on-resistance.
- In lower voltage devices, the P-body doping becomes comparable to the N^- epitaxial layer and supports part of the applied voltage.
- Careful design of the body and Epi doping and thickness is needed to optimize the performance.

On-State Characteristic

- In this we will consider power MOSFET under two different modes of operations:

    1) The first quadrant operation.

    2) The third quadrant operation.

First Quadrant Operation

- For an n-channel MOSFET, the device operates in the first quadrant when a positive voltage is applied to the drain, as shown in figure on next slide.
- As the gate voltage V_G increases above the threshold voltage V_{TH}, the MOSFET channel begins to conduct current.
- The amount of current it conducts depends on the on-resistance of the MOSFET, as defined by

$$R_{DSON} = V_D/I_D$$

- For sufficiently large gate overdrive ($V_G >> V_{TH}$), the I_D-V_D curve appears linear because the MOSFET channel is fully turned on.
- Under low gate overdrive, the drain current reaches a saturation point when $V_D > (V_G\text{-}V_{TH})$ due to a pinch-off effect of the channel.

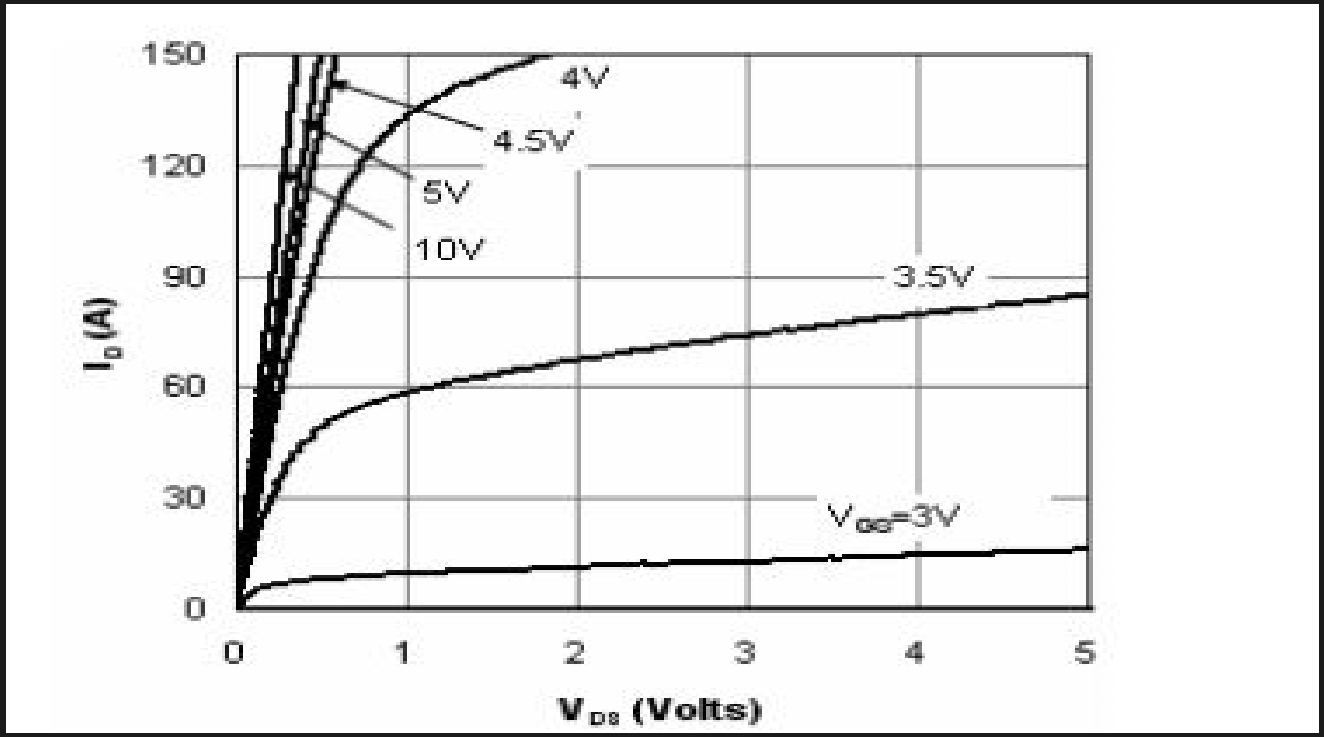

Figure [3]. On-region characteristics (first-quadrant operation)

For Trench MOSFET R_{DSON} consist of following components:

- R_S: source resistance
- R_{CH}: channel resistance
- R_{ACC}: resistance from the accumulation region
- R_{EPI}: resistance from the top layer of silicon (epitaxial silicon, also known as epi); epi controls the amount of blocking voltage the MOSFET can sustain
- R_{SUBS}: resistance from the silicon substrate on which the epi is grown

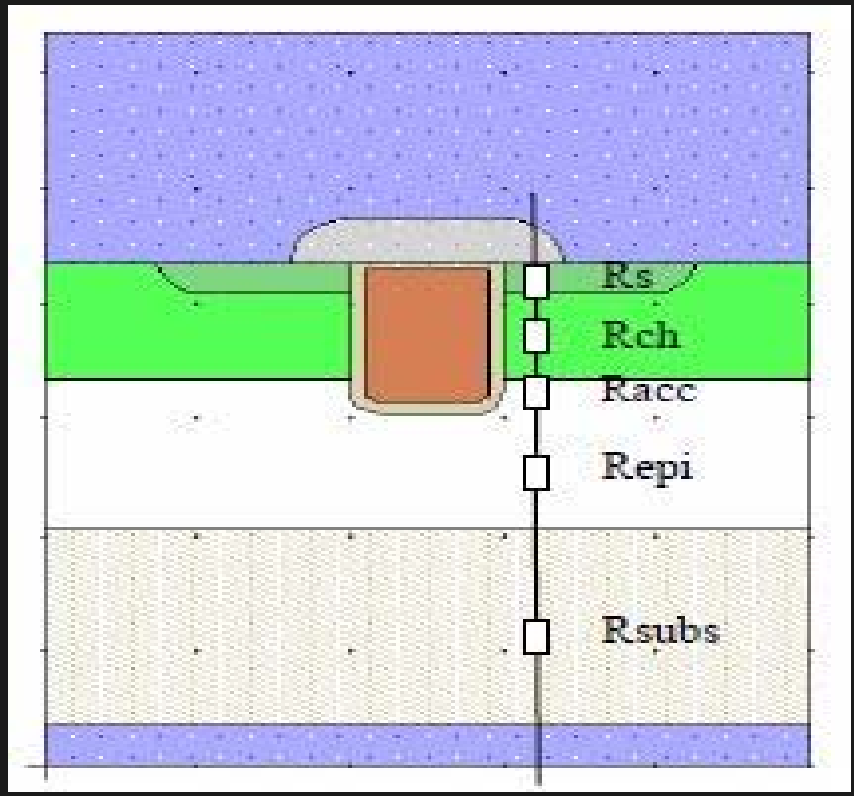

Figure [4]. R_{DSON} components of a trench MOSFET

For a planar MOSFET, the R_{DSON} components are similar to that of a trench MOSFET.

- The primary difference is the presence of a JFET component.
- As devices scale down to smaller dimensions, R_S, R_{CH}, R_{ACC} are reduced because more individual unit cells can be packed in a given silicon area. R_{JFET} on the other hand suffers from a “JFET”-effect where current is constrained to flow in a narrow n-region by the adjacent P-body region.
- Due to the absence of R_{JFET}, trench MOSFETSs benefit from high density scaling to achieve very low R_{DSON}

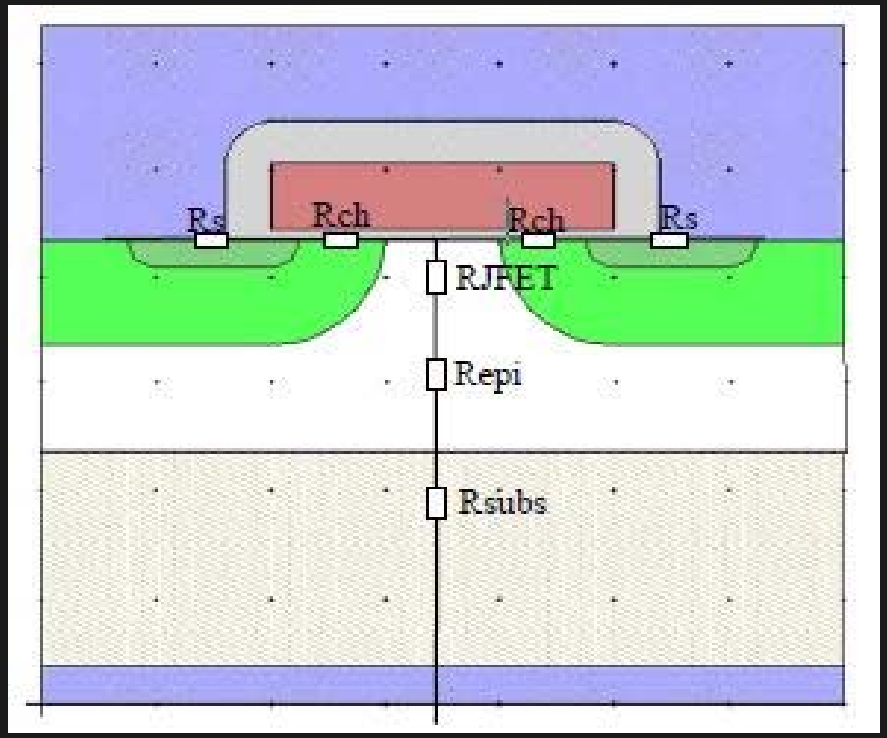

Figure [5]R_{DSON} components of a planar MOSFET

On State Characteristic - II

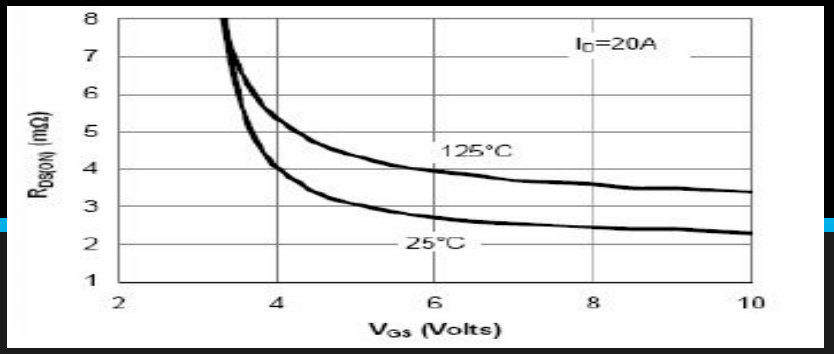

Figure [6].R_{DSON} vs. Gate bias and Temperature

- The channel resistance R_{CH} is highly dependent on the amount of the gate overdrive.
- R_{CH} decreases with increasing V_{GS}.
- R_{DSON} initially decreases rapidly as V_{GS} increases above V_{TH}, indicating the turning-on of the MOSFET channel.
- As V_{GS} increases further, R_{DSON} drops to a flat region because the channel is fully turned on and the MOSFET resistance is limited b the other resistance components.
- R_{DSON} increases with temperature due to the decreasing carrier mobility. This is an important characteristic for device paralleling.

Threshold Voltage

- Threshold voltage, $V_{GS(TH)}$ is defined as the minimum gate bias which can form a conducting channel between the source and drain.
- For power MOSFETs, it is usually measured at the drain-source current of 250uA. Gate oxide thickness and doping concentration of the channel can be used to control the $V_{GS(TH)}$.
- Threshold voltage has a negative temperature coefficient, which means it decreases with increasing temperature.
- With power MOSFETs finding increasing use in portable electronics and wireless communications where battery power is at a premium, the trend is toward lower values of R_{DSON} and V_{TH}.

Third Quadrant Operation - I

- Third-quadrant operation for power MOSFET is common in DC-DC buck converters, where the current conduction occurs under at V_{DS} (for an n-channel MOSFET).
- Current flows in the reverse direction compared to first-quadrant operation. The same R_{DSON} components apply.
- Under relatively low current, the on-state characteristics for the third-quadrant operation are symmetric to that of the first quadrant operation. Thus, we can assume same R_{DSON} for both types of operation.

Third Quadrant Operation - II

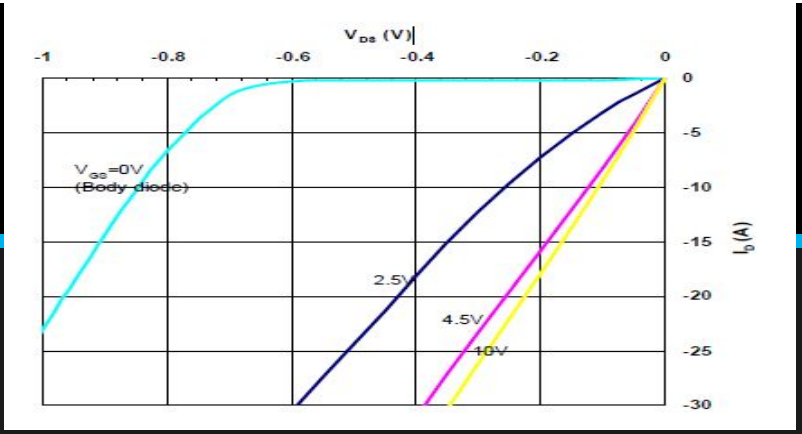

Figure [8].Third Quadrant Operation

- Difference would appear only under sufficient large current, and therefore sufficient large V_{DON}.
- When V_{DON} approaches the forward drop voltage of the body diode, the body diode starts to conduct.
- Hence, the current increases and no current saturation behavior is observed.

Capacitance

- The MOSFET's switching behavior is affected by the parasitic capacitances between the device's three terminals, that is, gate-to-source C_{GS}, gate-to-drain C_{GD} and drain-to-source C_{DS} capacitances as shown in figure.
- These capacitances values are non-linear and a function of device structure, geometry, and bias voltages.

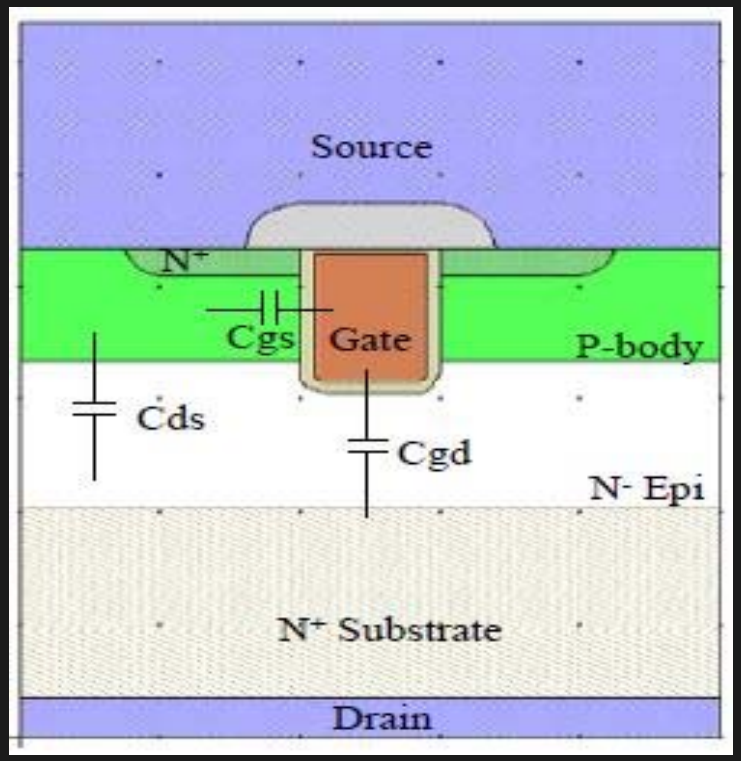

Figure [10] Illustration of MOSFET parasitic capacitances

Capacitance - II

- The MOSFET capacitances are non-linear as well as a function of the dc bias voltage. Figure 11a shows how capacitances vary with increased V_{DS} voltage.
- All the MOSFET capacitances come from a series combination of a bias independent oxide capacitance and a bias dependent depletion (Silicon) capacitance.
- The decrease in capacitances with V_{DS} comes from the decrease in depletion capacitance as the voltage increases and the depletion region widens.

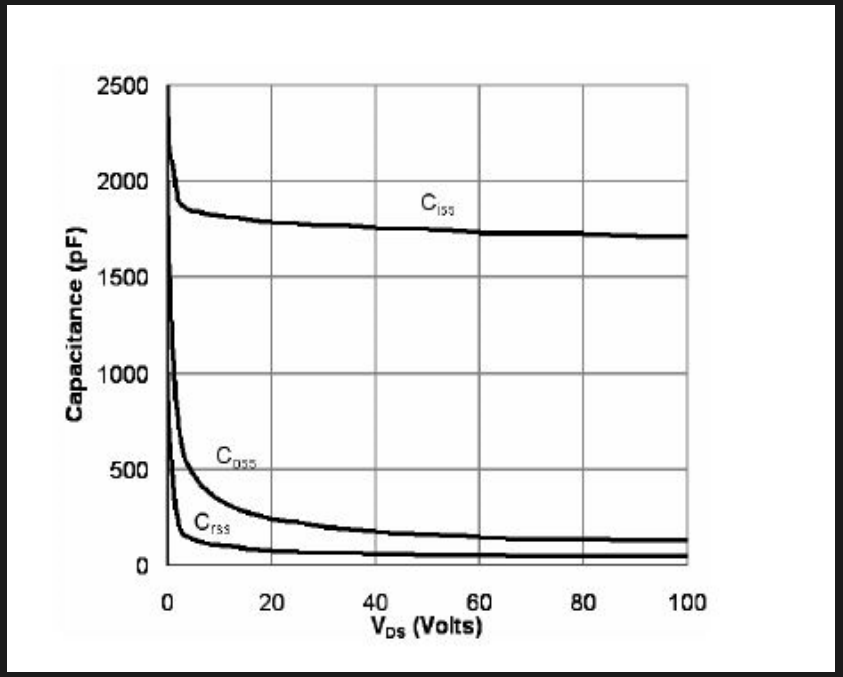

Figure [11 a]. Typical variation of Capacitances with V_{DS}

Capacitance - III

- Figure 11b shows that the MOSFET gate capacitance also increases when the V_{GS} voltage increases past the threshold voltage (for low V_{DS} values) because of the formation of an inversion layer of electrons in the MOS channel and an accumulation layer of electrons under the trench bottom.
- This why the slope of the gate charge curve increases once the voltage goes beyond the Q_{gd} phase.

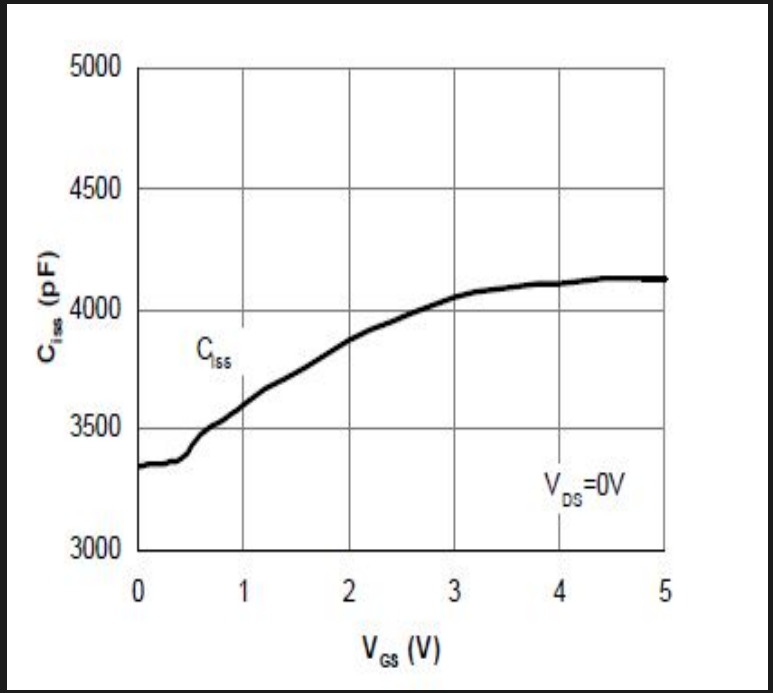

Figure [11 b]. Typical variation of C_{ISS} with V_{GS}

Gate Charge/ Gate Resistance

- Gate charge parameter can be used to estimate switching times of the power MOSFET once the gate drive current is known.
- It depends only on the device parasitic capacitances. This parameter is also weakly dependent of the drain current, the supply voltage, and the temperature.
- The power MOSFET gate presents an impedance like an RC network to its gate drive.
- The equivalent R is referred to as the gate resistance R_g. The gate resistance is caused by the finite resistance of the Polysilicon gate conductors, and the metal and contact structures that route the gate signal to the pad for connection to external package leads.

Power Dissipation

- Power dissipation P_D and P_{DSM} are the maximum power that is allowed for device safe operation. Power dissipation is calculated using the following formula:

$$P_D = \frac{T_{J(max)} - T_C}{R\Theta_{JC(max)}}$$

$$P_{DSM} = \frac{T_{J(max)} - T_A}{R\Theta_{JA(max)}}$$

- T_j max = Maximum allowable temperature of the p-n junction in the device (normally 1500C or 1750C) R Θ JC / JA = Junction-to-case thermal impedance of the device.
- P_D is based on junction to case thermal resistance.
- P_{DSM} is based on junction to ambient thermal resistance.

Package Limitation

- Continuous current rating is limited by two factors:

  1. thermal resistance 2. package limitation

- Package limitation usually refers to bond wire current handling capability. The conventional way to rate bond wire current limit is based on bond wire fusing temperature, which is not correct because:

  1. Wire temperature can not exceed 220^{o}C, or it will cause the degradation of the plastic molding compound.

  2. In most cases the silicon resistance is ~10 times higher than wire resistance. Most of the heat is generated on the silicon surface. The hottest spot is on silicon.

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