ECE 4813

Semiconductor Device and Material Characterization

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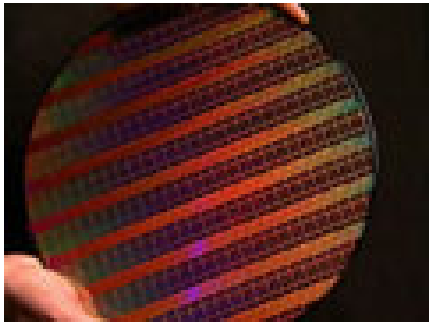
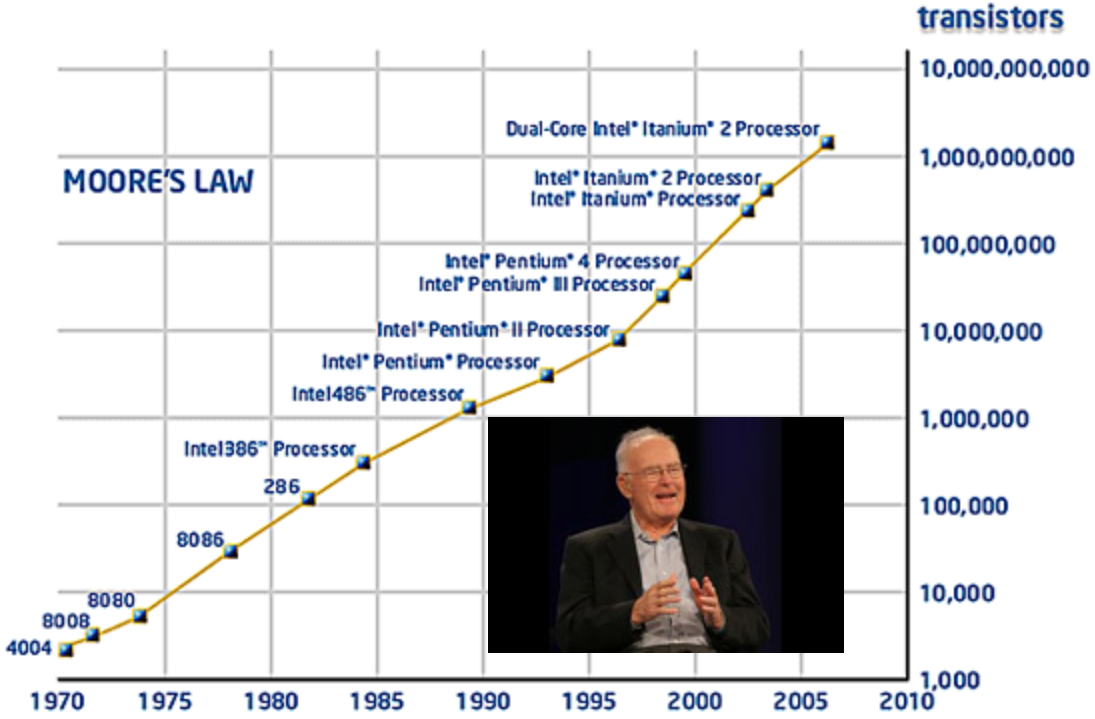
As with all of these lecture slides, I am indebted to Dr. Dieter Schroder from Arizona State University for his generous contributions and freely given resources. Most of (>80%) the figures/slides in this lecture came from Dieter. Some of these figures are copyrighted and can be found within the class text, *Semiconductor Device and Materials Characterization*. ***Every serious microelectronics student should have a copy of this book!***

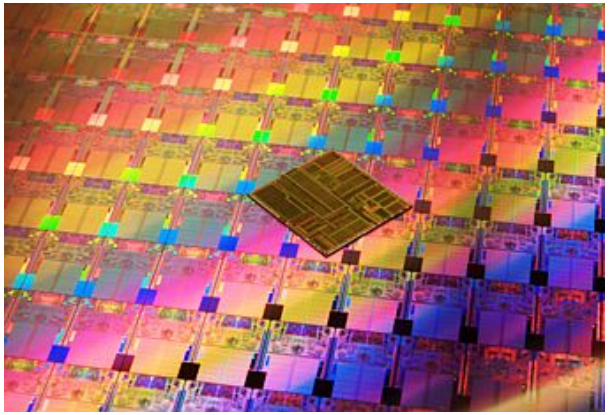
Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

Moore's Law: The Growth of the Semiconductor Industry

Moore's law (Gordon Moore, co-founder of Intel, 1965):
Empirical rule which predicts that the number of components per chip doubles every 18-24 months
Moore's Law turned out to be valid for more than 30 years (and still is!)







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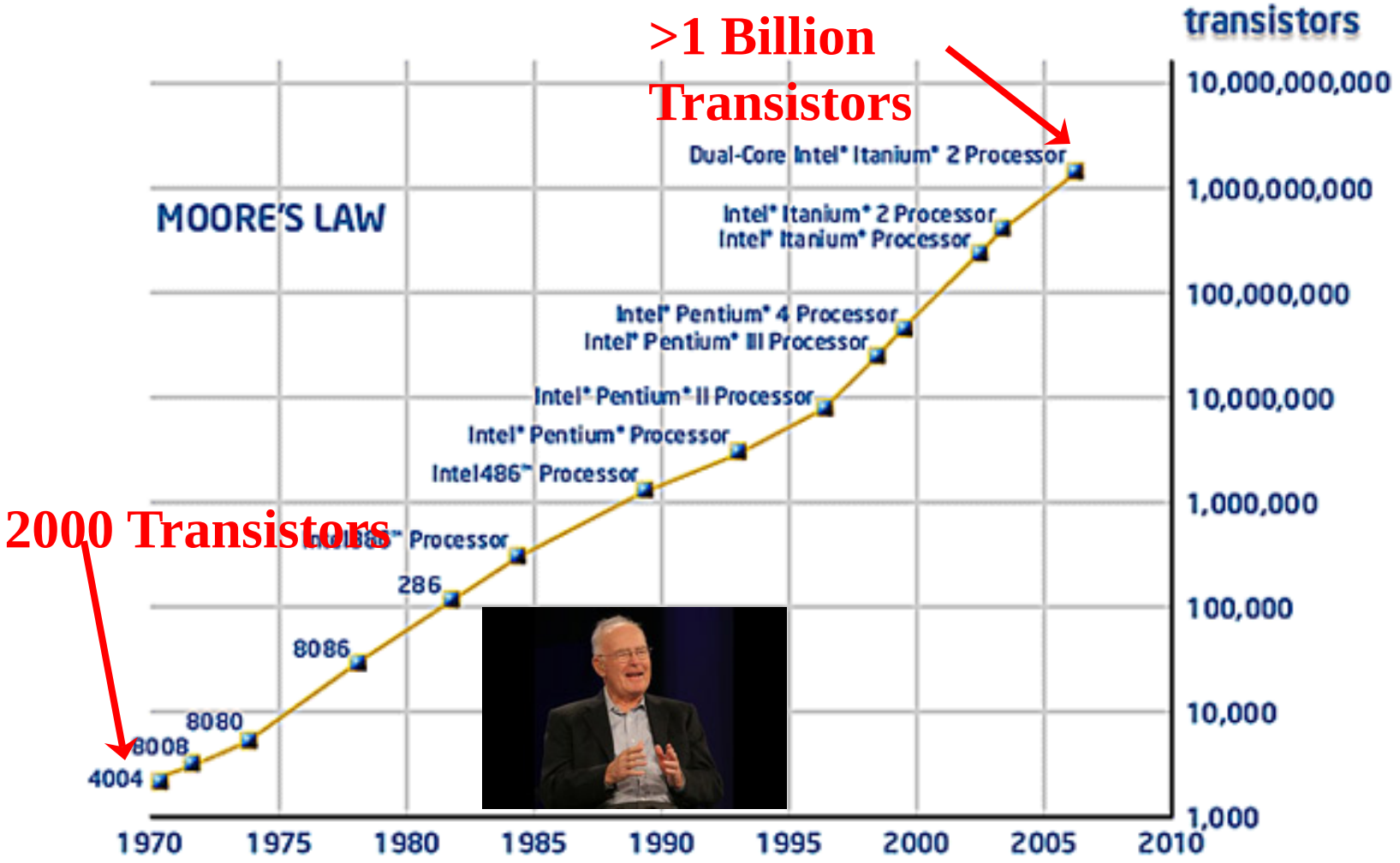

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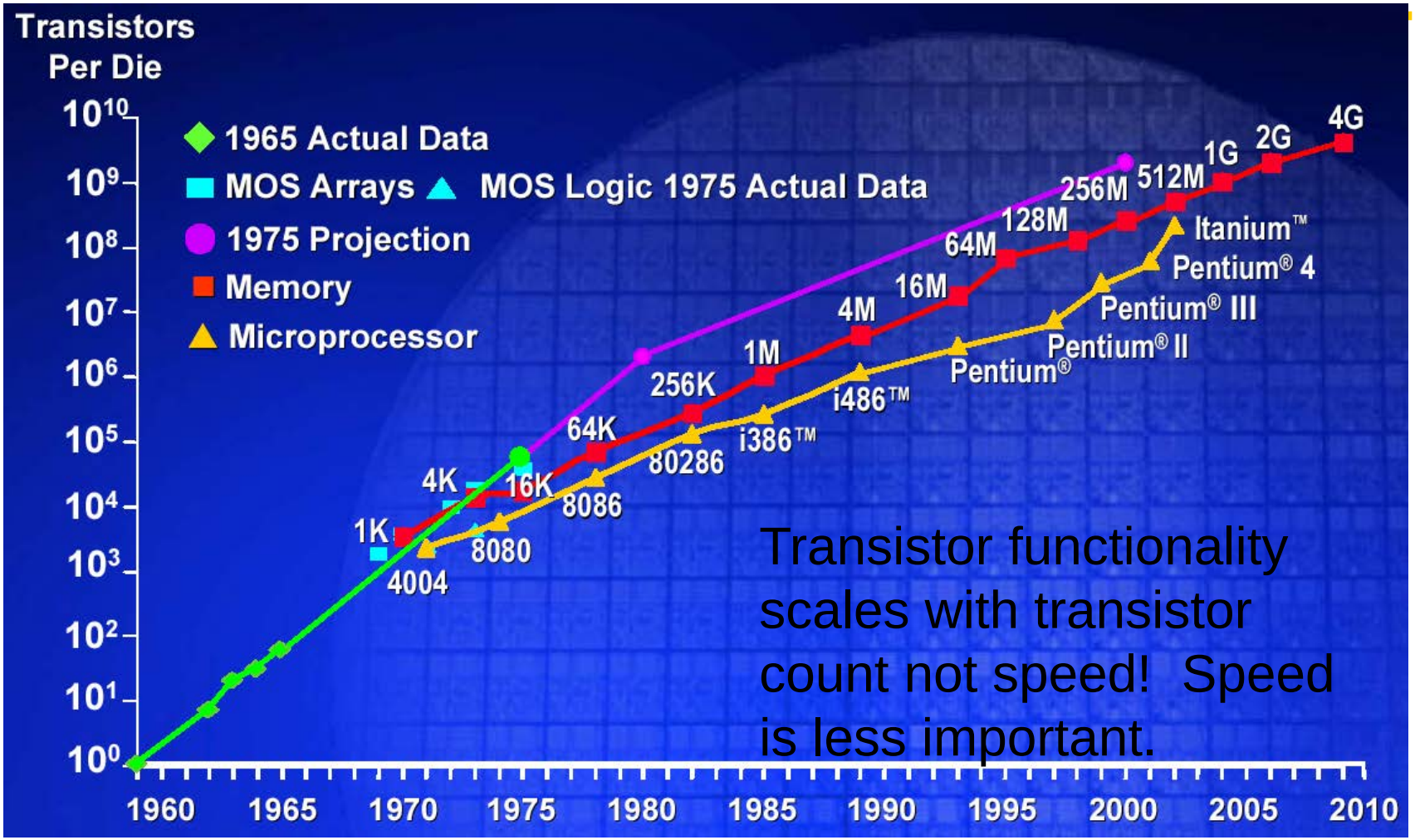
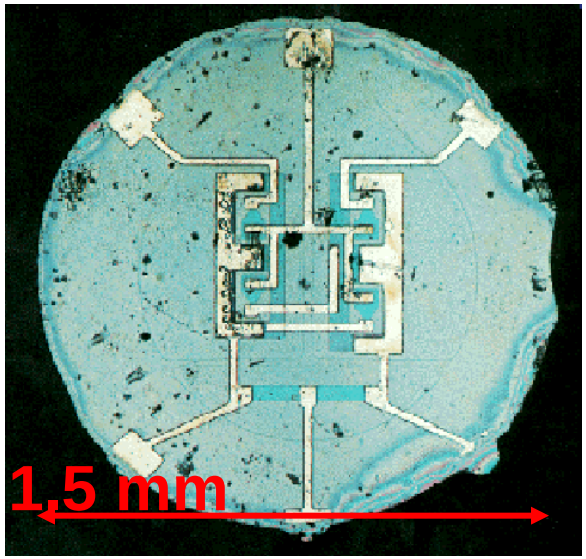


from G. Moore, ISSCC 2003

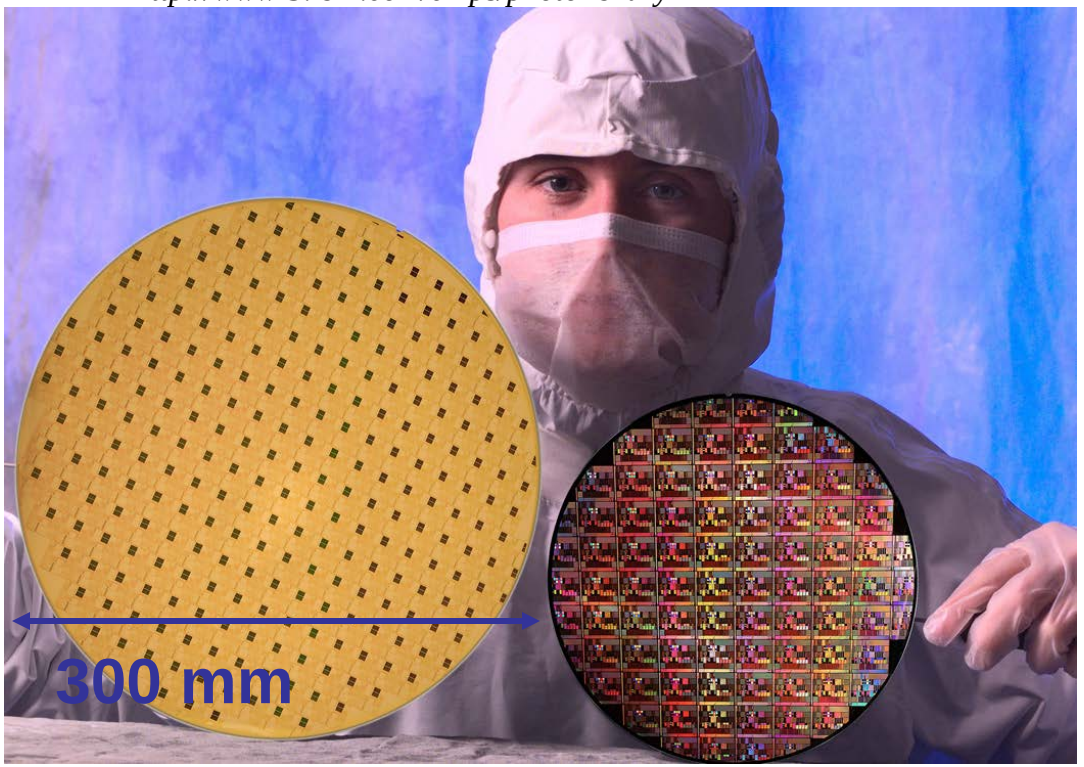
Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

How did we go from 4 Transistors/wafer to Billions/wafer?



First Planar IC
1961, Fairchild
http://smithsonianchips.si.edu/

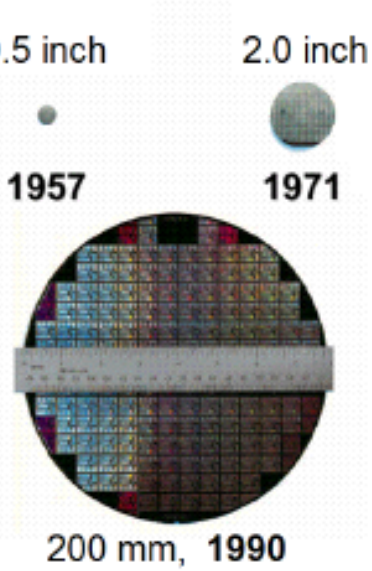
IBM 200 mm and 300 mm wafer
http://www-3.ibm.com/chips/photolibrary

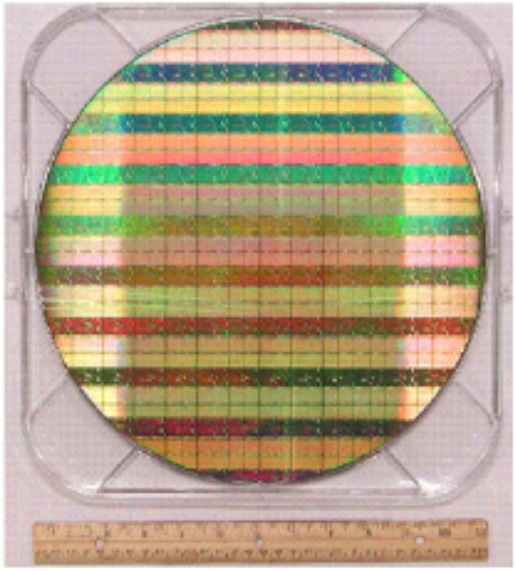


Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

Some Facts About Silicon (Si):

- Si is a Group IV element, and crystallizes in the diamond structure
- Perfect Si crystals can be grown very large (12 inches by 8 feet!)
- Si can be made extremely pure (< .000001 ppm impurities!)
- Si is very abundant and non-toxic (70% of the earth's crust are silicates!)
- Si oxidizes trivially to form one of nature's most perfect insulators (SiO_2)
- Si is a great conductor of heat (better than many metals!)





Slide after Dr. John Cressler

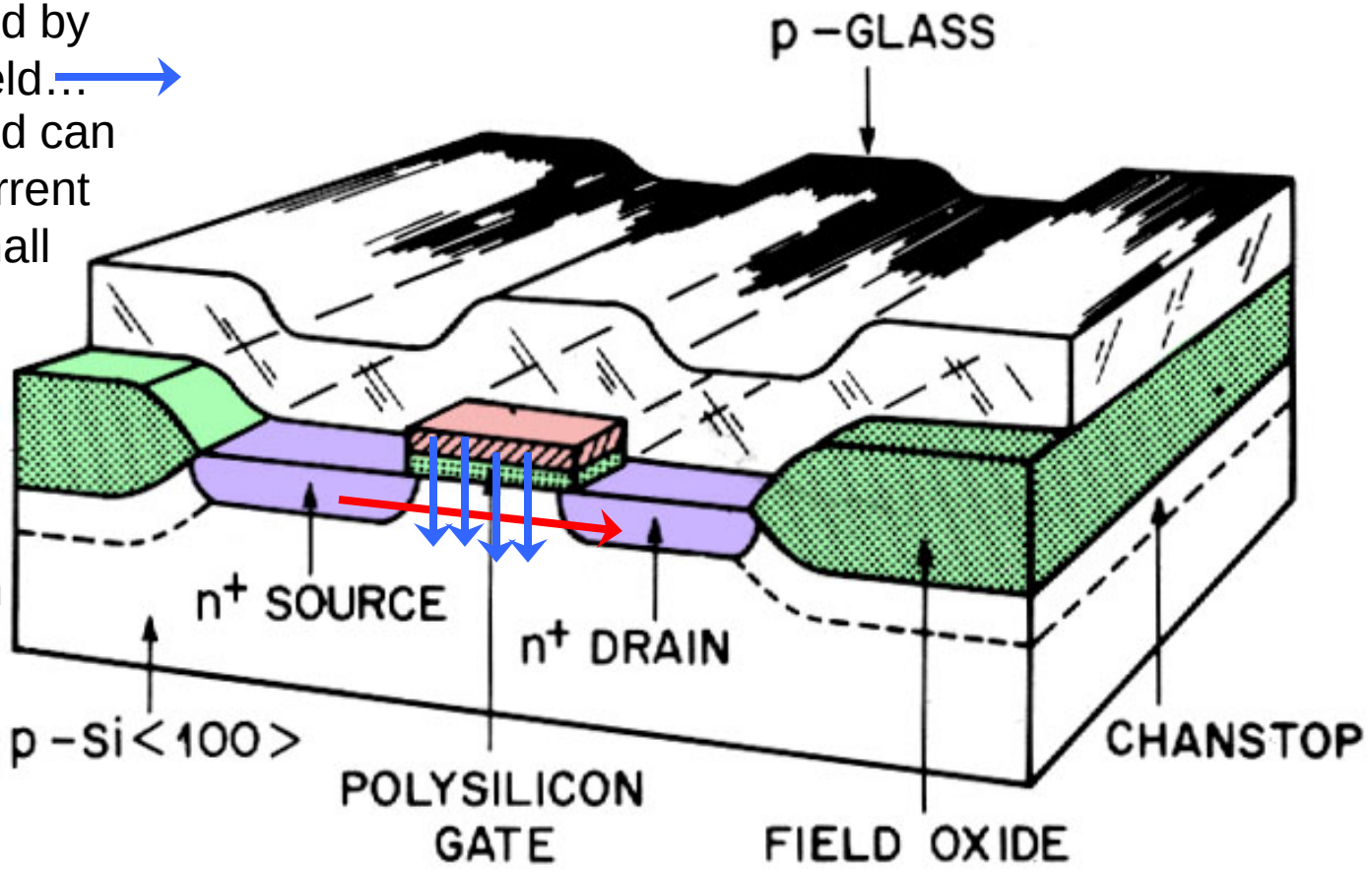
The Basic Device in CMOS Technology is the MOSFET

Direction of Desired Current flow… →

…is controlled by an electric field… →

…but this field can also drive current through a small gate.

Modern (pre-2009) transistors have more power loss in the gate circuit than the source - drain! New approaches are needed.



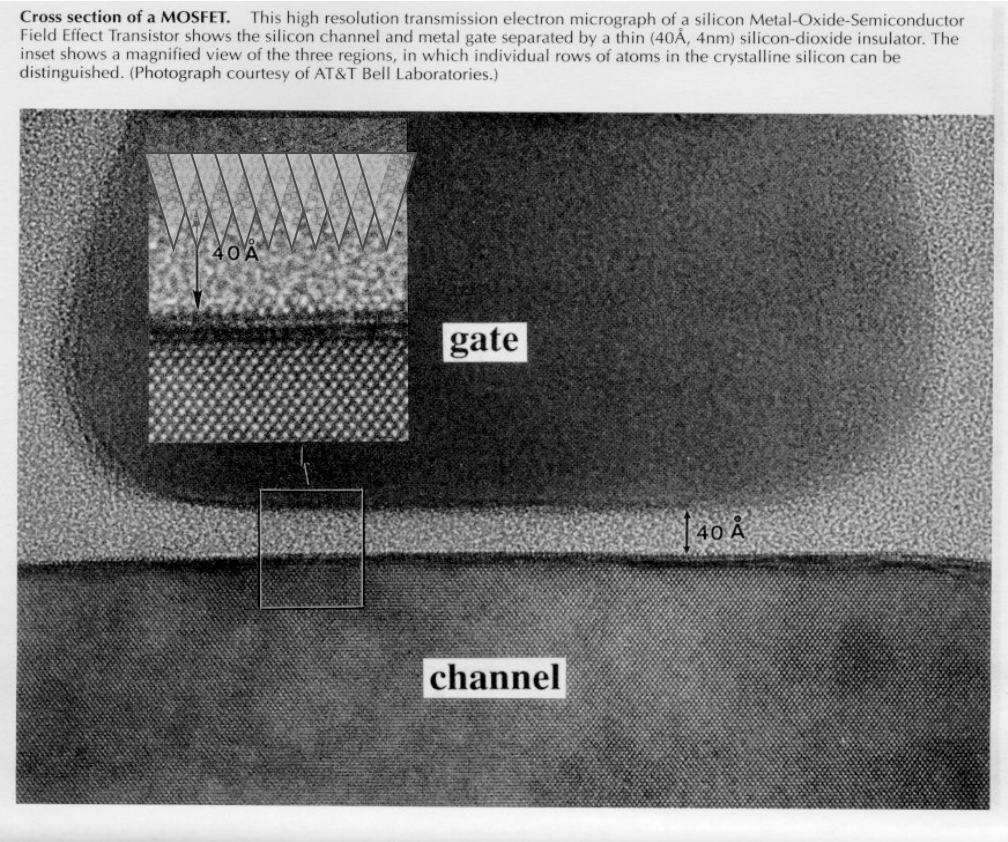
Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

Early MOSFET: SiO_2 Gate Oxide, Aluminum (Al) Source/Drain/Gate metals

Problem: As sizes shrank, devices became unreliable due to metallic spiking through the gate oxide.

Solution: Replace Metal Gate with a heavily doped poly-silicon.

This change carried us for decades with challenges in fabrication (lithography) being the primary barriers that were overcome …until…



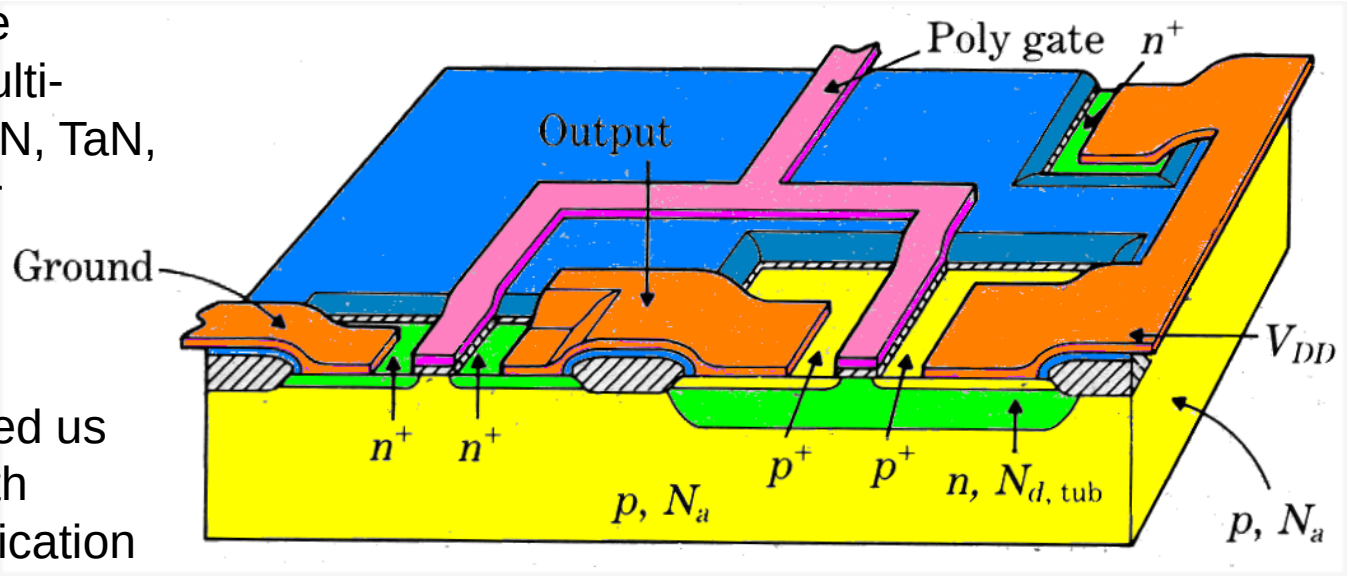
Cross section of a MOSFET. This high resolution transmission electron micrograph of a silicon Metal-Oxide-Semiconductor Field Effect Transistor shows the silicon channel and metal gate separated by a thin (40Å, 4nm) silicon-dioxide insulator. The inset shows a magnified view of the three regions, in which individual rows of atoms in the crystalline silicon can be distinguished. (Photograph courtesy of AT&T Bell Laboratories.)

Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

Semi-Modern MOSFET (late 1990's vintage): SiO_2 Gate Oxide, Polysilicon gate metals, metal source/drain contacts and Aluminum metal interconnects

Problem: As interconnect sizes shrank, Aluminum lines became too resistive leading to slow RC time constants

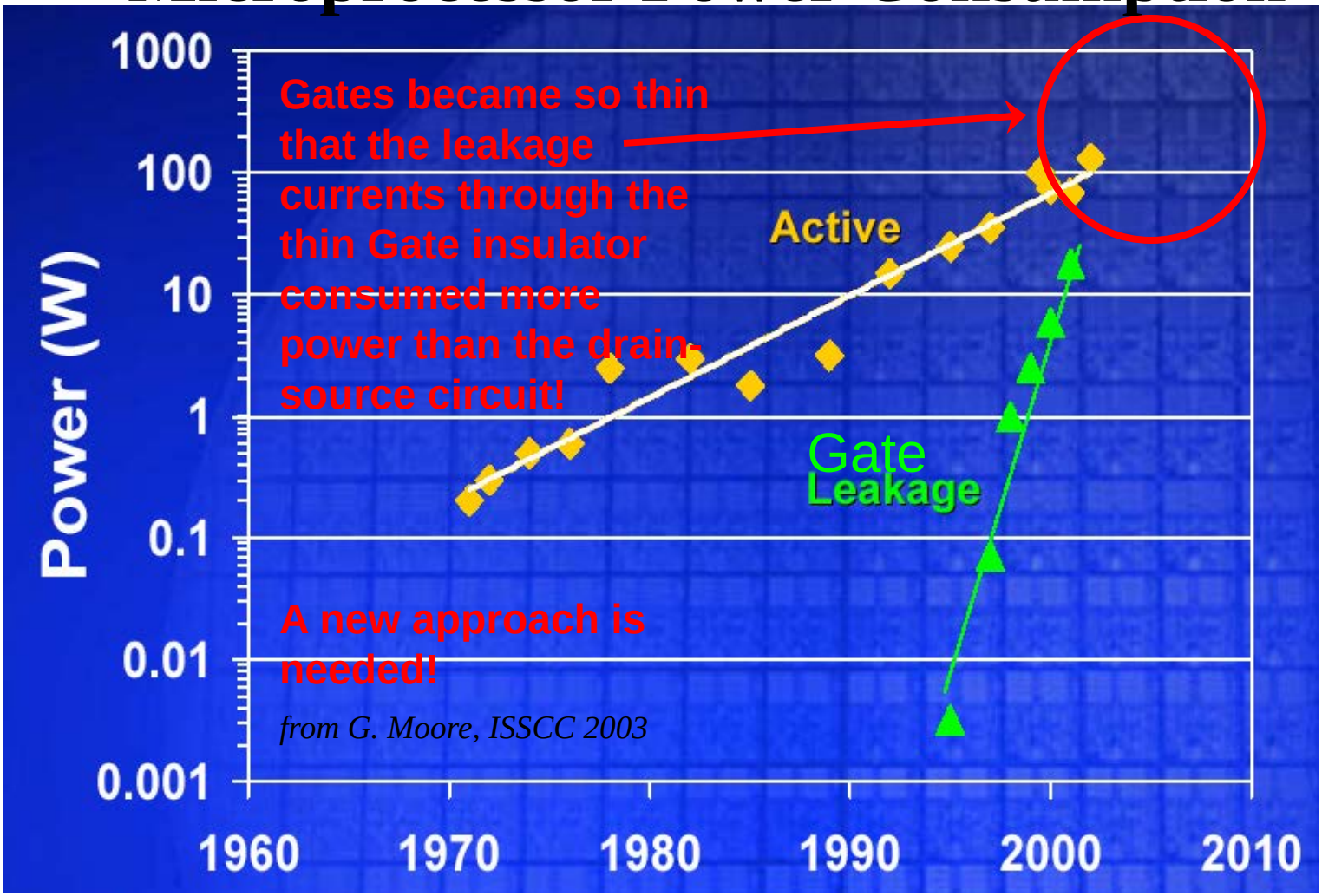
Solution: Replace Aluminum with multi-metal contacts (TiN, TaN, etc…) and copper interconnects.



This change carried us for ~ 1 decade with challenges in fabrication (lithography) being the primary barriers that were overcome …until…

Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

Microprocessor Power Consumption



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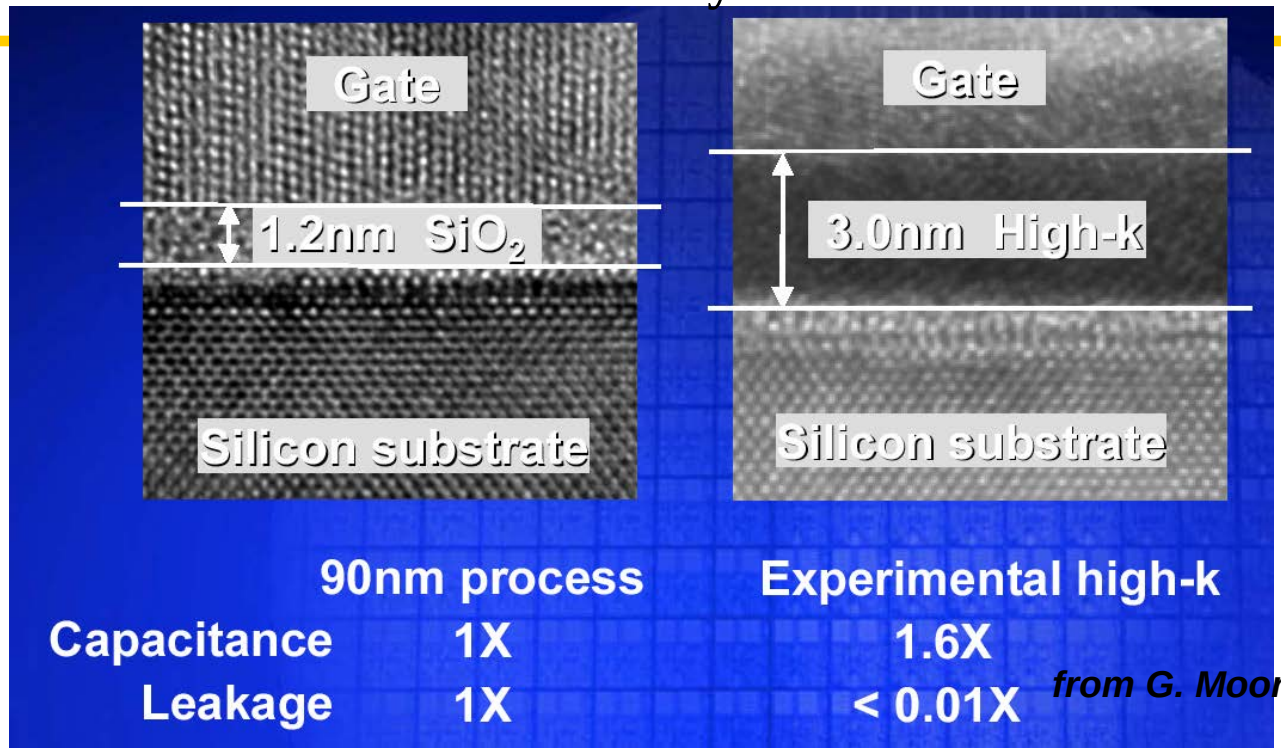


from G. Moore, ISSCC 2003

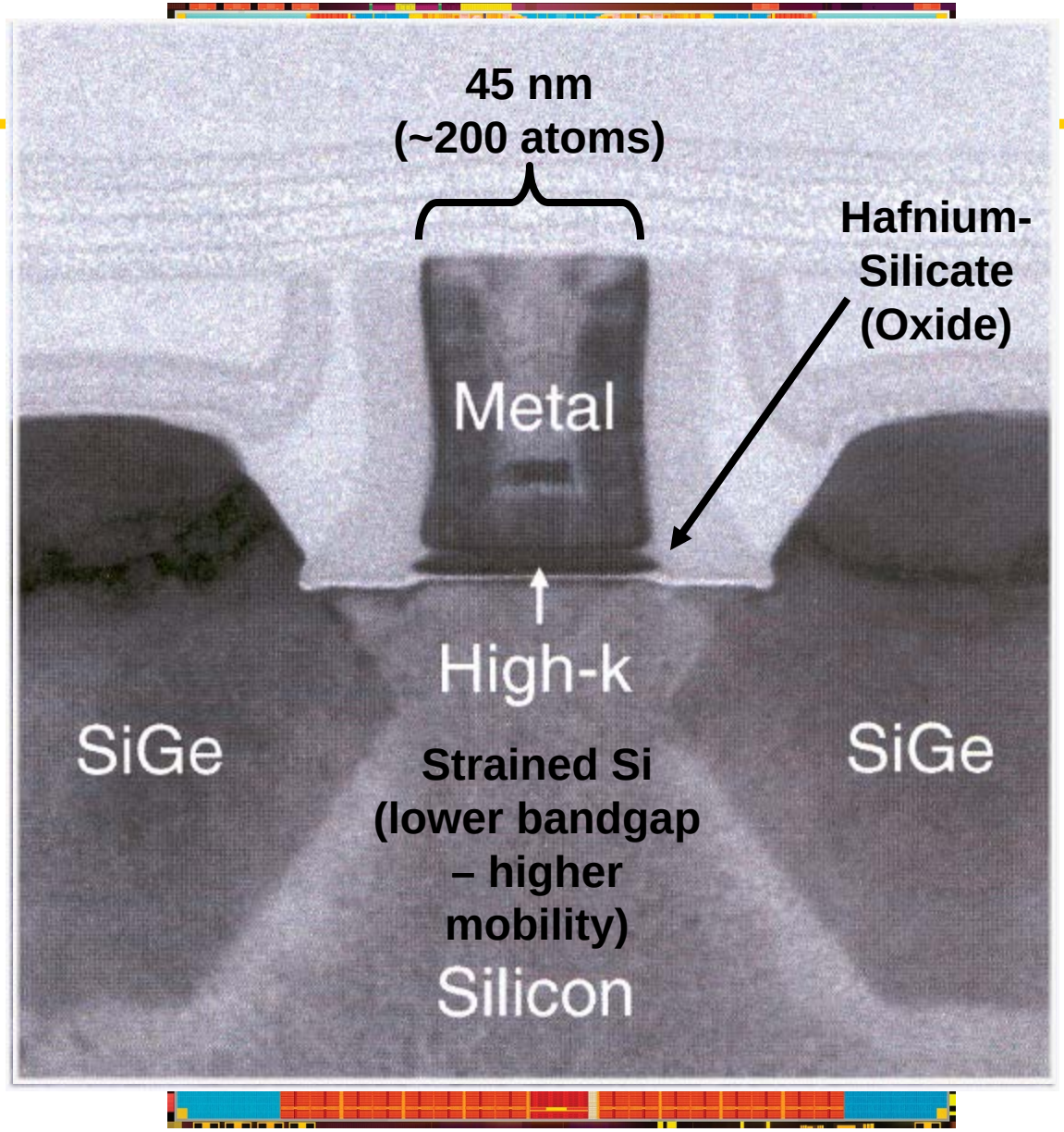
$$D_{insulator} = k_{insulator} E$$

$$D_{insulator} = k_{insulator} \left(\frac{V_{Gate}}{t_{Gate}} \right)$$

$$I_{Gate\ Leakage} \propto e^{t_{Gate}}$$

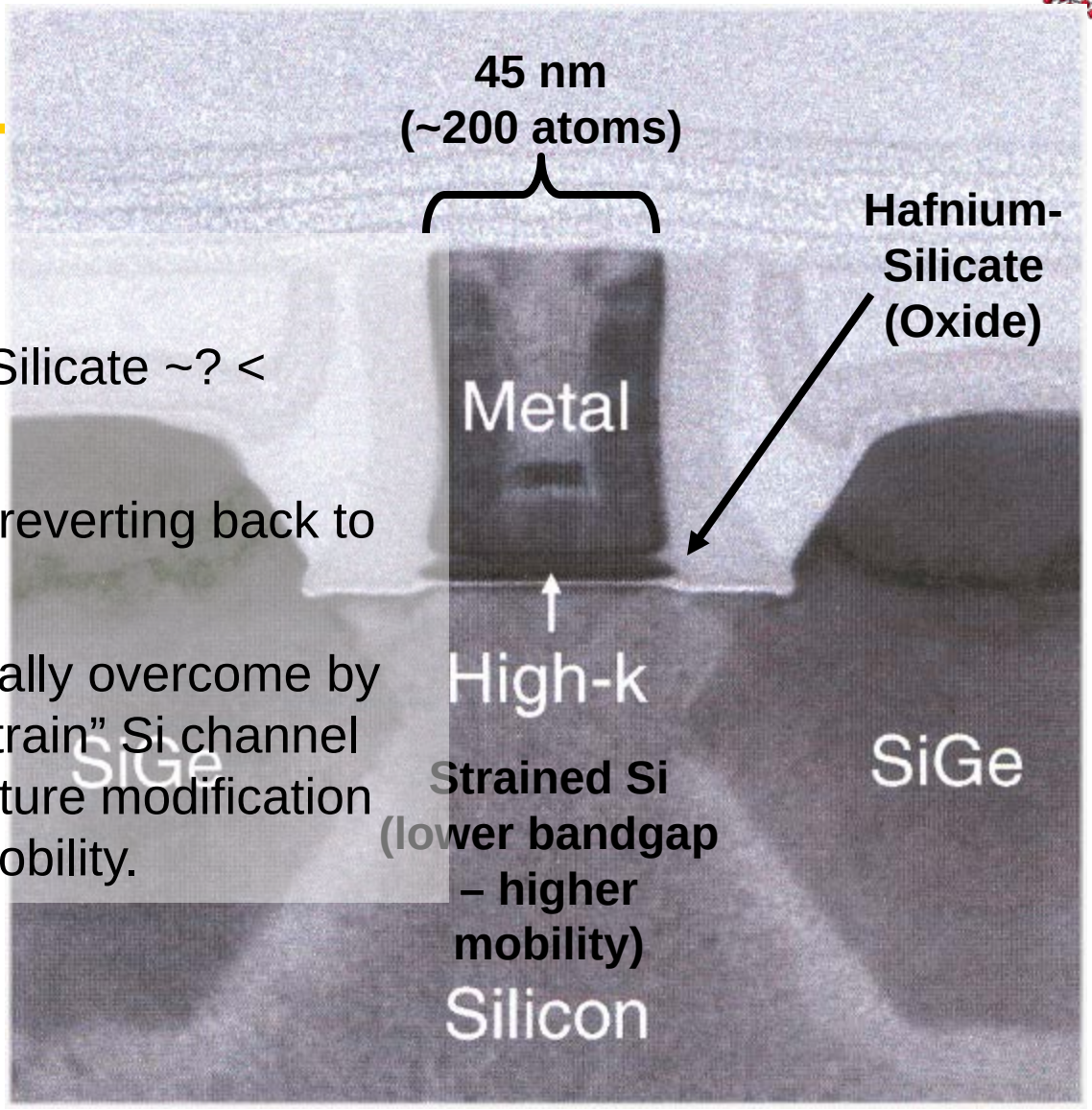
Gate leakage current can be dramatically lowered by increasing Gate insulator thickness but to do so without changing the channel conductivity, you have to increase the dielectric constant of the insulator. NEW GATE INSULATORS FOR THE FIRST TIME IN 60 YEARS!!!!

2008 Vintage Intel Microprocessor

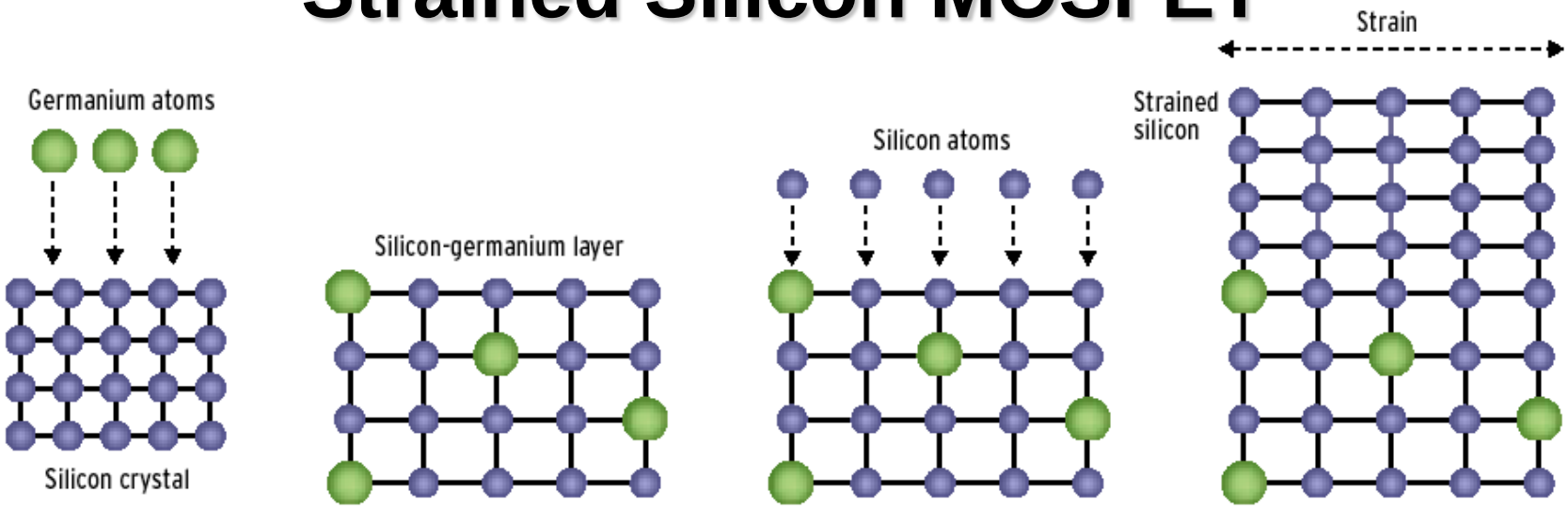


2008 Vintage Intel Microprocessor

- High K Gate Dielectric:
  - K of SiO_2~3.9< Hafnium Silicate ~? < HfO_2~ 22
- Deviation from SiO_2 required reverting back to Metal Gates (no Poly-silicon)
- Limited Speed of Silicon partially overcome by using SiGe to "mechanically strain" Si channel resulting in Energy Band structure modification that increases electron/hole mobility.



Strained Silicon MOSFET



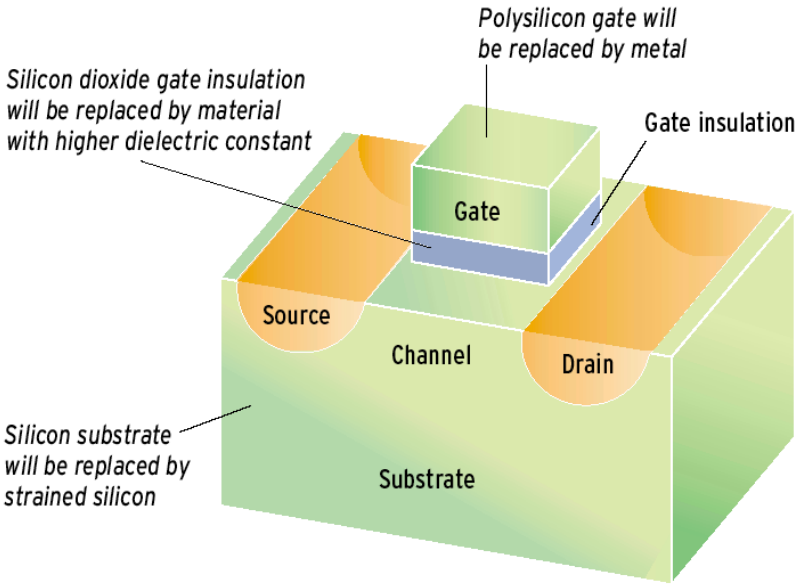
from IEEE Spectrum, 10/2002

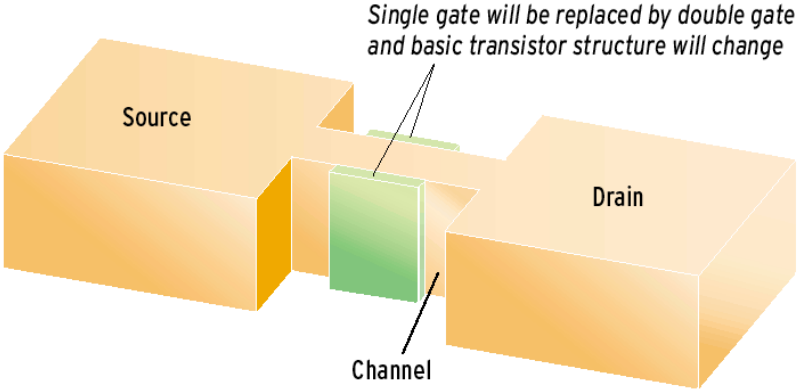
- **Silicon in channel region is strained in two dimensions by placing a Si-Ge layer underneath (or more recently adjacent to) the device layer**
- **Strained Si results in changes in the energy band structure of conduction and valence band, reducing lattice scattering**
- **Benefit: increased carrier mobility, increased drive current (drain current)**

Slide after Dr. Oliver Brandt

What is in the future? Double-Gate Transistors

- Change of basic transistor structure by introducing a double gate (or more general enclose the channel area by the gate)
- Benefit: better channel control resulting in better device characteristics
- Challenge: double-gate transistors require completely new device structures with new fabrication challenges

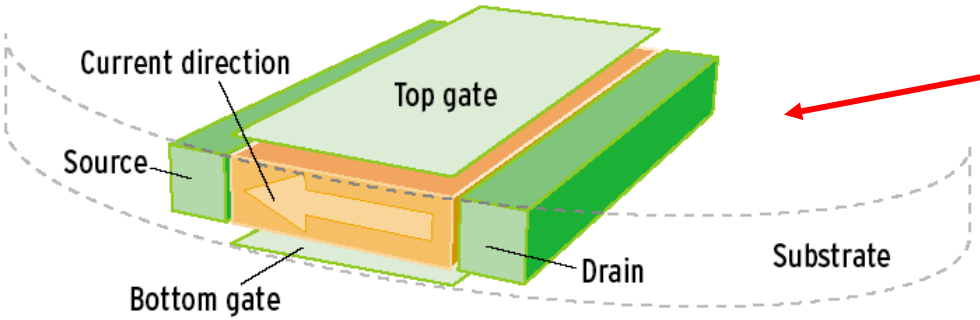




from IEEE Spectrum, 10/2002

Slide after Dr. Oliver Brandt

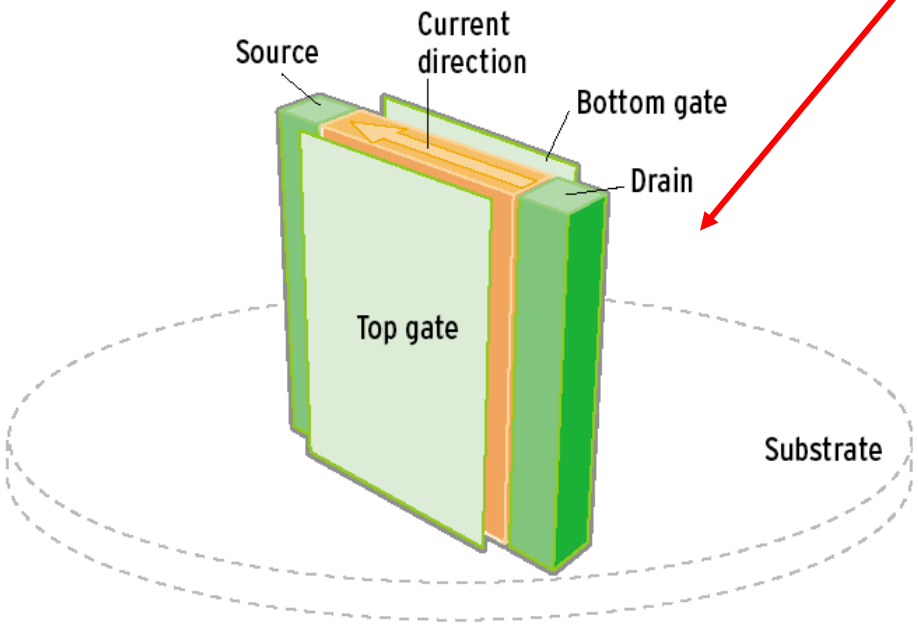
Double-Gate Transistor Designs

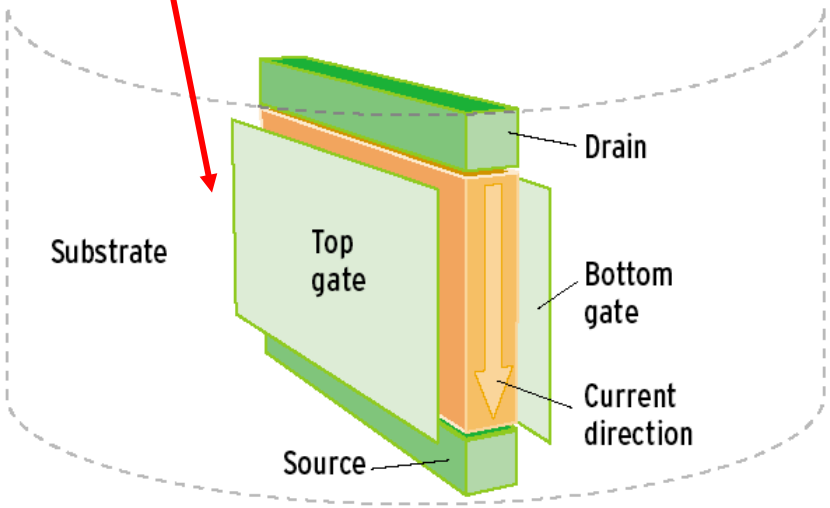


Channel in chip plane

Channel perpendicular to chip plane with current flow in chip plane (FinFET)

Channel perpendicular to chip plane with current flow perpendicular to chip plane

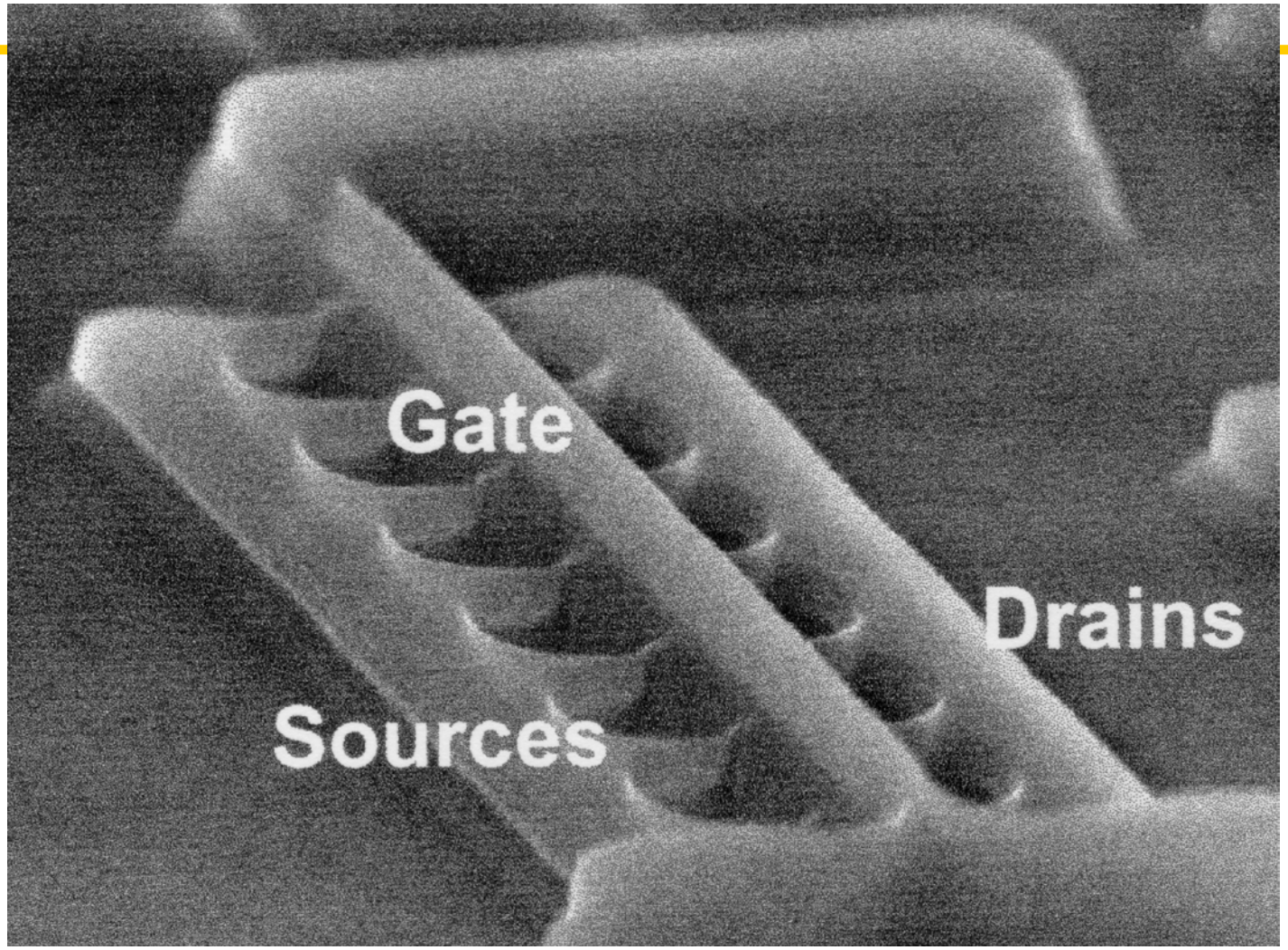




from IEEE Spectrum, 10/2002

Slide after Dr. Oliver Brandt

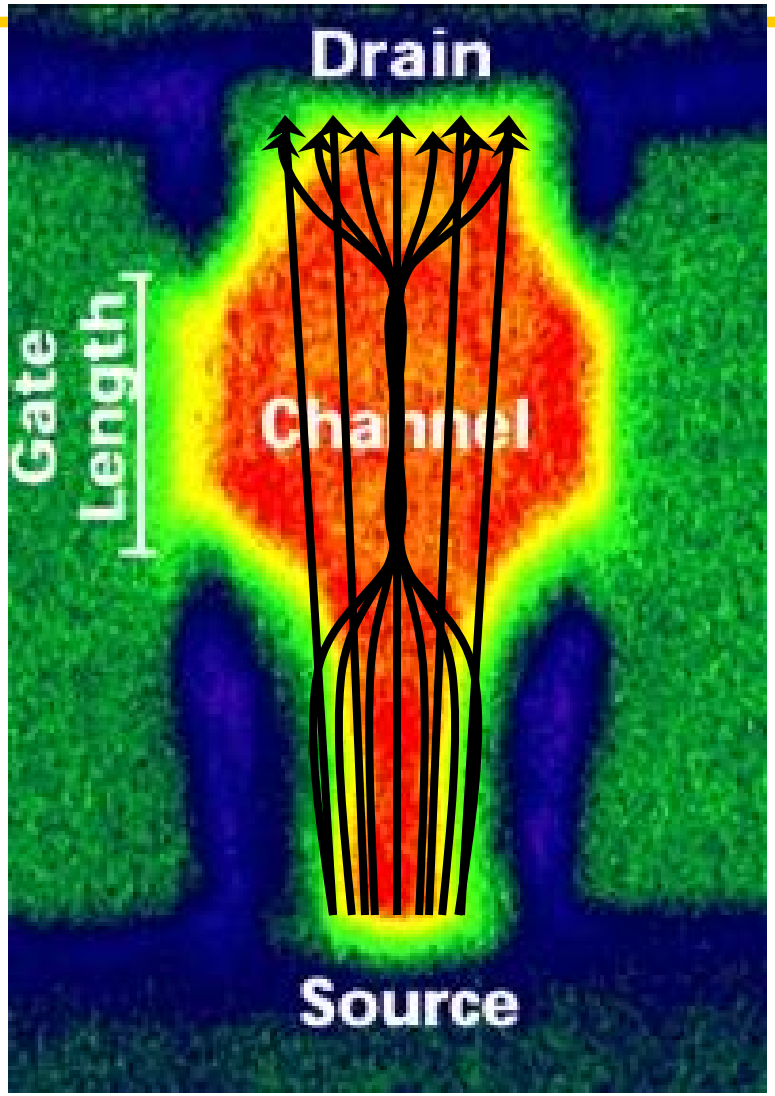
FinFET Double-Gate Transistor



from http://www.intel.com/pressroom

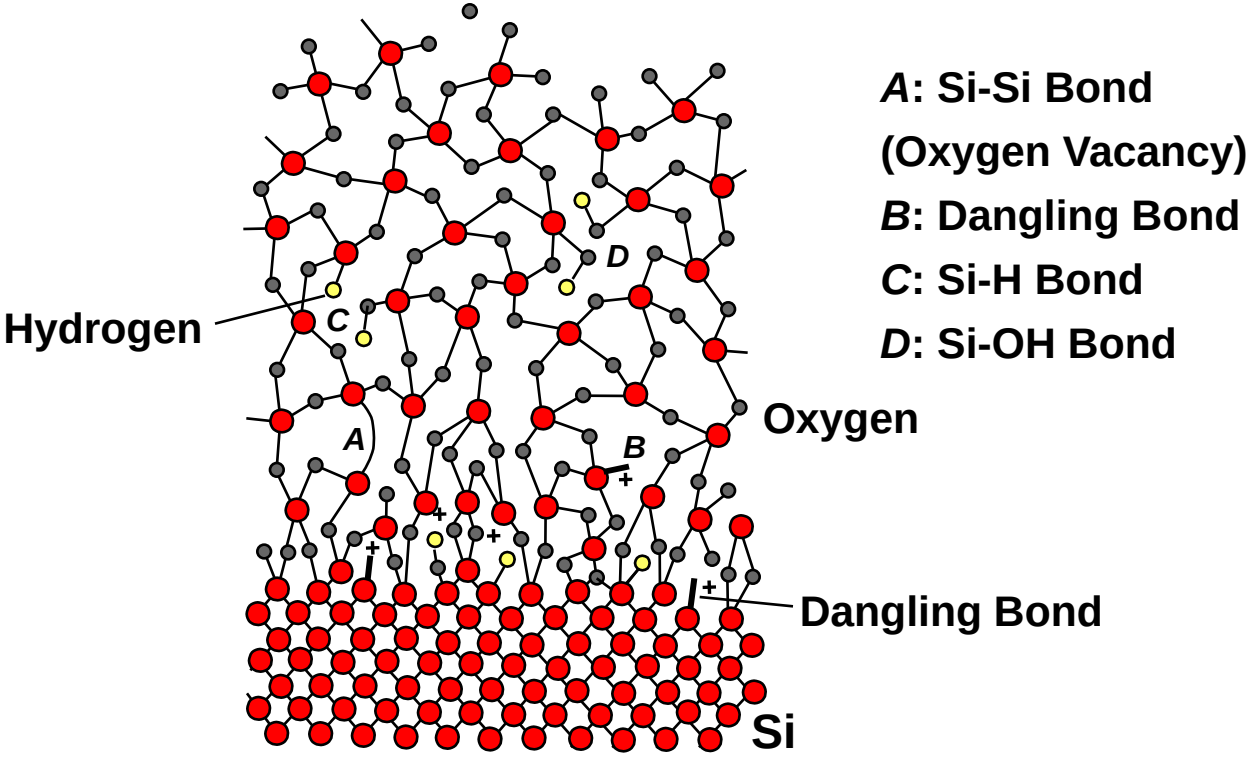
Slide after Dr. Oliver Brandt

Vertical multi-gate structures take us back to JFET like structures but now with the advantage of insulators. – Life is circular



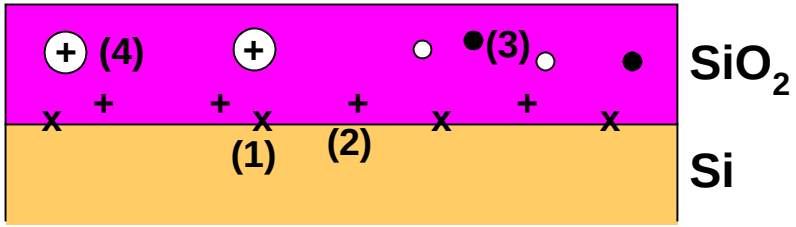
SiO_2 and SiO_2/Si Interface

- Si, Si/SiO_2 interface, SiO_2 bulk, and oxide defect structure



Oxide Charges / Interface Traps

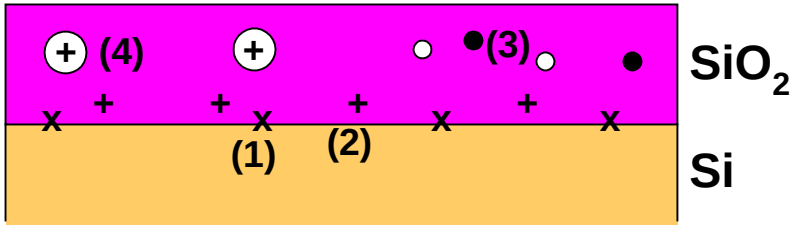
$Q=CV$



Charge	Type	Location	Cause	Effect on Device
1) D_{it}(cm^{-2} eV^{-1}), N_{it} (cm^{-2}), Q_{it} (C/cm^2)	Interface Trapped Charge	SiO_2/Si interface	Dangling Bond, Hot electron damage, contaminants	Junction Leakage Current, Noise, Threshold Voltage Shift, Subthreshold Slope
2) N_f, Q_f (cm^{-2}, C/cm^2)	Fixed Charge	Close to SiO_2/Si interface	Si^+ (?)	Threshold Voltage Shift
3) N_{ot}, Q_{ot} (cm^{-2}, C/cm^2)	Oxide Trapped Charge	In SiO_2	Trapped electrons and holes	Threshold Voltage Shift
4) N_m, Q_m (cm^{-2}, C/cm^2)	Mobile Charge	In SiO_2	Na, K, Li	Threshold Voltage Shift (time dependent)

1) Interface Trapped Charges

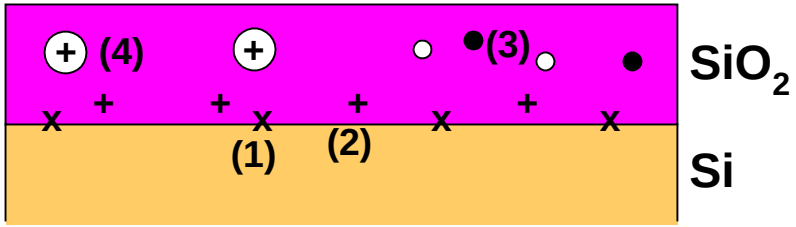
Q=CV



- Can be either positive or negative charge
- Due to:
  - Structural Defects
  - Oxidation Induced Defects
  - Metallic Impurities
  - Radiation induced broken bonds
  - Radiation induced broken bonds
- Can be drastically improved by a low temperature (~450 C) anneal in a Hydrogen bearing gas.

2) Fixed Oxide Charges

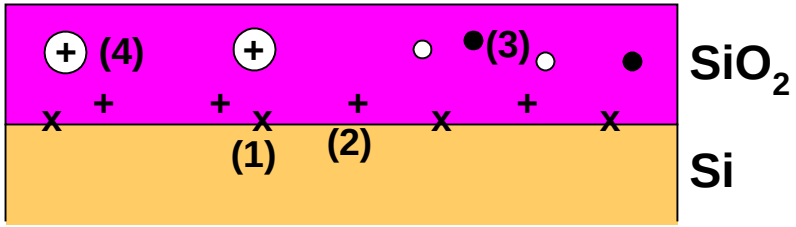
Q=CV



- Generally positive charge and is related to oxidation conditions:
  - Increases with decreasing oxidation temperature
  - Can be reduced to a fixed (minimum value) by anneals in inert gases
  - Can be effected by rapid cooling

3) Oxide Trapped Charges

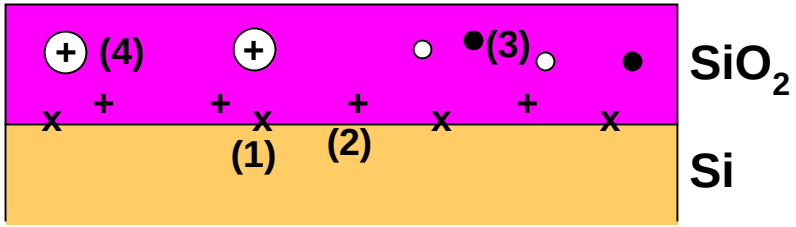
Q=CV



- Can be either positive or negative charge
- Due to electrons or holes trapped in the oxide:
  - Ionizing radiation (~>9 eV)
  - Tunnel currents
  - Breakdown

4) Mobile Charges

Q=CV



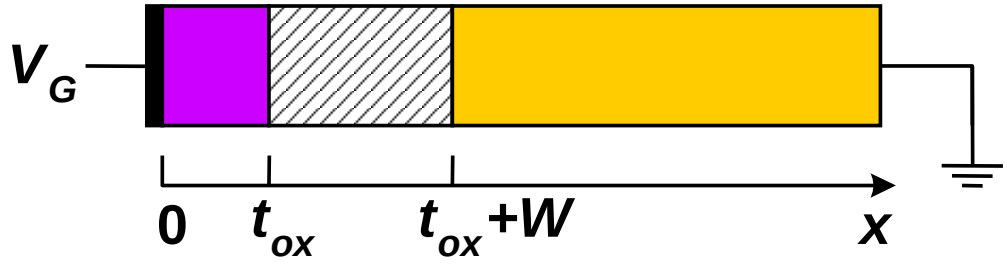
- Generally positive (sometimes negative but generally limited mobility if negative)
- Due to contaminants (Na, K, Li) in the oxide:
  - Gate voltage slowly drives the charge across the oxide changing the threshold voltage and capacitance characteristics
  - Can lead to hysteresis in the CV curve
  - Can lead to time dependent threshold voltages

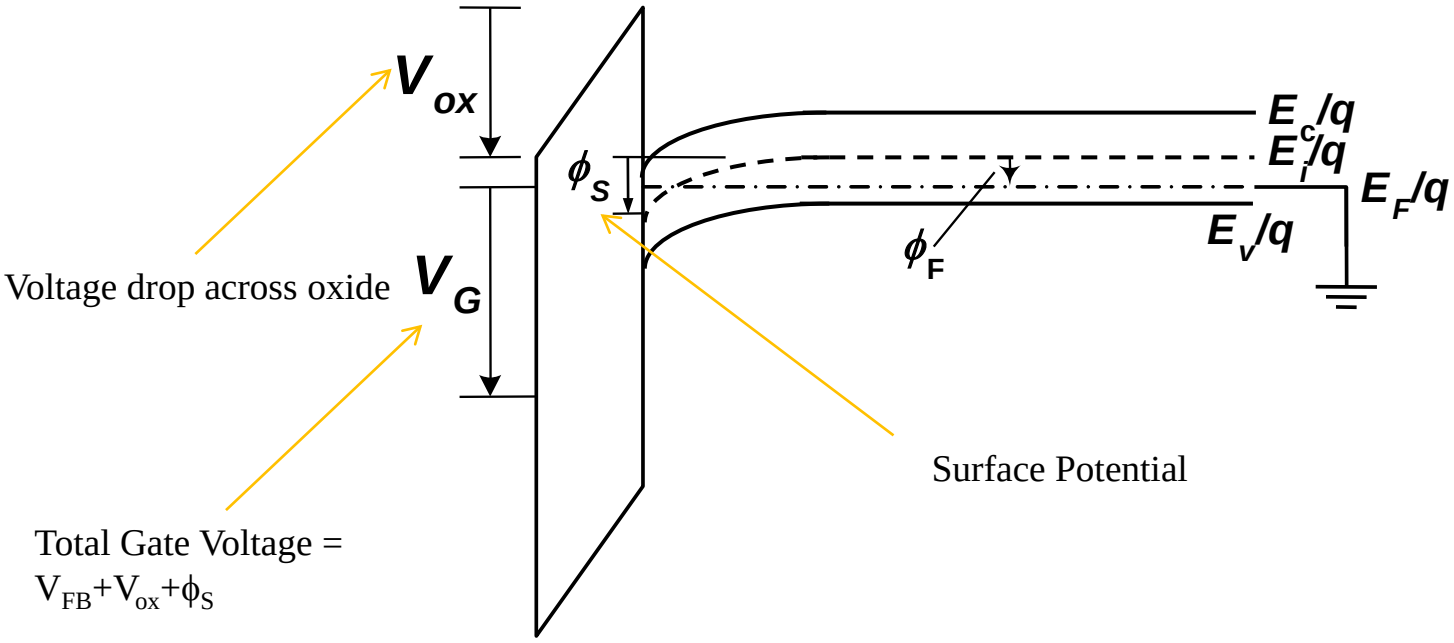
MOS Capacitor

- MOS Capacitor (MOS-C) can be used to determine
  - Oxide charge
  - Interface trapped charge
  - Oxide thickness
  - Flatband voltage
  - Threshold voltage
  - Substrate doping density
  - Generation lifetime
  - Recombination lifetime

MOS Capacitor

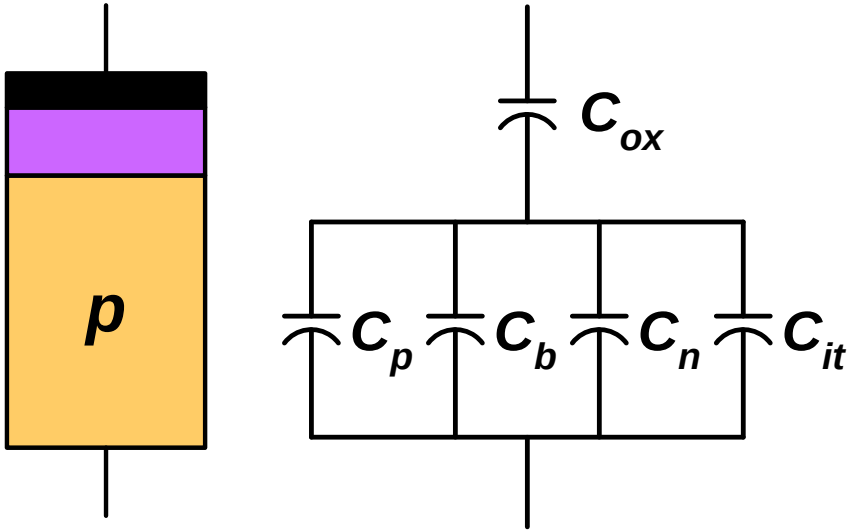
- MOS capacitor cross section and band diagram





MOS Capacitor

- Capacitance consists of
  - C_{ox}: oxide capacitance
  - C_p: accumulation capacitance
  - C_b: bulk (space-charge region) capacitance
  - C_n: inversion capacitance
  - C_{it}: interface trap capacitance
- Is generally given in units of Farads/cm^2



MOS Capacitor

- The capacitance is

$$C = \frac{dQ_G}{dV_G}$$

- The charge is

Assuming no oxide charge, gate charge = (-) semiconductor and interface charge

$$Q_G = -Q_s - Q_{it} = -(Q_p + Q_b + Q_n + Q_{it})$$

Hole, space charge, electron, and interface charge densities.

- This gives

$$C = \frac{dQ_G}{dV_G} = -\frac{dQ_s + dQ_{it}}{dV_G} = -\frac{dQ_s + dQ_{it}}{dV_{ox} + d\phi_s}$$

Because V_{FB} is fixed

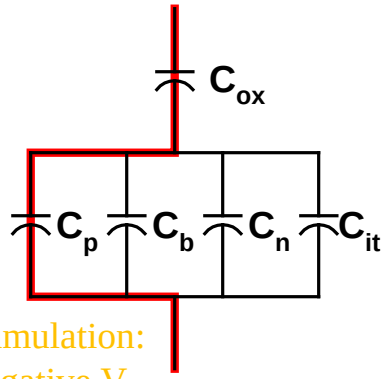
Math

$$C = -\frac{1}{\frac{dV_{ox}}{dQ_s + dQ_{it}} + \frac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}}$$

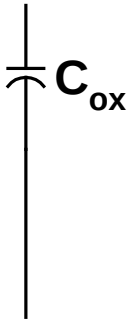
$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_p + C_b + C_n + C_{it}}}$$

MOS Capacitance

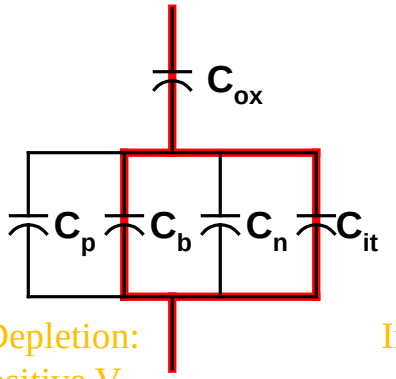
- **Accumulation**
  - $C_p >> C_{ox} \rightarrow C_{Total} \sim C_{ox}$
- **Depletion**
  - $C_b \approx < C_{ox} \approx > C_{it} \rightarrow C_{Total} < C_{ox}$
- **Inversion – *low frequency***
  - $C_n >> C_{ox} \rightarrow C_{Total} \sim C_{ox}$
- **Inversion – *high frequency***
  - $C_b \approx C_{ox} \rightarrow C_{Total} < C_{ox}$



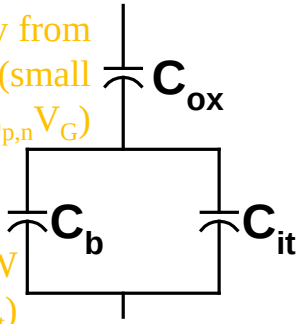
Accumulation: Negative V_G draws holes toward interface (Large $Q_p=C_pV_G$)



Accumulation

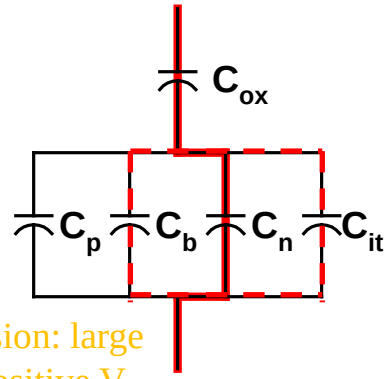


Depletion: Positive V_G pushes holes away from interface (small $Q_{p,n}=C_{p,n}V_G$)

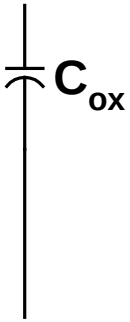


$Q_b=-qN_AW$ ($C_b>>C_{it}$)

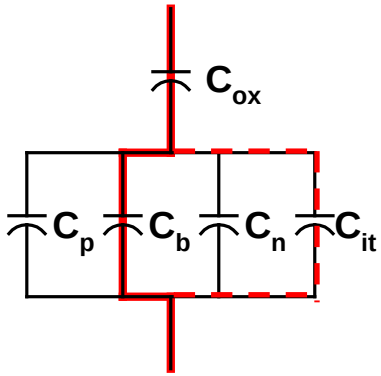
Depletion



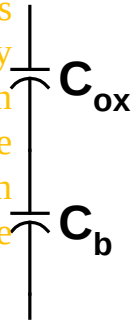
Inversion: large Positive V_G inverts surface region (Large $Q_n=C_nV_G$ dominates over C_b and C_{it})



Inversion - lf



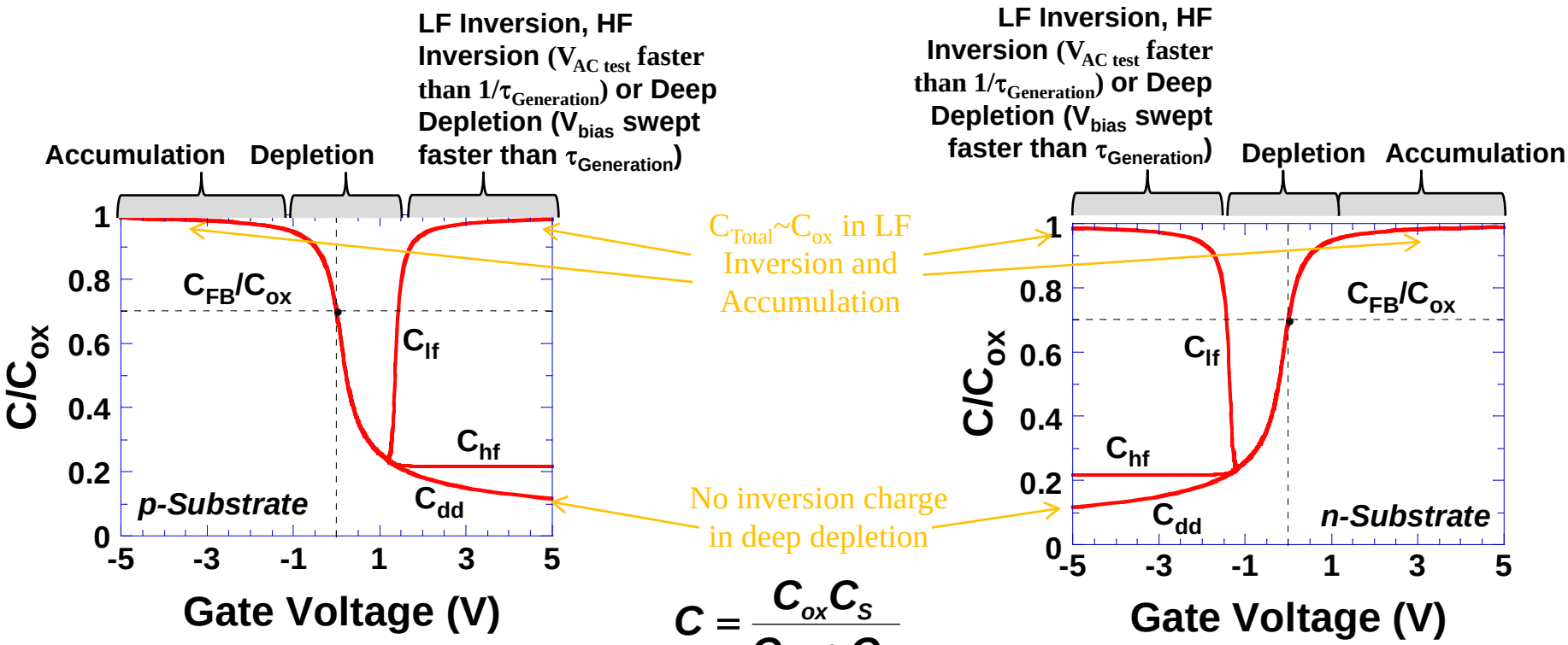
HF: When excitation is significantly faster than the generation lifetime



Inversion - hf

MOS Capacitance

- **Accumulation**
  - $C_p >> C_{ox} \rightarrow C_{Total} \sim C_{ox}$
- **Depletion**
  - $C_b \approx < C_{ox} \approx > C_{it} \rightarrow C_{Total} < C_{ox}$
- **Inversion – *low frequency***
  - $C_n >> C_{ox} \rightarrow C_{Total} \sim C_{ox}$
- **Inversion – *high frequency***
  - $C_b \approx C_{ox} \rightarrow C_{Total} < C_{ox}$



$$C = \frac{C_{ox} C_S}{C_{ox} + C_S}$$

MOS Capacitance – Generally Complex Mathematics

$$C_{S,lf} = \hat{U}_S \frac{K_s \varepsilon_0}{2L_{Di}} \frac{\left[e^{U_F}\left(1-e^{-U_S}\right)+e^{-U_F}\left(e^{U_S}-1\right)\right]}{F\left(U_S,U_F\right)}$$

$$\hat{U}_S = \frac{|U_S|}{U_S};\ U_S = \frac{\phi_s}{kT/q};\ L_{Di} = \sqrt{\frac{K_s \varepsilon_0 kT}{2q^2 n_i}}$$

$$F\left(U_S,U_F\right) = \sqrt{e^{U_F}\left(e^{-U_S}+U_S-1\right)+e^{-U_F}\left(e^{U_S}-U_S-1\right)}$$

$$C_{S,hf} = \hat{U}_S \frac{K_s \varepsilon_0}{2L_{Di}} \frac{\left[e^{U_F}\left(1-e^{-U_S}\right)+e^{-U_F}\left(e^{U_S}-1\right)/(1+\delta)\right]}{F\left(U_S,U_F\right)}$$

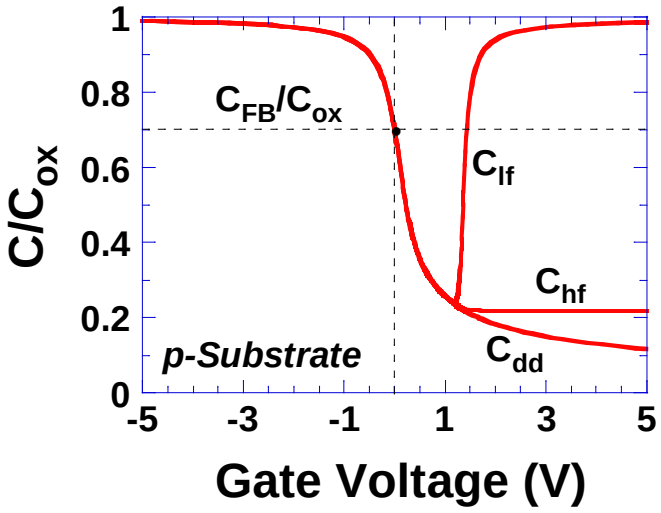
$$\delta = \frac{\left(e^{U_S}-U_S-1\right)/F\left(U_S,U_F\right)}{\int_0^{U_S} \frac{e^{U_F}\left(1-e^{-U}\right)\left(e^{U}-U-1\right)}{2\left[F\left(U_S,U_F\right)\right]^3} dU}$$

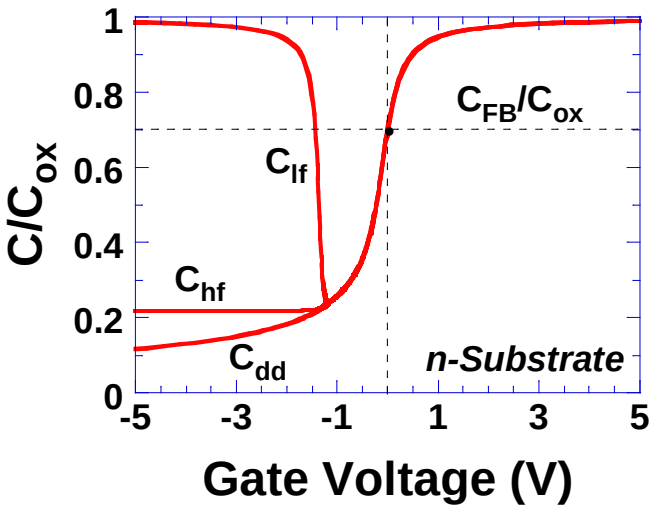
$$C_{S,dd} = \frac{C_{ox}}{\sqrt{\left[1+2\left(V_G-V_{FB}\right)/V_0\right]}-1}$$

MOS Capacitance

$$C = \frac{C_{ox}C_S}{C_{ox} + C_S}$$

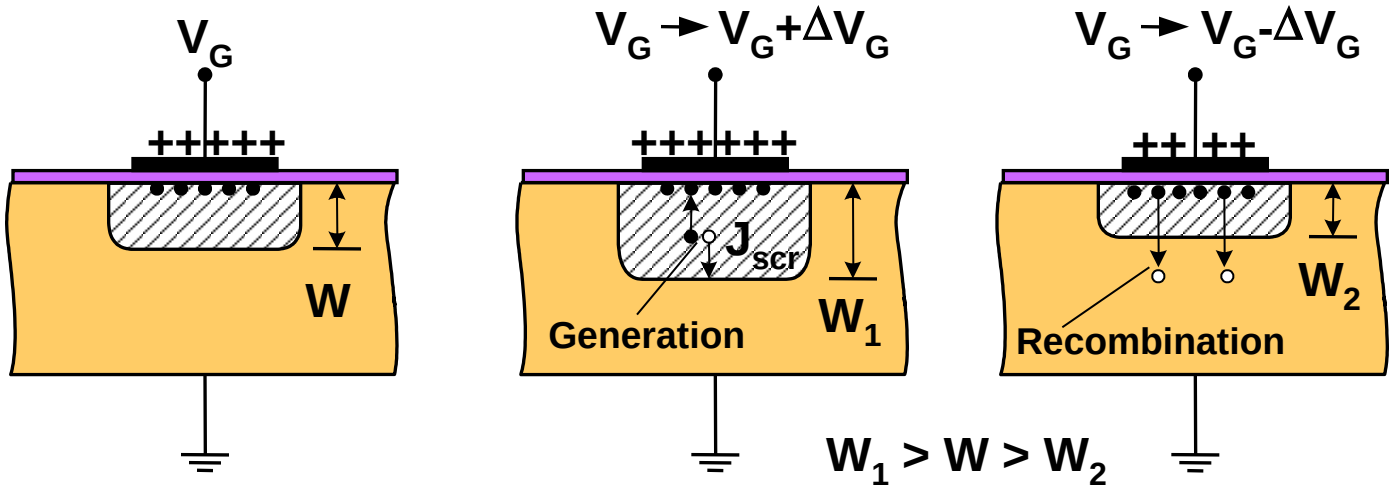
$$V_G = V_{FB} + \phi_S + V_{ox} = V_{FB} + \phi_S + \hat{U}_S \frac{kTK_s t_{ox} F(U_S, U_F)}{qK_{ox} L_{Di}}$$





Low-Frequency Capacitance

- To measure the low-frequency *C-V*$_G$ curve, the inversion carriers must be able to respond to both the ac gate voltage and the dc gate voltage sweep rate
- + ½ Cycle of V_G: Driven displacement current (gate) must be less than the available space charge (generation) current
- - ½ Cycle of V_G: Recombination is fast enough to not be an issue



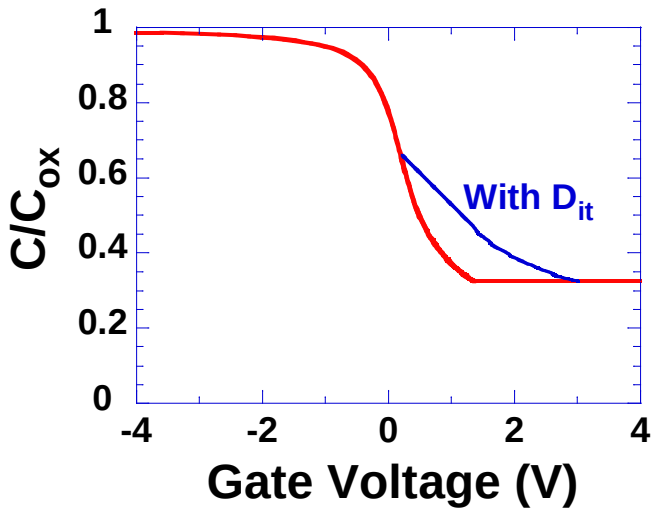
$$J_{scr} = \frac{qn_iW}{\tau_g} \qquad J_{displ} = C_{ox}\frac{dV_G}{dt} \Rightarrow \frac{dV_G}{dt} \le \frac{qn_iW}{\tau_g C_{ox}} = \frac{0.046Wt_{ox}}{\tau_g}\ V/s \qquad f_{eff} = \frac{1}{v_g}\frac{dV_G}{dt}$$

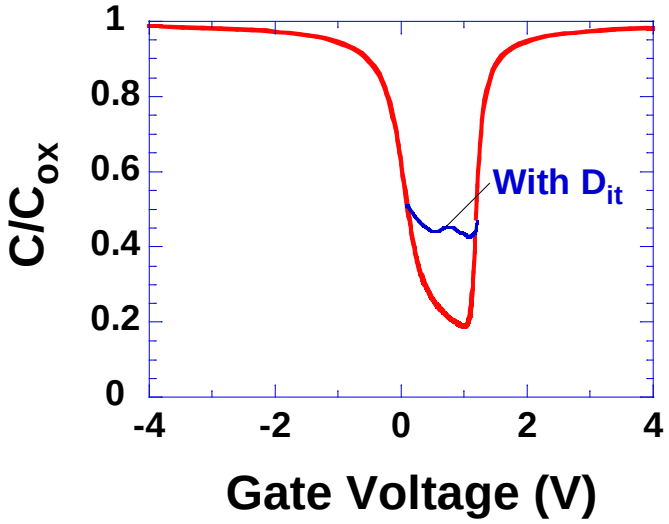
in μm, in nm, in μs

Low-Frequency Capacitance

- The effective frequency is < 1 Hz
  - Very difficult to measure the capacitance
  - Measure current

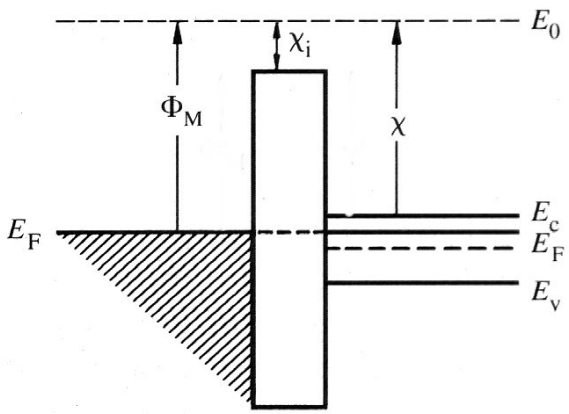
$$I = \frac{dQ}{dt} = \frac{dQ}{dV_G}\frac{dV_G}{dt} = C\frac{dV_G}{dt} \quad or \quad I \sim C$$

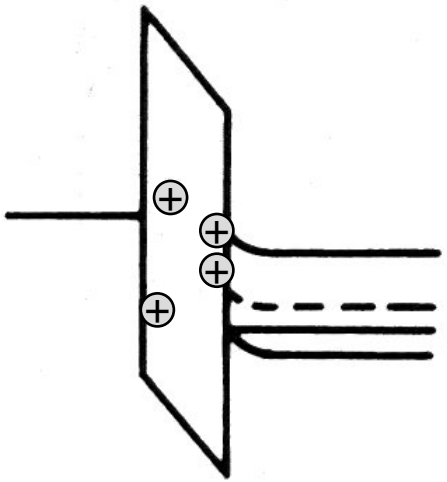




Flatband Voltage (and Capacitance)

- Most Junior level classes assume:
  - A metal can be selected that aligns perfectly with the fermi-level in the semiconductor
  - No charges exist in the Oxide
- These are generally not true (once again, we lied to you), leading to a "pre-bias" on the device
- This shifts the CV Curve and requires a voltage be applied to obtain "flat band" conditions.
- To determine V_{FB}, one must compare the measured to theoretical CV curves and thus must know the theoretical flatband capacitance

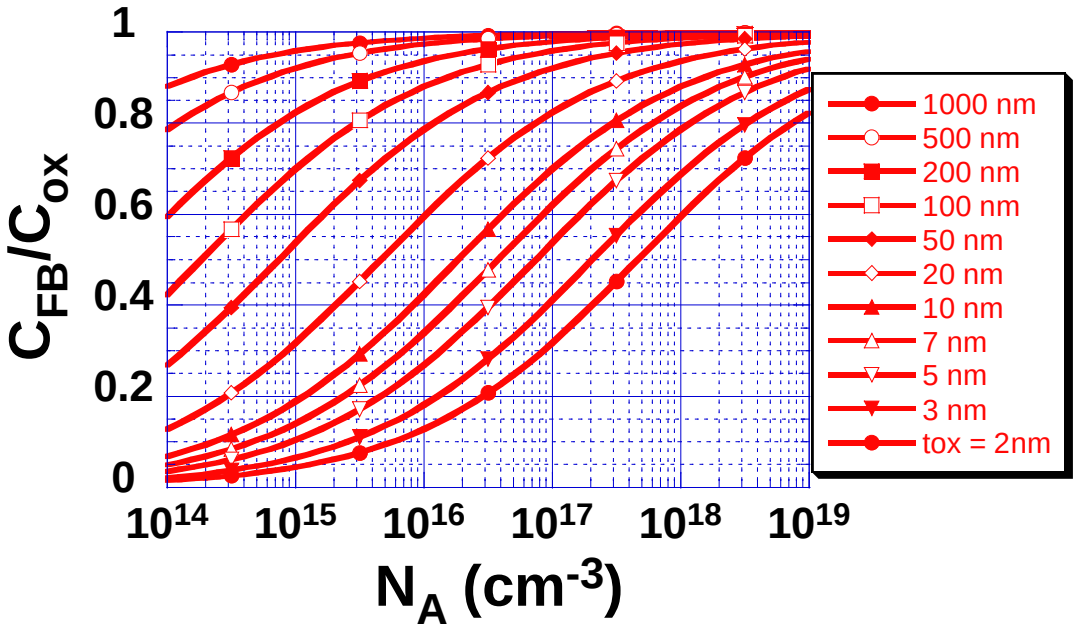




Flatband Capacitance

- The flatband voltage is that gate voltage at which the capacitance is the flatband capacitance

$$C_{FB} = \frac{C_{ox}C_{S,FB}}{C_{ox} + C_{S,FB}}; \quad C_{S,FB} = \frac{K_S\varepsilon_0}{L_D}; \quad L_D = \sqrt{\frac{K_S\varepsilon_0 kT}{q^2(p+n)}} \approx \sqrt{\frac{K_S\varepsilon_0 kT}{q^2 N_A}}$$

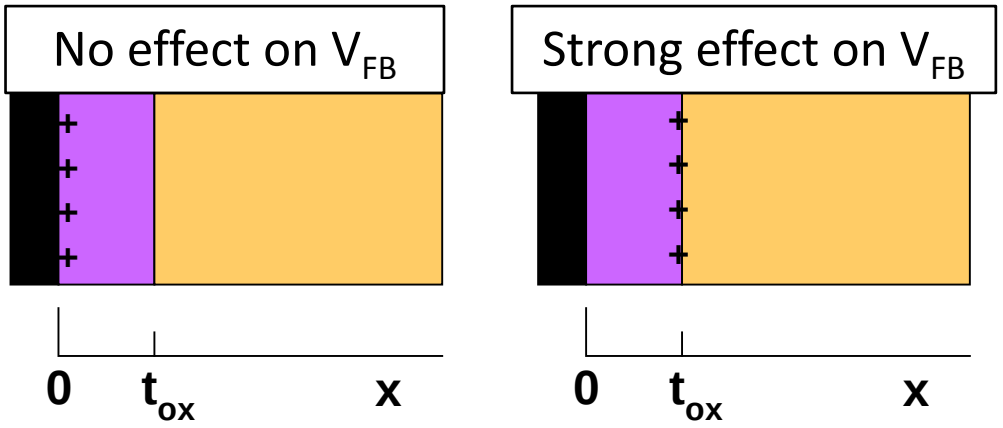


Flatband Voltage

- **Flatband voltage depends on various gate, semiconductor, and oxide parameters**

$$V_{FB} = \phi_{MS} - \left[\frac{Q_f}{C_{ox}}\right] - \left[\frac{1}{C_{ox}}\int_0^{t_{ox}} (x/t_{ox})\rho_{Mobile}(x)dx\right] - \left[\frac{1}{C_{ox}}\int_0^{t_{ox}} (x/t_{ox})\rho_{OxideTrapped}(x)dx\right] - \left[\frac{Q_{it}(\phi_S)}{C_{ox}}\right]$$

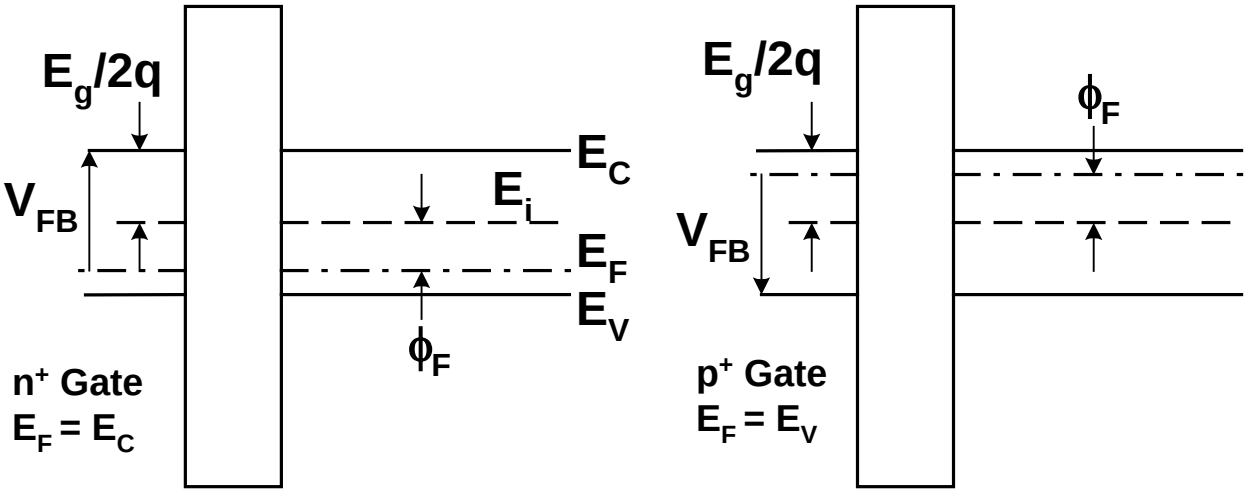
Weighted sum (integral) accounts for how far away the charge is from the oxide-semiconductor interface.



Work Function Difference

- The work function difference, ϕ_{MS}, depends on the Fermi level of the gate (polysilicon) and the substrate
- Assuming the gate is degenerately doped (i.e. fermi level is in the majority carrier band…

$$\phi_{MS} = \phi_M - \phi_S = \phi_F(gate) - \phi_F(substrate)$$

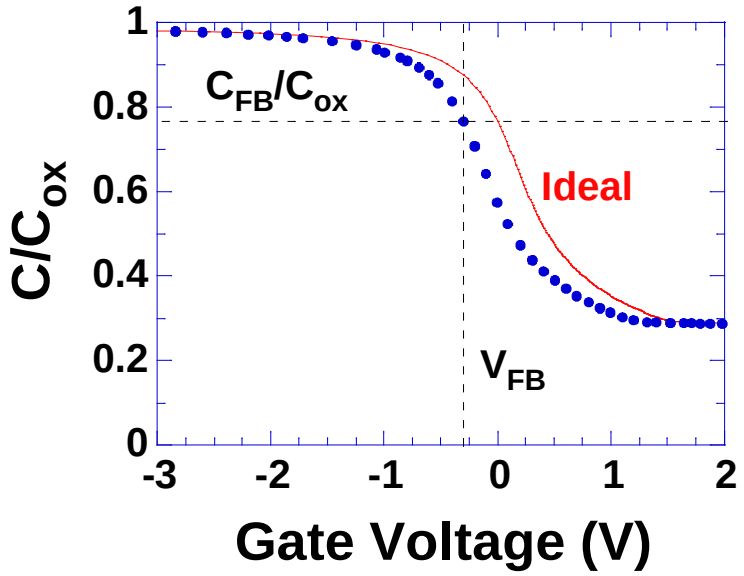


Q_f, ϕ_{MS} Measurements

- Assume $Q_m = Q_{ot} = Q_{it} = 0$

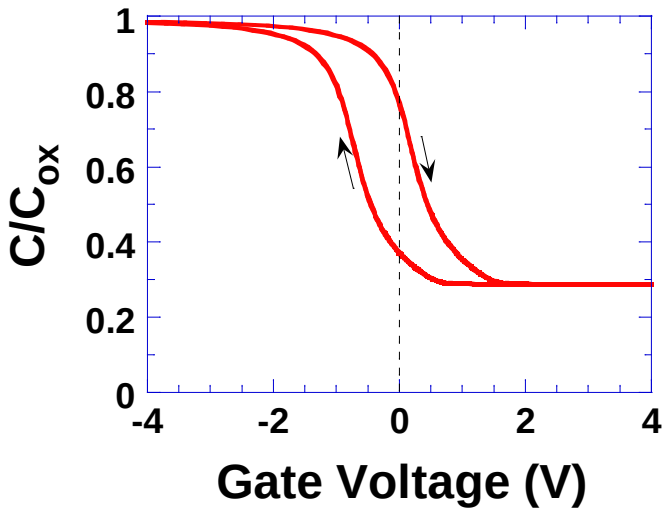
$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} = \phi_{MS} - \frac{qN_f}{K_{ox}\varepsilon_0} t_{ox}$$

- Measure and plot V_{FB} versus t_{ox}



Mobile Charge

- Bia[illegible]-temperature stress (BTS)
  - [illegible]ly positive gate voltage to produce $\mathcal{E}_{ox} \approx 10^6$ V/cm at [illegible]0 °C for t = 5-10 min. Cool device with applied [illegible], measure C-V_G at room temperature
  - [illegible]t with negative gate voltage
  - The [illegible]te voltage shift, ΔV_{FB}, between the two curves is due to mobile charge



$$Q_m = -\Delta V_{FB} C_{ox}$$

Mobile Charge

- **Triangular voltage sweep**
  - **MOS-C is held at T = 200-300°C**
  - **High-frequency C - V_G and low-frequency I - V_G measured**

$$I = \frac{dQ_G}{dt}$$

$$I = C_{lf}\left(\alpha - \frac{dV_{FB}}{dt}\right)$$

$$\int_{-V_{G1}}^{V_{G1}} \left(\frac{I}{C_{lf}} - \alpha\right) dV_G = -\alpha\left\{V_{FB}\left[t\left(V_{G2}\right)\right] - V_{FB}\left[t\left(-V_{G1}\right)\right]\right\}$$

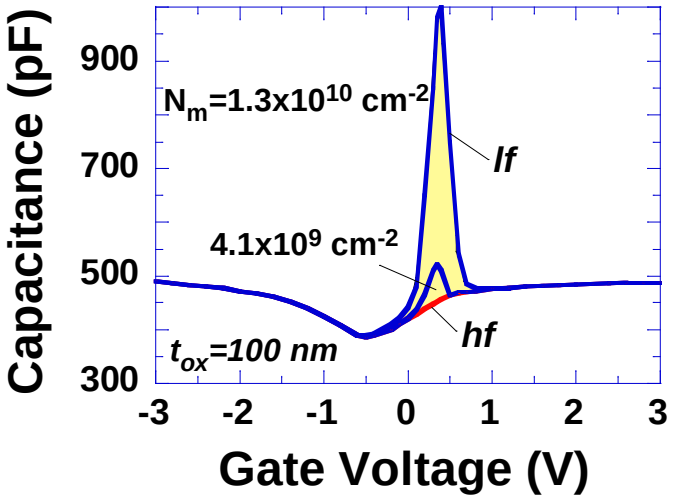
$$-\alpha\left\{V_{FB}\left[t\left(V_{G2}\right)\right] - V_{FB}\left[t\left(-V_{G1}\right)\right]\right\} = \alpha\frac{Q_m}{C_{ox}}$$

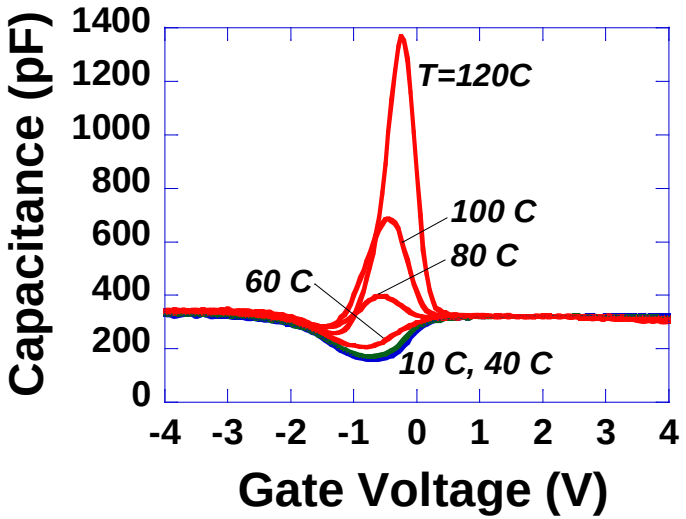
$$\int_{-V_{G1}}^{V_{G1}} \left(\frac{I}{C_{lf}} - \alpha\right) C_{ox}\, dV_G = -\alpha Q_m$$

Mobile Charge

Triangular Voltage Sweep (TVS)

- Measure *hf* and *lf* C-V_G curves simultaneously at $T \approx 200°C$
- Q_m = area between *lf* and *hf* curves
- Suitable for gate oxides and interlevel dielectrics





$$Q_m = \int_{-V_{G1}}^{V_{G2}} (C_{lf} - C_{hf}) dV_G$$

Interface Trapped Charge

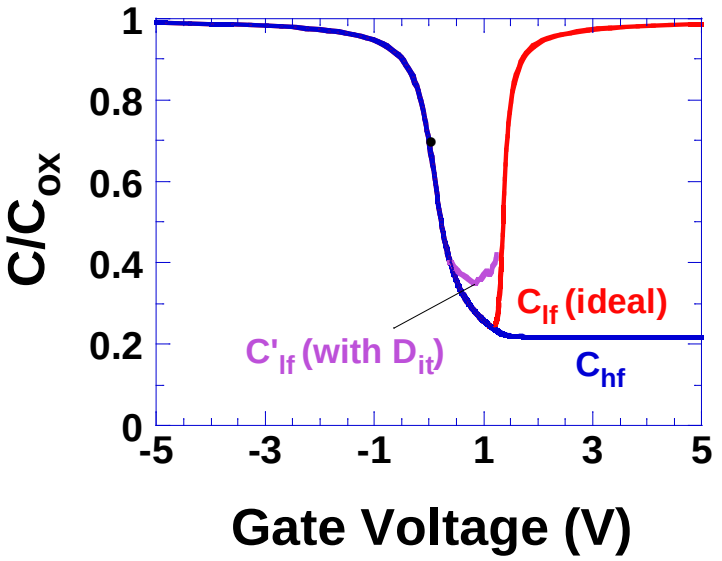
- **Quasi-static method**
  - **High-frequency and low-frequency *C*-V_G curves are measured**

$$C_{lf} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_S + C_{it}}}$$

$$D_{it} = \frac{C_{it}}{q^2} = \frac{1}{q^2}\left(\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - C_S\right)$$

$$\phi_s = \int_{V_{G1}}^{V_{G2}} \left(1 - \frac{C_{lf}}{C_{ox}}\right) dV_G + \Delta$$

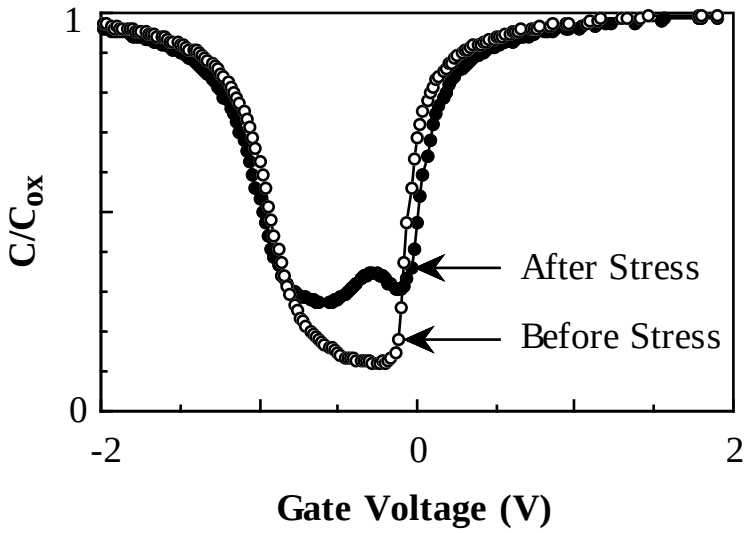
$$C_S = \frac{C_{ox}C_{hf}}{C_{ox} - C_{hf}}$$

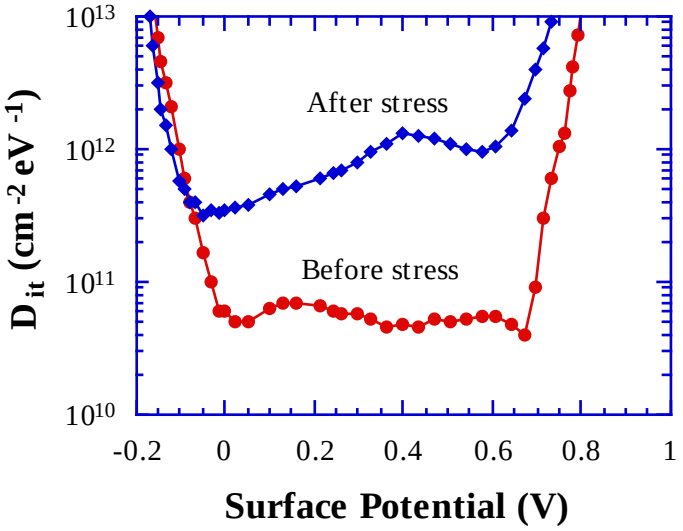


$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right)$$

Quasistatic Method

- Current flow through oxide causes
  - Interface state generation
  - Oxide charge trappping

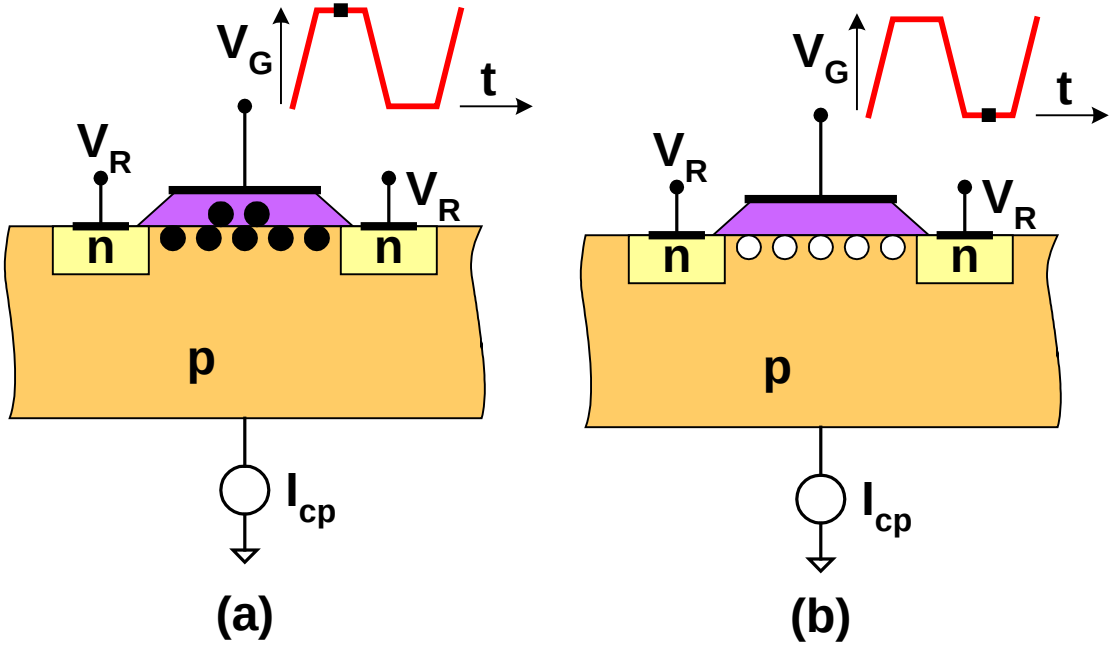




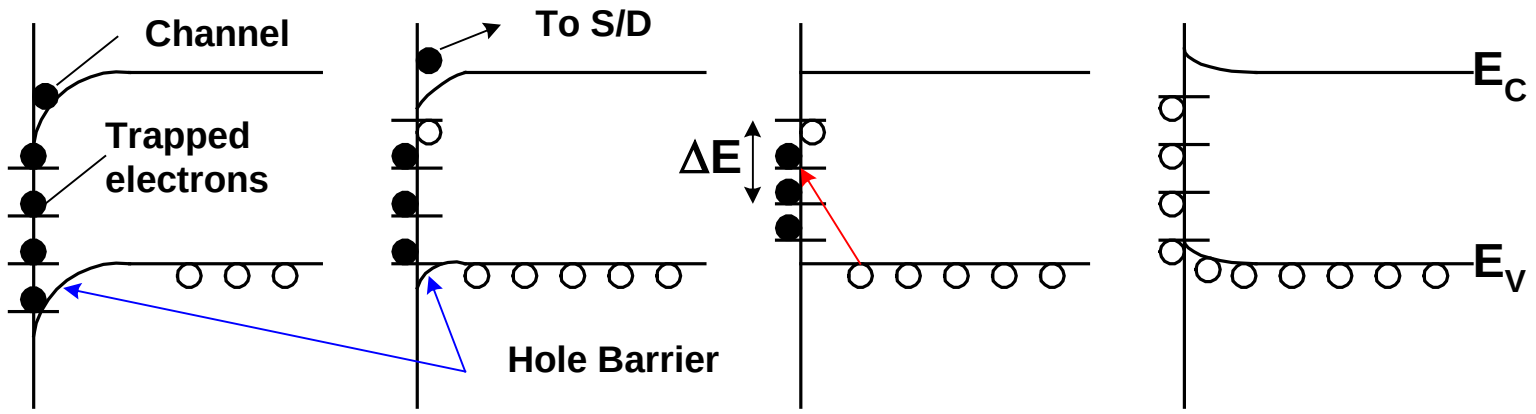
Data courtesy of W. Weishaar, Arizona State University

Interface Trapped Charge

- Charge Pumping
  - Uses MOSFET
  - Apply periodically varying gate voltage
  - Measure resulting current at the substrate or source/drain



Charge Pumping



$$\tau_e = \frac{\exp((E_C - E_1)/kT)}{\sigma_n v_{th} N_C} \qquad \tau_c = \frac{1}{\sigma_p v_{th} p_s}$$

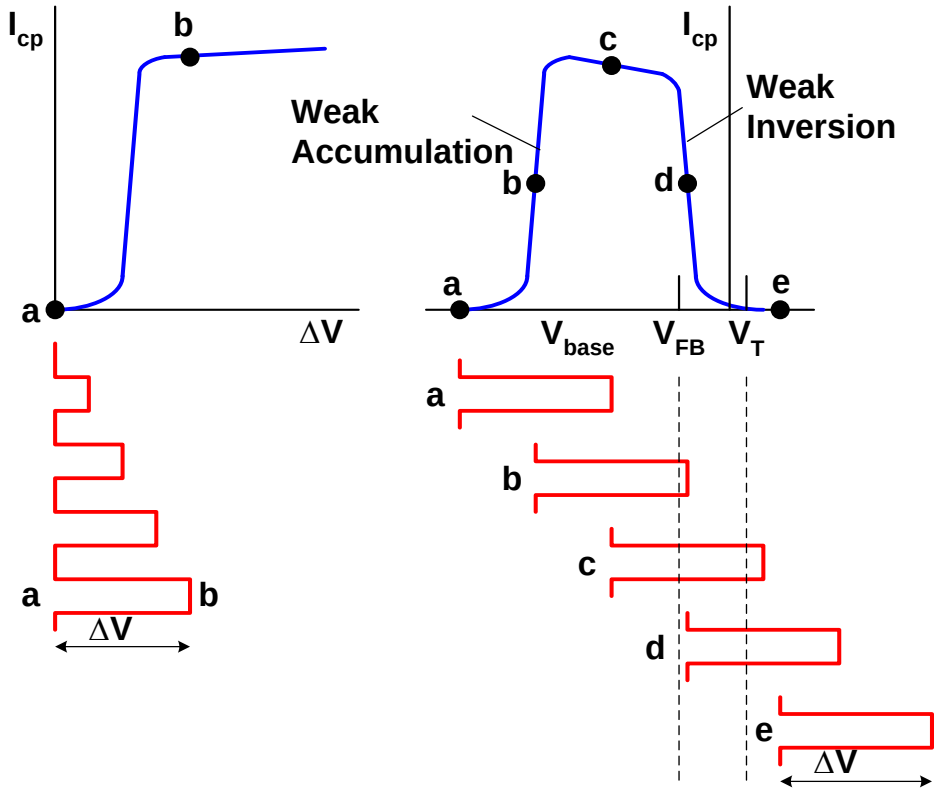
$$E_C - E_1 = kT \ln\left(\frac{\sigma_n v_{th} N_C}{2f}\right) \qquad E_2 - E_V = kT \ln\left(\frac{\sigma_p v_{th} N_V}{2f}\right)$$

$$\Delta E \approx E_g - kT\left(\ln\left(\frac{\sigma_n v_{th} N_C}{2f}\right) + \ln\left(\frac{\sigma_p v_{th} N_V}{2f}\right)\right)$$

$$I_{cp} = A_G f\left[qD_{it}\Delta E + \alpha C_{ox}\left(V_G - V_T\right)\right]$$

Charge Pumping

- Bilevel
  - Keep baseline constant, vary pulse height
  - Vary baseline, keep pulse height constant



MOSFET Subthreshold I_D - V_G

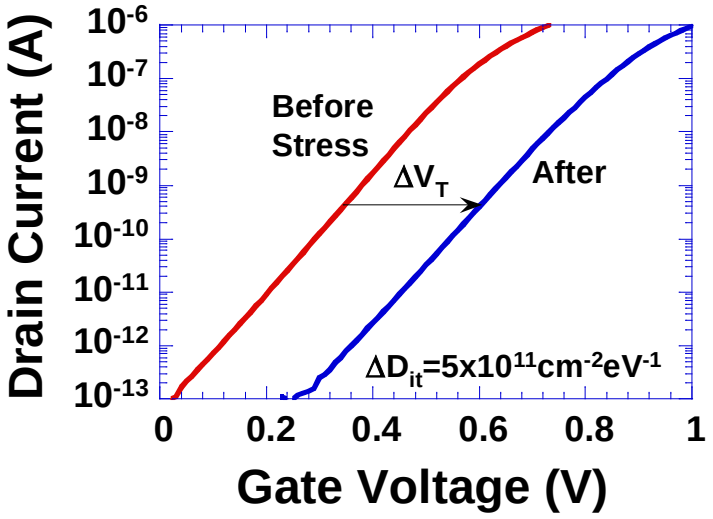
- Below V_T, I_D depends exponentially on V_G
- Slope change due to stress is very small for thin oxides

$$I_D = I_o e^{q(V_G - V_T)/nkT}$$

$$n = 1 + \frac{C_s + q^2 D_{it}}{C_{ox}}$$

$$= 1 + \frac{q(N_A W + qD_{it})}{K_{ox}\varepsilon_o} t_{ox}$$

$$= 1 + 4.65x10^{-7}(N_A W + D_{it})t_{ox}$$



$$\Delta D_{it} = \frac{C_{ox}}{2.3kT}\left(\frac{1}{Slope\ After} - \frac{1}{Slope\ Before}\right)$$

Review Questions

- Name the four main charges in the oxide
- How is the low-frequency capacitance measured?
- What is the flatband voltage and flatband capacitance?
- Describe charge pumping.
- How does the subthreshold slope yield the interface trap density?