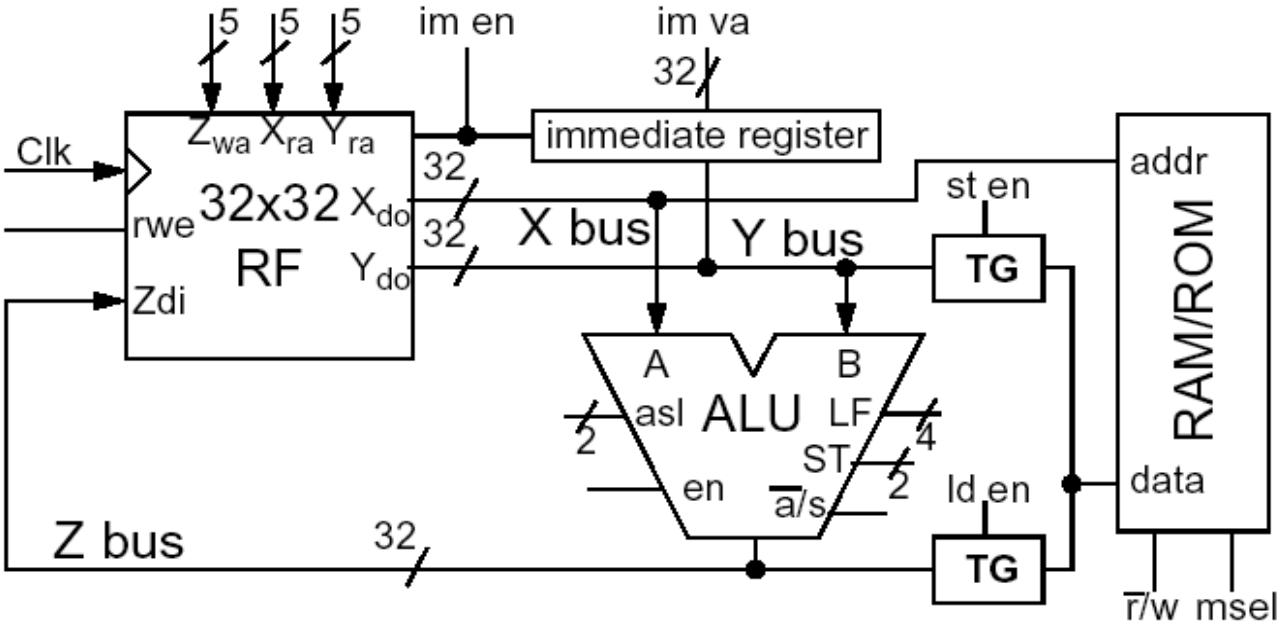
ECE2030b- HW-7 Due Monday Nov. 11, 2002 – CPU Control Lines - Microcode



Show how the control lines are set to achieve the operations below. Assume msel = 1;

asl: 0=AU, 1=LU, 2=SU, 3 = invalid; ST: 0=arithmetic, 1=logical, 2=rotate, 3 = invalid;

LF: 0=AND, 1=OR, 2=XOR, 3 = invalid; a'/s: 0=add, 1= subtract rwe: 1=write, 0= do not write

Add $5 to the value in $2 and put the result into memory (address=$9)

M[$9] = $5 + $2

(note: loading or storing data requires a separate CPU clock cycle - $9 means the value presently in R9)

Mem r'/w	X	Y	Z	rwe	asl	a'/s	en	ld en	st en	im en	im va (Immediate Value)
-	*5*	*2*	*1**	*1*	*1*	*0*	*1*	*0*	*0*	*0*	-
1	9	1*	-	0	0	-	0	0	1	0	-

* can be any register except $0 or $9.