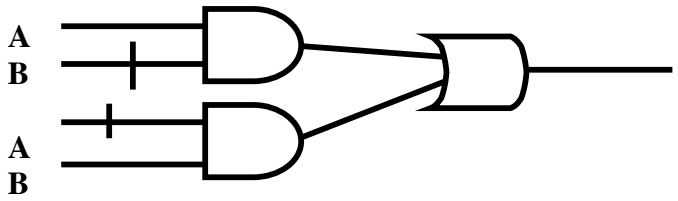
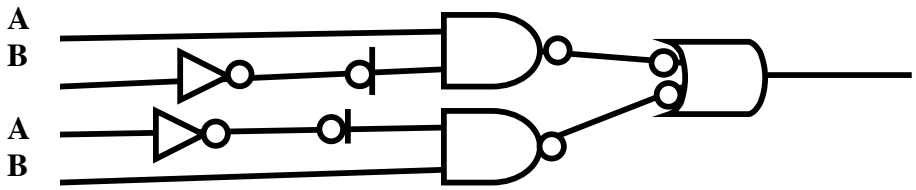
Problem 1. Design an XOR gate (AB' + A'B) using NAND gates and Inverters by the Mixed Logic Technique. Show the each stage separately. The procedure for performing mixed logic conversions is as follows:

1. Draw the logic network for the given Boolean equation using only AND and OR gates. Replace all complements with a bar (no bubbles or inverters yet!) Do not use XOR gates.



Once the initial Boolean equation is drawn with AND gates, OR gates and bars, the self-documenting redesign begins.

2. Add complement bubbles and NOT gates (inverters) within the network to appropriately convert logic gates to the desired gate sets.



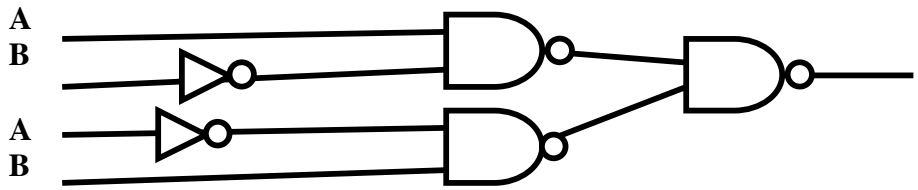
The rules in adding complement bubbles and NOT gates

a. All pairs of bubbles must cancel each other out.

b. Exactly one and only one bubble needed on each bar (which then can disappear).

c. Add a NOT gate and a bubble where needed to make bubbles cancel, or a bubble is needed to make a gate the desired type.

3. Replace DeMorgan equivalent gate symbols with standard gate symbols (e.g., NAND gates should be shown as an AND gate symbol with a "bubble" on the output instead of an OR gate symbol with bubbles on the inputs).



Problem 2. On a separate sheet of paper, design a XOR gate using only NOR gates and Inverters using the same steps as in problem 1.