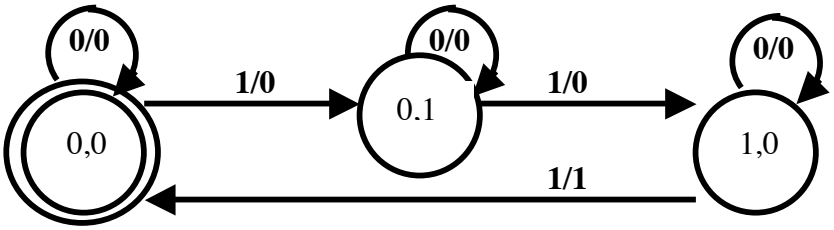
HW-7. Finite State Machine - Circuit Design

Design the logic to implement the following FSM. This is the state diagram for a Mealy machine with 3 states that outputs a "1" on every third "1" received as input, no matter how many "0"s are intermingled. For example:

```
Input:  0101101001011101101 0
Output: 0000100000010001000 10
```



This is the truth table for the logic that is needed. P1,P0 is the present state, Number the states such that 2*P1 + P0 is the number of 1's seen in the present sequence of 3. N1,N0 the next state.

P1	P0	Input		N1	N0	Output
0	0	0		**0**	**0**	**0**
0	0	1		**0**	**1**	**0**
0	1	0		**0**	**1**	**0**
0	1	1		**1**	**0**	**0**
1	0	0		**1**	**0**	**0**
1	0	1		**0**	**0**	**1**

_____ Answer _____

N1 = P1 • I' + P0 • I

Input (I) - P1,P0	00	01	11	10
0	0	0	x	1
1	0	1	x	0

N0 = P0 • I' + P1' • P0' • I

Input (I) - P1,P0	00	01	11	10
0	0	1	x	0
1	1	0	x	0

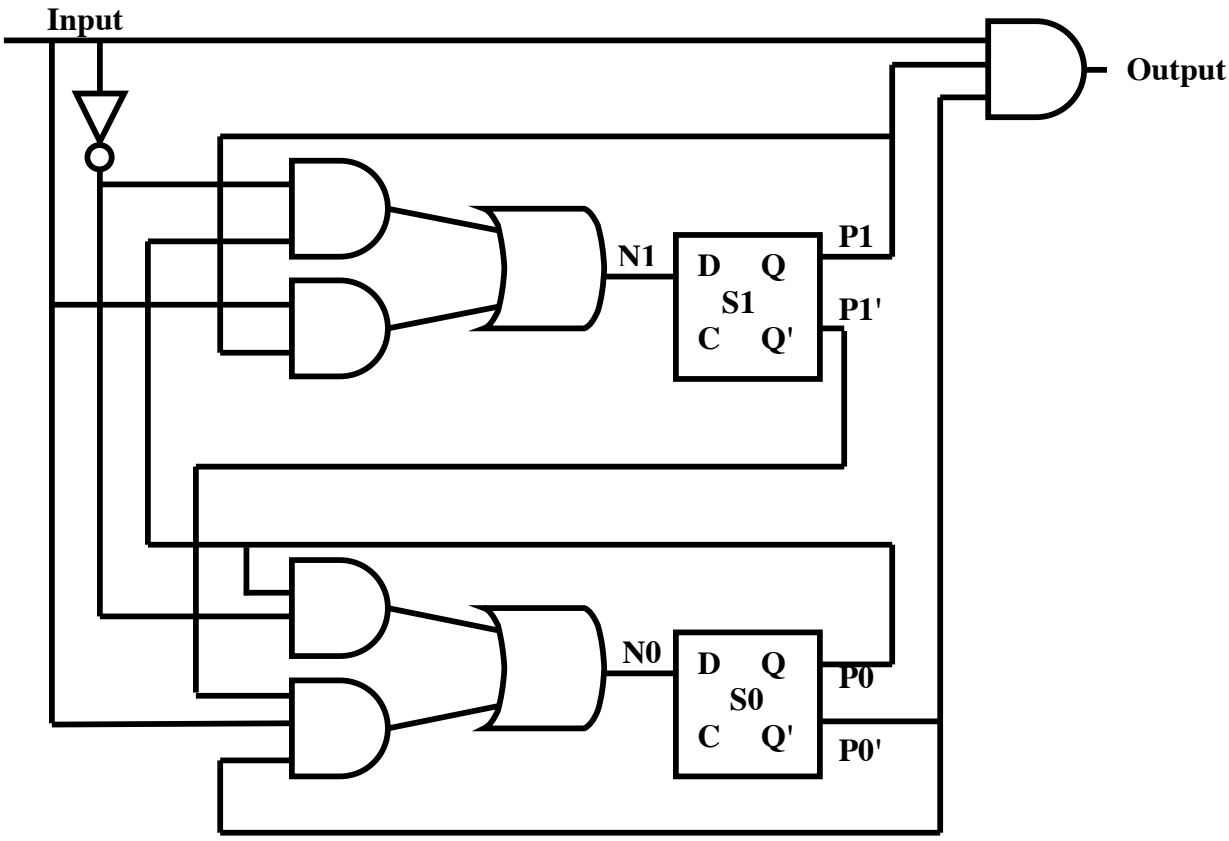
Output = P1 • P0' • I

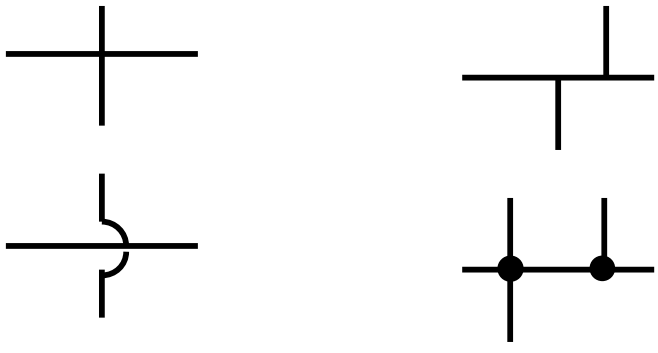
Input (I) - P1,P0	00	01	11	10
0	0	0	x	0
1	0	0	x	1

N1 = P1 • I' + P0 • I

N0 = P0 • I' + P1' • P0' • I

Output = P1 • P0' • I





Not-Connected Lines **Connected Lines**