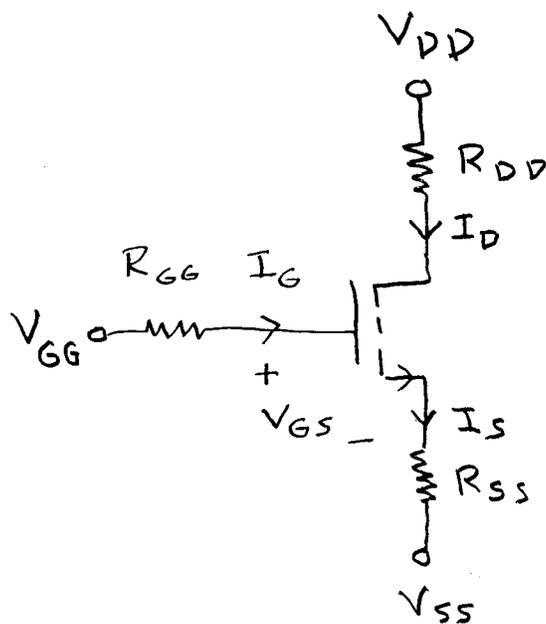


1-05/22/03

## The MOSFET Bias Equation

Replace the dc circuits looking out of the drain, gate, and source leads with Thévenin equivalents



The loop equation between the  $V_{GG}$  and  $V_{SS}$  nodes is

$$V_{GG} - V_{SS} = I_G R_{GG} + V_{GS} + I_S R_{SS}$$

But  $I_G = 0$  and  $I_S = I_D$

$$\Rightarrow V_{GG} - V_{SS} = V_{GS} + I_D R_{SS}$$

2-05/22/03

To solve for  $V_{GS}$ , we use the equation

$$I_D = K(V_{GS} - V_{T0})^2$$

$$\Rightarrow V_{GS} = \sqrt{\frac{I_D}{K}} + V_{T0}$$

$$\Rightarrow V_{GG} - V_{SS} = \sqrt{\frac{I_D}{K}} + V_{T0} + I_D R_{SS}$$

$$\Rightarrow I_D R_{SS} + \sqrt{\frac{I_D}{K}} + V_{T0} - (V_{GG} - V_{SS}) = 0$$

Let  $I_D = x^2$  and  $V_1 = V_{GG} - V_{SS} - V_{T0}$

$$\Rightarrow x^2 R_{SS} + \frac{1}{\sqrt{K}} x - V_1 = 0$$

This is a quadratic equation with the solution

$$x = \frac{1}{2R_{SS}} \left[ -\frac{1}{\sqrt{K}} + \sqrt{\frac{1}{K} + 4V_1 R_{SS}} \right]$$

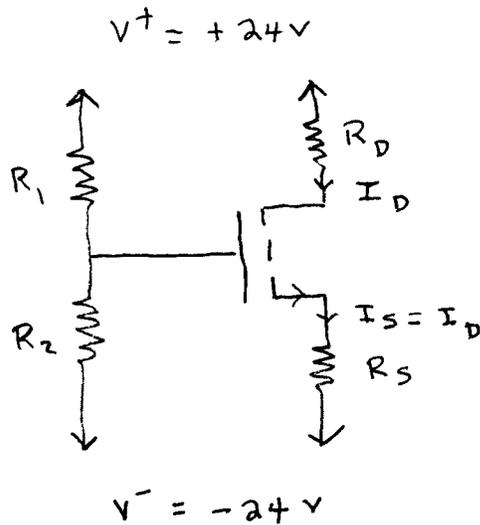
$$= \frac{1}{2R_{SS}\sqrt{K}} \left[ \sqrt{1 + 4KV_1 R_{SS}} - 1 \right]$$

$$= \sqrt{I_D}$$

3 - 05 / 22 / 03

$$\Rightarrow I_D = \frac{1}{4KR_{SS}^2} \left[ \sqrt{1 + 4KV_1 R_{SS}} - 1 \right]^2$$

Example 1



$$R_1 = 5 \text{ M}\Omega$$

$$R_2 = 2 \text{ M}\Omega$$

$$R_D = 10 \text{ k}\Omega$$

$$R_S = 3 \text{ k}\Omega$$

$$K = 0.001 \text{ A/V}^2$$

$$V_{T0} = 1.75 \text{ V}$$

Solve for  $I_D$

$$V_{GG} = V^+ \frac{R_2}{R_1 + R_2} + V^- \frac{R_1}{R_1 + R_2} = -16 \text{ V}$$

$$R_{GG} = R_1 \parallel R_2 = 1.43 \text{ M}\Omega$$

$$V_{SS} = V^- = -24 \text{ V}$$

$$R_{SS} = R_S = 3 \text{ k}\Omega$$

$$V_1 = V_{GG} - V_{SS} - V_{T0} = 6.25 \text{ V}$$

$$I_D = \frac{1}{4KR_S} \left[ \sqrt{1 + 4KV_1 R_S} - 1 \right]^2 = 1.655 \text{ mA}$$

4-05/22/03

For the MOSFET to be in the active mode,  $V_{DS} > V_{GS} - V_{T0}$

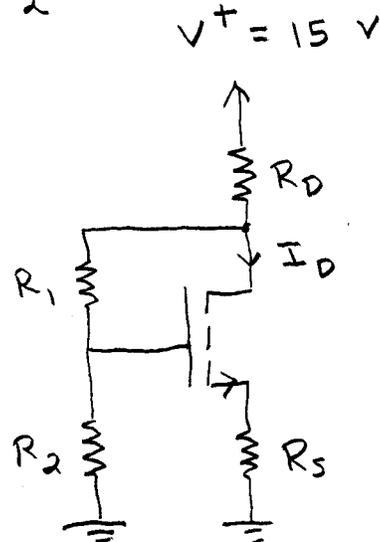
$$\begin{aligned} V_{GS} &= V_G - V_S = V_{GG} - (v^- + I_D R_S) \\ &= 3.036 \text{ V} \end{aligned}$$

$$V_{GS} - V_{T0} = 1.286 \text{ V}$$

$$\begin{aligned} V_{DS} &= (v^+ - I_D R_D) - (v^- + I_D R_S) \\ &= v^+ - v^- - I_D (R_D + R_S) \\ &= 26.49 \text{ V} \end{aligned}$$

$\Rightarrow V_{DS} > V_{GS} - V_{T0} \Rightarrow \text{Active Mode}$

Example 2



$$R_D = 2.5 \text{ k}\Omega$$

$$R_S = 1 \text{ k}\Omega$$

$$R_1 = 1 \text{ M}\Omega$$

$$R_2 = 1 \text{ M}\Omega$$

$$K = 0.001 \text{ A/V}^2$$

$$V_{T0} = 1.5 \text{ V}$$

5-05/22/03

$$V_{GG} = V + \frac{R_2}{R_D + R_1 + R_2} - I_D \frac{R_D}{R_D + R_1 + R_2}$$
$$= 7.491 - 1199 I_D$$

$$R_{SS} = R_S = 1 \text{ k}\Omega \quad V_{SS} = 0$$

From the derivation of the bias equation, we have

$$I_D R_{SS} + \sqrt{\frac{I_D}{K}} + V_{T0} - (V_{GG} - V_{SS}) = 0$$

$$\Rightarrow 2199 I_D + 31.62 \sqrt{I_D} - 5.991 = 0$$

$$\text{Let } I_D = x^2$$

$$\Rightarrow 2199 x^2 + 31.62 x - 5.991 = 0$$

$$\Rightarrow x = 0.04550$$

$$\Rightarrow I_D = x^2 = 2.07 \text{ mA}$$

6-05/22/03

For the MOSFET to be in the active mode  $V_{DS} > V_{GS} - V_{TO}$ .

$$V_D = V + \frac{R_1 + R_2}{R_D + R_1 + R_2} - I_D R_D \parallel (R_1 + R_2)$$

$$= 10.02 \text{ V}$$

$$V_S = I_D R_S = 2.07 \text{ V}$$

$$V_{DS} = V_D - V_S = 7.95 \text{ V}$$

$$V_{GS} = \sqrt{\frac{I_D}{K}} + 1.5 = 3.026 \text{ V}$$

$$V_{GS} - V_{TO} = 1.526 \text{ V}$$

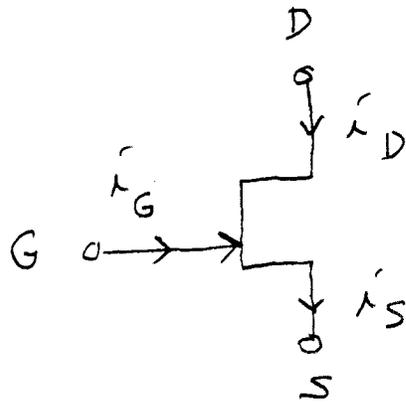
$\Rightarrow V_{DS} > V_{GS} - V_{TO} \Rightarrow$  Active mode

The Junction Field Effect Transistor  
or The JFET

The JFET differs from the MOSFET in that the gate is separated from the channel by

7-05/22/03

a pn junction instead of an insulating or dielectric layer. The pn junction must be reverse biased, otherwise gate current will flow. The circuit symbol for the n-channel JFET is



The drain current is given by

$$i_D = \beta_0 (1 + \lambda v_{DS}) (v_{GS} - V_{T0})^2$$

If we let

$$\beta = \beta_0 (1 + \lambda v_{DS})$$

the drain current can be written

8-05/22/03

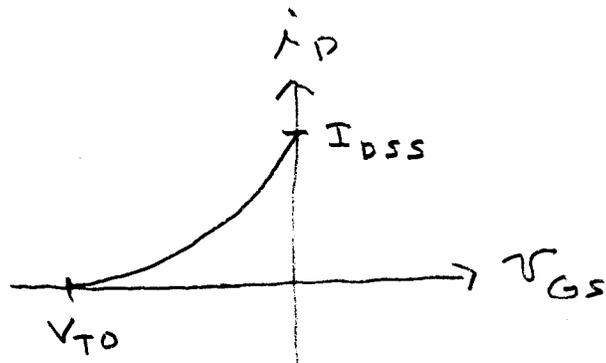
$$i_D = \beta (v_{GS} - v_{TO})^2$$

$\beta$  is the transconductance parameter. Its zero bias value is  $\beta_0$ .  $v_{TO}$  is the threshold voltage.

For the JFET to be in the active mode, we must have

$$v_{DS} > v_{GS} - v_{TO}$$

The JFET is a depletion mode device, thus  $v_{TO}$  is negative. The transfer characteristics are a plot of  $i_D$  versus  $v_{GS}$  for  $v_{DS} = \text{constant}$ .



9-05/22/03

For  $v_{GS} > 0$ , gate current flows. Thus  $v_{GS}$  is constrained to be in the range  $V_{T0} \leq v_{GS} \leq 0$ .

The value of  $i_D$  for  $v_{GS} = 0$  is denoted  $I_{DSS}$ . This is called the drain to source saturation current.

$$I_{DSS} = \beta V_{T0}^2$$

$$\Rightarrow \beta = \frac{I_{DSS}}{V_{T0}^2}$$

$$\begin{aligned} \Rightarrow i_D &= \frac{I_{DSS}}{V_{T0}^2} (v_{GS} - V_{T0})^2 \\ &= I_{DSS} \left( \frac{v_{GS}}{V_{T0}} - 1 \right)^2 \\ &= I_{DSS} \left( 1 - \frac{v_{GS}}{V_{T0}} \right)^2 \end{aligned}$$

The latter equation is a commonly used equation for  $i_D$ . Note that  $I_{DSS}$  varies with  $v_{DS}$

10-05/22/03

according to the equation

$$I_{DSS} = \beta V_{T0}^2 = \beta_0 (1 + \lambda V_{DS}) V_{T0}^2$$

If  $K$  in the MOSFET equations is replaced with  $\beta$ , we obtain the corresponding JFET equation. The hybrid- $\pi$  and T models are the same. For the JFET

$$g_m = 2 \sqrt{\beta I_D} = \frac{-2}{V_{T0}} \sqrt{I_D I_{DSS}}$$

$$r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D}$$

$$r_{\pi} = \frac{1}{g_m}$$

Note that  $g_m > 0$  because  $V_{T0} < 0$ .

The JFET bias equation is the same as the MOSFET bias equation with  $K$  replaced with  $\beta$ .