**ECE3050 Summer 2005**
**Design Project**

The figure shows the circuit diagram of an operational amplifier. The object of this assignment is to calculate the circuit elements and perform a SPICE simulation. You must write the netlist or SPICE deck for the assignment. You are not permitted to use a schematic editor to generate the netlist. To do this, you use an ascii text editor. Such an editor is part of both *PSpice*, Notepad, or Wordpad . The first line of the netlist must be a title line. You can title it ECE 3050 DESIGN PROJECT. A suggested name for the ascii netlist file is opamp.cir. Comment lines must be preceded by an asterisk. Continuation lines must be preceded by a plus sign followed by a space. Write the netlist using all capital letters.

For the JFET and BJTs in the circuit, you are to use the following SPICE MODEL statements:

| | |
|---|---|
| $J_1$ | `.MODEL MNJF1 NJF BETA=5E-4 VTO=-3 LAMBDA=0.0125` |
| $Q_1$, $Q_2$, $Q_5 - Q_7$ | `.MODEL MNPN1 NPN IS=1.26E-14 BF=149 VA=150` |
| $Q_3$, $Q_4$, $Q_8$ | `.MODEL MPNP1 PNP IS=1.26E-14 BF=149 VA=150` |

where BF for the BJT is its $\beta$. The other parameters should be self explanatory. In your calculations for the resistors, you can neglect the Early effect, i.e. set $V_A = \infty$ and $\lambda = 0$. In addition, with the exception of $Q_5$ and $Q_6$, neglect all BJT base currents, i.e. set $I_B = 0$.

First, label the node numbers for each node in the circuit. The ground node must be labeled 0. Voltage sources are of the form `VX N1 N2 AC ACVAL DC DCVAL`, where `VX` is the source name, `N1` is the positive node, `N2` is the negative node, `ACVAL` is the ac phasor value, and `DCVA` is the dc value. Current sources are of the form `IX N1 N2 AC ACVAL DC DCVAL`. The arrow in the current source symbol points from the `N1` node to the `N2` node. Resistors and capacitors are specified as `RX N1 N2 VALUE` and `CX N1 N2 VALUE`. BJTs are specified as `QX NC NB NE QMDL`, where `QX` is the BJT name, `NC`, `NB`, and `NE`, respectively, are the collector, base, and emitter nodes, and `QMDL` is the model name. JFETs are specified as `JX ND NG NS JMDL`, where `JX` is the JFET name, `ND`, `NG`, and `NS`, respectively, are the drain, gate, and source nodes, and `JMDL` is the model name.

The first step in any design is to specify the dc bias values. These are specified to be $V^+ = 18\,\text{V}$, $V^- = -18\,\text{V}$, $V_O = 0\,\text{V}$, $I_{D1} = 1.5\,\text{mA}$, $I_{C3} = 0.5\,\text{mA}$, $I_{C4} = 1.5\,\text{mA}$, $I_{C6} = 2\,\text{mA}$, and $I_{E7} = I_{E8} = 2\,\text{mA}$. The small-signal ac gain with feedback can be approximated by the equation

$$\frac{v_o}{v_i} = 1 + \frac{R_{F2}}{R_{F1}}$$

This is the familiar gain formula for the non-inverting op-amp amplifier. The gain is specified to have a value of 10 (20 dB). The value of $R_{F2}$ is to be $10\,\text{k}\Omega$. The value of $C_F$ is to be calculated so that $1/(2\pi R_{F1} C_F) = 10\,\text{Hz}$. The value of $R_L$ is specified to be $R_L = 1\,\text{k}\Omega$. The value of both $R_{1A}$ and $R_{1B}$ are specified to be equal to $R_{F2}$. The value of $C_1$ is to be calculated so that $1/(2\pi R_{1B} C_1) = 10\,\text{Hz}$. The values of $R_{E7}$ and $R_{E8}$ are to be $10\,\Omega$.

The circuit is to be designed for the gain-bandwidth product $f_x = 1\,\text{MHz}$ and the slew rate $SR = 10\,\text{V}/\mu\text{s}$. The approximate design equations which set these parameters are

$$f_x = \frac{1}{4\pi\,(r_e + R_E)\,C_c} \qquad SR = \frac{I_{D1}}{2C_c}$$

where $r_e = 2V_T/I_{D1}$. You can use these equations to solve for the values of $R_E$ and $C_c$. The default value of $V_T$ in SPICE is 25.86 mV. This value should be used in the calculations.

The voltage across $R_{E6}$ is specified to be $0.5V_{BE6}$, where $V_{BE6}$ is the base-emitter voltage. You can use the transistor collector current equation to calculate $V_{BE6}$. To calculate $R_{C1}$, use the transistor collector current equation to calculate $V_{EB3}$ and $V_{EB4}$. Then neglect the base currents in $Q_3$ and $Q_4$ to calculate $R_{C1} = (V_{EB3} + V_{EB4})/I_{C1}$. The current through $R_5$ is specified to be $20I_{B6}$. The voltage across $R_{E6}$ is specified to be equal to $V_{BE6}$. If the base currents in $Q_7$ and $Q_8$ are neglected, the current through the $V_{BE}$ multiplier is equal to $I_{C6}$. The $V_{BE}$ multiplier is to be designed so that $I_{E5} = 0.9I_{C6}$ and the current through $R_3$ is $0.1I_{C6}$.

SPICE Analyses:

1. Perform a dot-OP analysis. Examine the dot-OUT file. Verify that all dc bias currents and voltages are equal to or close to the desired values. Do not proceed until the bias values are correct. They do not have to be exact, but you should be able to come within 5% to 10% of the specified values. You will find the bias currents in $Q_7$ and $Q_8$ are extremely sensitive to the voltage across the $V_{BE}$ multiplier. You may have to experimentally "tweak" the value of either $R_2$ or $R_3$ to obtain the desired current.

2. Perform a dot-AC analysis using AC 1 for $V_i$. Plot the amplifier gain versus frequency using log scales for both the vertical and horizontal axes. Do not use linear scales! Verify that the mid-frequency gain is approximately 10, the gain at 10 Hz is approximately 5, and the high-frequency gain passes through unity at approximately $f = f_x$. Do not proceed with the following steps until you meet these specifications.

3. Determine the upper frequency at which the gain is $10/\sqrt{2}$. Verify that this frequency multiplied by the mid-frequency gain of 10 is equal to $f_x$.

4. Plot the open-loop gain as a function of frequency by plotting $V_o/(V_{b1} - V_{b2})$.

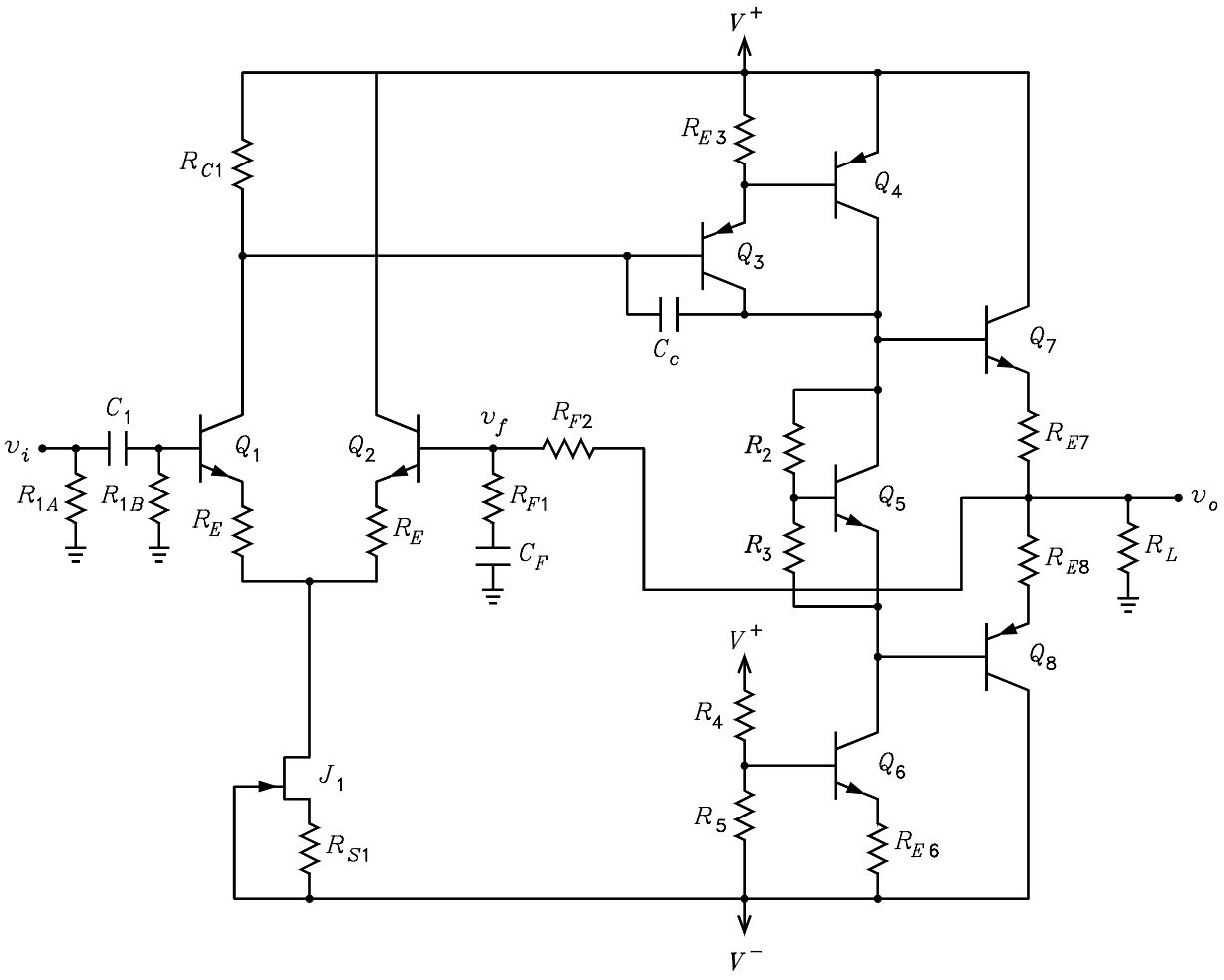
5. Perform a dot-TRAN analysis using a voltage step at the input of value 1 V. Plot the output voltage as a function of time and evaluate the maximum slope. This should be equal to the positive slew rate. With 1 V input, the output should rise to 10 V.

6. Perform a dot-TRAN analysis using a voltage step at the input of value $-1$ V. Plot the output voltage as a function of time and evaluate the maximum slope. This should be equal to the negative slew rate. With $-1$ V input, the output should fall to $-10$ V.

7. Perform a dot-TRAN analysis using a sine wave at the input with a frequency of 1 kHz. Increase the amplitude of the sine wave until the op amp is driven just to the clipping level. Is the clipping symmetrical? Obtain a plot of the output voltage.

8. Set $V_i = 0$, replace $R_L$ with a 1 A ac current source. Perform a dot-AC analysis and plot $V_o$ as a function of frequency using log-log scales. This plot is a plot of the small-signal output impedance of the op amp.

In your write-up, include calculations, a copy of the circuit diagram with all SPICE nodes numbered, and a copy of the netlist. Include a copy of the dot-OUT file showing all dc bias currents and voltages. Include all frequency response plots and all transient response plots. Title all plots and label pertinent values on the plots, e.g. mid-band gain, lower cutoff frequency, upper cutoff frequency, gain-bandwidth product, slew rates, etc.


$V^+$
$R_{E3}$
$Q_4$
$R_{C1}$
$Q_3$
$C_c$
$Q_7$
$C_1$
$v_f$
$R_{F2}$
$R_{E7}$
$v_i$
$Q_1$
$Q_2$
$R_2$
$Q_5$
$v_o$
$R_{1A}$
$R_{1B}$
$R_E$
$R_E$
$R_{F1}$
$C_F$
$R_3$
$R_{E8}$
$R_L$
$V^+$
$Q_8$
$R_4$
$Q_6$
$J_1$
$R_5$
$R_{E6}$
$R_{S1}$
$V^-$