Chapter 1

Ideal Op-Amp Circuits

The operational amplifier, or *op amp* as it is commonly called, is a fundamental element of analog circuit design. It is most commonly used in amplifier and analog signal processing circuits in the frequency band from 0 to 100 kHz. High-frequency op amps are used in applications that require a bandwidth into the MHz range. The first op amps were vacuum-tube circuits which were developed for use in analog computers. Modern op amps are fabricated as integrated circuits that bare little resemblance to early circuits. This chapter covers some of the basic applications of the op amp. It is treated as an ideal circuit element without regard to its internal circuitry.

The notation used in this chapter is as follows: Total quantities are indicated by lower-case letters with upper-case subscripts, e.g. v_I, i_O, r_{IN}. Small-signal quantities are indicated by lower-case letters with lower-case subscripts, e.g. v_i, i_o, r_{in}. Transfer function variables and phasors are indicated by upper case letters and lower-case subscripts, e.g. V_i, I_o, Z_{in}.

1.1 The Ideal Op-Amp

The *ideal op amp* is a three terminal device that is modeled as a voltage-controlled voltage source. That is, its output voltage is a gain multiplied by its input voltage. The circuit symbol is given in Fig. 1.1(a). The input voltage is the difference voltage between the two input terminals. The output voltage is measured with respect to the circuit ground and is given by

$$v_O = A\left(v_+ - v_-\right) \tag{1.1}$$

where A is the voltage gain, v_+ is the voltage at the non-inverting input, and v_- is the voltage at the inverting input. The controlled source model is shown in Fig. 1.1(b).

There are three conditions that the terminal characteristics of the ideal op amp satisfy. These are as follows:

1. The current in each input lead is zero. This means that the input resistance to each input is infinite.

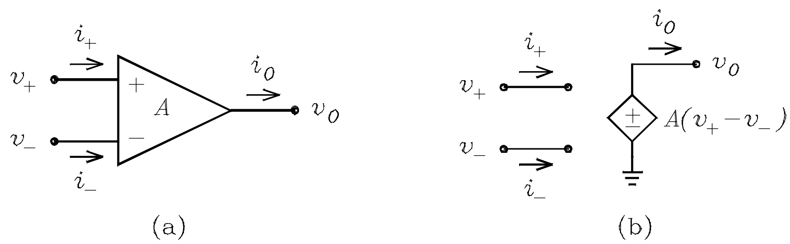

Figure 1.1: (a) Op-amp symbol. (b) Controlled-source model of the ideal op amp.

2. The output voltage is independent of the output current. This means that the output resistance is zero.
3. The voltage gain is very large, approaching infinity in the limit. If the output voltage is finite, this means that the difference voltage between the two inputs must approach zero.

For it to be act as an amplifier, the op amp must have feedback applied from its output to its inverting input. That is, part of the output voltage must be sampled by a network and fed back into the inverting input. This makes it possible to design an amplifier so that its gain is set by the feedback network.

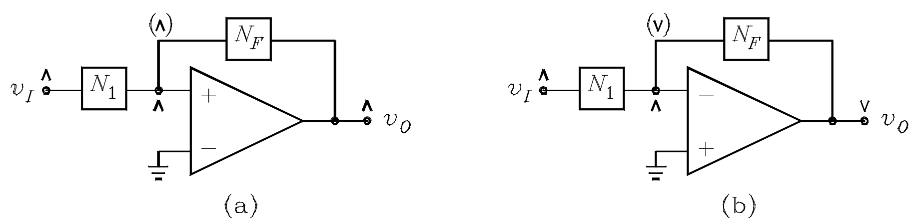

Figure 1.2: (a) Op amp with positive feedback. (b) Op amp with negative feedback.

To illustrate the effects of feedback, consider the circuits in Fig. 1.2. The networks labeled N_1 and N_F, respectively, are the input and feedback networks. The op amp of Fig. 1.2(a) has positive feedback whereas the op amp of Fig. 1.2(b) has negative feedback. Let a unit step of voltage be applied to the input of each circuit. The arrows in the figures indicate the directions in which the input voltages change, i.e. each input voltage goes positive. For the circuit of Fig. 1.2(a), the positive voltage at v_I is fed through N_1 to cause the voltage at the v_+ terminal to go positive. This is amplified by a positive gain $(+A)$ and causes the output voltage to go positive. This is fed back through N_F to make the voltage at the v_+ terminal to go more positive. (The arrow for the feedback voltage is enclosed in parentheses to distinguish it from the arrow for the initial increase in voltage.) This causes the output voltage to increase further, causing v_+ to increase further, etc. It is clear that the circuit is not stable with positive feedback.

For the circuit of Fig. 1.2(b), the positive voltage at the input is fed through N_1 to cause the voltage at the v_- terminal to go positive. This is amplified by a negative gain $(-A)$ and causes the output voltage to go negative. This is fed back through N_F to partially cancel the positive voltage at the v_- input. Because the v_- voltage is decreased by the feedback, it follows that v_O is prevented from going more negative. Thus the circuit reaches a stable equilibrium.

To illustrate the effects of feedback, we have used the concept of *signal tracing* in the circuits of Fig. 1.2. Signal tracing is a simple concept which can be applied to any circuit to check for positive and negative feedback. Circuits which have positive feedback are unstable in general and are not used for amplifier circuits. With few exceptions, the circuits covered in this chapter have only negative feedback.

1.2 Inverting Amplifiers

1.2.1 The Inverting Amplifier

Figure 1.3(a) shows the circuit diagram of an *inverting amplifier*. The input signal is applied through resistor R_1 to the v_- op-amp input. Resistor R_F is the feedback resistor which connects from the output to the inverting input. We will find that the voltage gain of the circuit is negative. This is the reason it is called an inverting amplifier. The v_+ op-amp input is not used. The figure shows this input grounded.

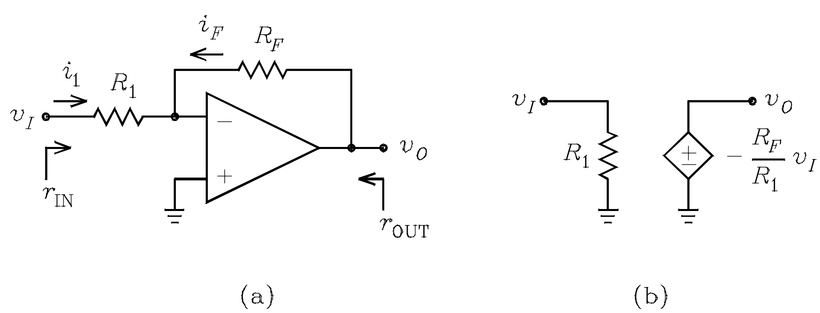

Figure 1.3: (a) Inverting amplifier. (b) Controlled-source equivalent circuit.

For the circuit of Fig. 1.3(a), the voltage at the inverting input is given by $v_- = -v_O/A$. If v_O is finite and $A \to \infty$, it follows that $v_- \to 0$. Even though the v_- input is not grounded, it is said to be a *virtual ground* because the voltage is zero, i.e. at ground potential. Because $i_- = 0$, the sum of the currents into the v_- node through resistors R_1 and R_F must be zero, i.e. $i_1 + i_F = 0$, where $i_1 = v_I/R_1$ and $i_F = v_O/R_F$. Thus we can write

$$i_1 + i_F = 0 \Rightarrow \frac{v_I}{R_1} + \frac{v_O}{R_F} = 0 \tag{1.2}$$

This can be solved for the voltage gain to obtain

$$\frac{v_O}{v_I} = -\frac{R_F}{R_1} \tag{1.3}$$

The input resistance is given by $r_{\text{IN}} = v_I / i_1$. Because $v_- = 0$, it follows that

$$r_{\text{IN}} = R_1 \tag{1.4}$$

The output resistance is equal to the output resistance of the op amp so that

$$r_{\text{OUT}} = 0 \tag{1.5}$$

The controlled source model of the inverting amplifier is shown in Fig. 1.3(b).

Example 1 *Design an inverting amplifier with an input resistance of* 2 kΩ*, an output resistance of* 100 Ω*, and an open-circuit voltage gain of* −30 *(an inverting decibel gain of* 29.5 *dB).*

Solution. The circuit diagram is given in Fig. 1.4(a). For $r_{\text{IN}} = 2$ kΩ, Eq. (1.4) gives $R_1 = 2$ kΩ. For $v_O/v_I = -30$, it follows from Eq. (1.3) that $R_F = 60$ kΩ. For $r_{\text{OUT}} = 100$ Ω, the resistor $R_O = 100$ Ω must be used in series with the output.

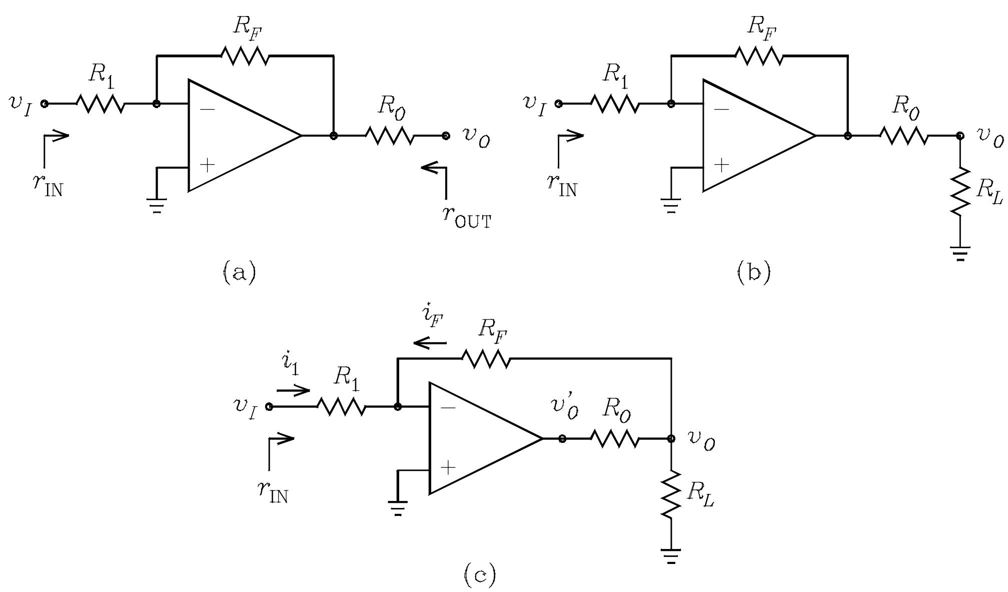

Figure 1.4: (a) Circuit for Example 1. (b) Circuit for Example 2.(c) Circuit for Example 3.

Example 2 *Calculate the voltage gain of the circuit of Fig. 1.4(a) if a* 1 kΩ *load resistor is connected from the output to ground. The circuit diagram is shown in Fig. 1.4(b).*

Solution. The voltage gain decreases when R_L is added because of the drop across R_O. The gain decreases by a factor given by the voltage division ratio

$$\frac{R_L}{R_O + R_L} = \frac{1000}{1000 + 100} = \frac{10}{11}$$

Thus the loaded gain is $(10/11) \times (-30) = -27.3$ (an inverting decibel gain of 28.7 dB).

Example 3 *For the inverting amplifier of Fig. 1.4(b), investigate the effect of connecting the feedback resistor R_F to the load resistor R_L rather than to the op amp output terminal. The circuit diagram is shown in Fig. 1.4(c).*

Solution. Because $i_1 + i_F = 0$, it follows that $v_I/R_1 + v_O/R_F = 0$. This can solved for the voltage gain to obtain $v_O/v_I = -R_F/R_1$. Because this is independent of R_L, it follows that the output resistance of the circuit is zero. Thus the circuit looks like the original circuit of Fig. 1.4(b) with $R_O = 0$. With $R_O \neq 0$, the op amp must put out a larger voltage in order to maintain a load voltage that is independent of R_O. Let v'_O be the voltage at the op-amp output terminal. By voltage division, v_O is given by

$$v_O = v'_O \frac{R_L \| R_F}{R_L \| R_F + R_O} = \frac{v'_O}{1 + R_O/\left(R_L \| R_F\right)}$$

Thus v'_O is larger than v_O by the factor $1 + R_O/\left(R_L \| R_F\right)$. If a load resistor is added to the circuit, v'_O will be even larger for a given v_O.

1.2.2 The Inverting Amplifier with T Feedback Network

If a high-gain inverting amplifier is required, Eq. (1.3) shows that either R_F must be large, R_1 must be small, or both. If R_1 is small, the input resistance given by Eq. (1.4) may be too low to meet specifications. The inverting amplifier with a T feedback network shown in Fig. 1.5(a) can be used to obtain a high voltage gain without a small value for R_1 or very large values for the feedback resistors.

The solution for the voltage gain is simplified by making a Thevenin equivalent circuit looking into R_2 from the v_- terminal. The circuit diagram is given in Fig. 1.5(b). Because $i_1 + i_F = 0$, it follows that

$$\frac{v_I}{R_1} + \frac{v_O R_3}{R_3 + R_4} \times \frac{1}{R_2 + R_3 \| R_4} = 0 \tag{1.6}$$

This can be solved for the gain to obtain

$$\frac{v_O}{v_I} = -\left[\frac{R_2}{R_1} + \frac{R_4}{R_1}\left(1 + \frac{R_2}{R_3}\right)\right] \tag{1.7}$$

The output resistance is zero. The input resistance is R_1.

Example 4 *For the inverting amplifier in Fig. 1.5(a), specify the resistor values which give an input resistance of* 10 kΩ *and a gain of* -100. *The maximum resistor value in the circuit is limited to* 100 kΩ.

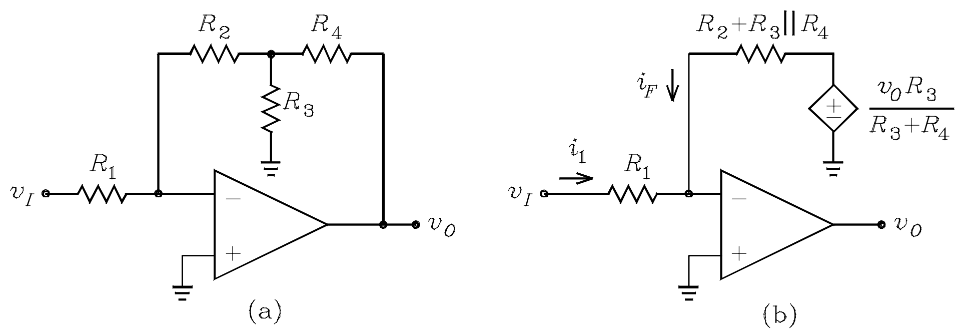

Figure 1.5: (a) Inverting amplifier with T feedback network. (b) Equivalent circuit for calculating v_O.

Solution. To meet the input resistance specification, let $R_1 = 10$ kΩ. Let $R_2 = R_4 = 100$ kΩ. It follows from Eq. (1.7) that R_3 is given by

$$R_3 = R_2 \left[\frac{R_1}{R_4} \left(\frac{v_O}{v_I} + \frac{R_2}{R_1} \right) - 1 \right]^{-1} = 12.5 \text{ k}\Omega$$

1.2.3 The Current-to-Voltage Converter

The circuit diagram of a *current-to-voltage converter* is given in Fig. 1.6(a). The circuit is a special case of an inverting amplifier where the input resistor is replaced with a short circuit. Because the v_- terminal is a virtual ground, the input resistance is zero. The output resistance is also zero. Because $i_1 + i_F = 0$ and $v_O = i_F R_F$, it follows that v_O/i_1 is given by

$$\frac{v_O}{i_1} = -R_F \tag{1.8}$$

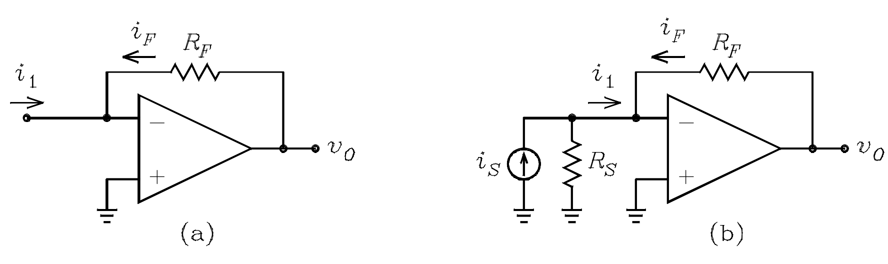

Figure 1.6: (a) Current-to-voltage converter. (b) Circuit with an input current source.

The circuit of Fig. 1.6(b) shows the current-to-voltage converter with a current source connected to its input. Because R_S connects from a virtual ground to ground, the current through it is zero. It follows that $i_1 = i_S$ and $v_O = -R_F i_S$. Thus the output voltage is independent of R_S.

1.3 Non-Inverting Amplifiers

1.3.1 The Non-Inverting Amplifier

Figure 1.7(a) shows the circuit diagram of a *non-inverting amplifier*. The input voltage v_I is applied to the non-inverting op-amp input. A voltage divider consisting of resistors R_F and R_1 connects from the output node to the inverting input. The circuit is called a non-inverting amplifier because its voltage gain is positive. If the circuits of the inverting and the non-inverting amplifiers are compared, it can be seen that the two are the same if $v_I = 0$. Thus the only difference between the two amplifiers is the node to which the input voltage is applied.

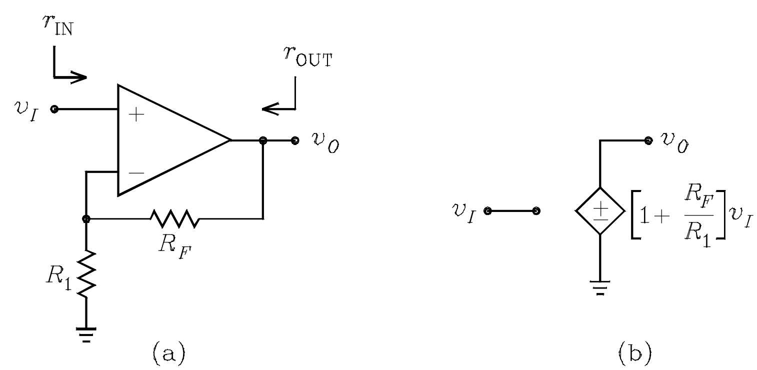

Figure 1.7: (a) Non-inverting amplifier. (b) Controlled-source model.

For the circuit of Fig. 1.7(a), the voltage difference between the two op-amp inputs is $v_+ - v_- = v_O/A$. For v_O finite and $A \to \infty$, it follows that $v_+ \to v_-$. Because there is no voltage between the two inputs, a *virtual short circuit* is said to exist between them. For $i_- = 0$, the condition that $v_+ = v_-$ requires v_I and v_O to satisfy the equation

$$v_+ = v_- \Rightarrow v_I = v_O \frac{R_1}{R_F + R_1} \tag{1.9}$$

where a voltage division has been used for v_-. This can be solved for the gain to obtain

$$\frac{v_O}{v_I} = 1 + \frac{R_F}{R_1} \tag{1.10}$$

The input and output resistances are given by

$$r_{\text{IN}} = \infty \tag{1.11}$$

$$r_{\mathrm{OUT}} = 0 \tag{1.12}$$

The controlled source model for the non-inverting amplifier is shown in Fig. 1.7(b).

Example 5 *Design a non-inverting amplifier which has an input resistance of* 10 *k*Ω*, an open-circuit voltage gain of* 20*, and an output resistance of* 600 Ω*. The feedback network is specified to draw no more than* 0.1 *mA from the op-amp output when the peak open-circuit output voltage is* 10 *V.*

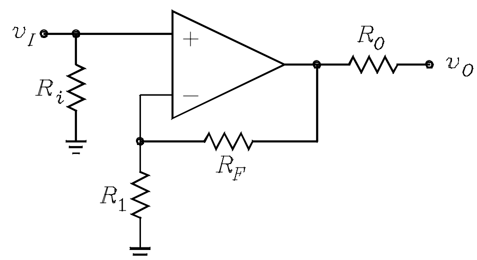

Figure 1.8: Circuit for Example 5.

Solution. The circuit diagram is shown in Fig. 1.8. The input and output resistance specifications require $R_i = 10$ kΩ and $R_O = 600$ Ω. For the specified current in the feedback network, we must have 0.1 mA $\leq 10/(R_F + R_1)$. If equality is used, we obtain $R_F + R_1 =$ 100 kΩ. For the specified open-circuit voltage gain, Eq. (1.10) gives $1 + R_F/R_1 = 20$ or $R_F = 19R_1$. It follows that $R_1 = 5$ kΩ and $R_F = 95$ kΩ.

Example 6 . *Examine the effect of a connecting a resistor between the* v_+ *node and the* v_- *node in the non-inverting amplifier of Fig. 1.7.*

Solution. For an ideal op amp, $v_+ - v_- = 0$. It follows that a resistor connected between the inputs has no current flowing through it. Therefore, the resistor has no apparent effect on the circuit. This conclusion applies also for the inverting amplifier circuit of Fig. 1.3. With physical op amps, however, a resistor connected between the v_+ and the v_- terminals can affect the performance of the circuit by effectively reducing the open-loop gain of the op amp.

1.3.2 The Voltage Follower

The *voltage follower* or *unity-gain buffer* is a non-inverting amplifier with unity gain. The circuit diagram is shown in Fig. 1.9. Because the output node is connected directly to the inverting input, the circuit is said to have 100% feedback. Because $v_+ = v_-$, it follows that $v_O = v_I$. Therefore, the circuit has unity voltage gain. The voltage follower is often used to isolate a low-resistance load from a source having a high output resistance. That is, the voltage follower supplies the current to drive the load while drawing no current from the input circuit. It is also used as a buffer in applications where it is desired to prevent the frequency response of a circuit from being a function of the output resistance of the source or a function of the load resistance.

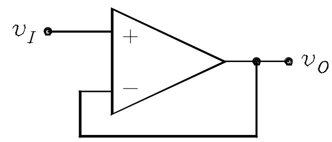

Figure 1.9: Voltage follower or unity-gain buffer.

1.3.3 The Non-Inverting Amplifier with Voltage and Current Feedback

Figure 1.10(a) shows the circuit diagram of a non-inverting amplifier in which the voltage fed back to the op-amp inverting input is a function of both the load voltage and the load current. To solve for the output voltage, it is convenient to first form the Thevenin equivalent circuit seen by R_L. The circuit is shown in Fig. 1.10(b). The source has a value equal to the open-circuit load voltage, i.e. the output voltage with $R_L \to \infty$. The resistor has a value equal to the ratio of the open-circuit load voltage to the short-circuit load current, i.e. the output current with $R_L = 0$.

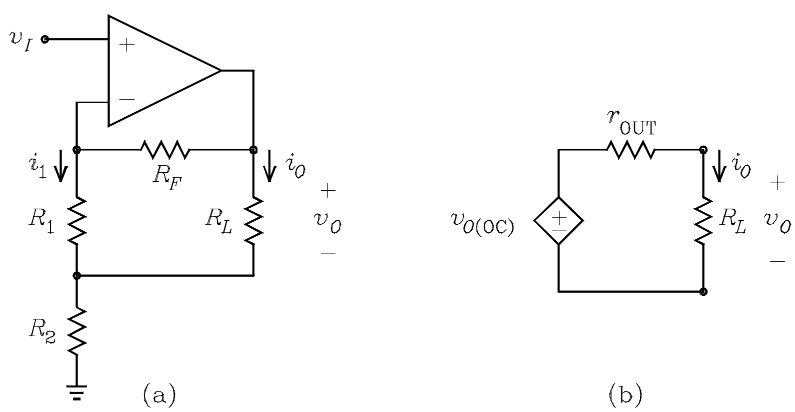

Figure 1.10: (a) Non-inverting amplifier with voltage and current feedback. (b) Thevenin equivalent circuit seen by the load.

With $R_L = \infty$, the output voltage is given by $v_{O(\mathrm{OC})} = i_1 \times (R_F + R_1)$. Because there is a virtual short between the v_+ and the v_- terminals, it follows that $i_1 = v_I / (R_1 + R_2)$.

Thus $v_{O(\text{OC})}$ can be written

$$v_{O(\text{OC})} = v_I \frac{R_F + R_1}{R_1 + R_2} \tag{1.13}$$

With $R_L = 0$, there can be no current through R_F or R_1 so that $v_I = v_- = i_{O(\text{SC})} R_2$. Thus $i_{O(\text{SC})}$ is given by

$$i_{O(\text{SC})} = \frac{v_I}{R_2} \tag{1.14}$$

The output resistance is given by

$$r_{\text{OUT}} = \frac{v_{O(\text{OC})}}{i_{O(\text{SC})}} = R_2 \frac{R_F + R_1}{R_1 + R_2} \tag{1.15}$$

By voltage division, it follows from Fig. 1.10(b) and Eq. (1.13) that the output voltage can be written

$$v_O = v_{O(\text{OC})} \frac{R_L}{r_{\text{OUT}} + R_L} = v_I \frac{R_F + R_1}{R_1 + R_2} \frac{R_L}{r_{\text{OUT}} + R_L} \tag{1.16}$$

1.3.4 The Negative Resistance Converter

Although it is not an amplifier, the *negative resistance converter* is an application of the non-inverting configuration. The circuit diagram is shown in Fig. 1.11. The resistor R bridges the input and output terminals of a non-inverting amplifier. We can write

$$r_{\text{IN}} = \frac{v_I}{i_1} \tag{1.17}$$

$$i_1 = \frac{v_I - v_O}{R} \tag{1.18}$$

$$v_O = \left(1 + \frac{R_F}{R_1}\right) v_I \tag{1.19}$$

Solution for r_{IN} yields

$$r_{\text{IN}} = -\frac{R_1}{R_F} R \tag{1.20}$$

Thus the circuit has a negative input resistance.

A resistor in parallel with another resistor equal to its negative is an open circuit. It follows that the output resistance of a non-ideal current source, i.e. one having a non-infinite output resistance, can be infinite by adding a negative resistance in parallel with the current source. Negative resistors do not absorb power from a circuit. Instead, they supply power. For example, if a capacitor with an initial voltage on it is connected in parallel with a negative resistor, the voltage on the capacitor will increase with time. Relaxation oscillators are waveform generator circuits which use a negative resistance in parallel with a capacitor to generate ac waveforms.

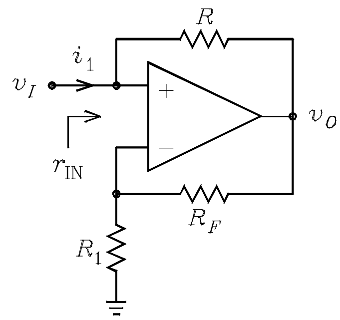

Figure 1.11: Negative resistance converter.

1.4 Summing Amplifiers

1.4.1 The Inverting Summer

The *inverting summer* is a basic op-amp circuit that is used to sum two or more signal voltages, to sum a dc voltage with a signal voltage, etc. The circuit diagram of a four-input inverting summer is shown in Fig. 1.12. If all inputs are grounded except the jth input, where $j = 1, 2, 3$, or 4, Eq. (1.3) for the inverting amplifier can be used to write $v_O = -(R_F/R_j)\,v_{Ij}$. It follows by superposition that the total output voltage is given by

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} - \frac{R_F}{R_3}v_{I3} - \frac{R_F}{R_4}v_{I4} \tag{1.21}$$

The input resistance to the jth input is R_j. The output resistance of the circuit is zero.

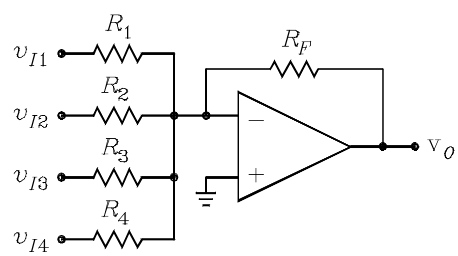

Figure 1.12: Four input inverting summer.

Example 7 *Design an inverting summer which has an output voltage given by $v_O = 3-2v_I$. Assume that +15 V and −15 V supply voltages are available.*

Solution. The output contains a dc component of +3 V. This can be realized by using the −15 V supply as one input. The circuit diagram is shown in Fig. 1.13. For the specified

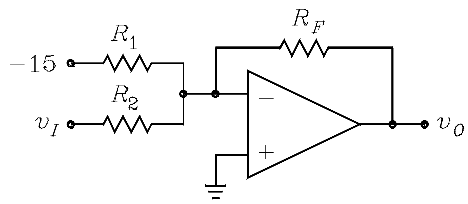

Figure 1.13: Circuit for Example 7.

output, we can write $(-15) \times (-R_F/R_1) = 3$ and $-R_F/R_2 = -2$. If we choose $R_F = 3$ kΩ, it follows that $R_1 = 15$ kΩ and $R_2 = 1.5$ kΩ.

1.4.2 The Non-Inverting Summer

A *non-inverting summer* can be realized by connecting the inputs through resistors to the input terminal of a non-inverting amplifier. Unlike the inverting amplifier, the input resistors do not connect to a virtual ground. Thus a current flows in each input resistor that is a function of the voltage at the other inputs. This makes it impossible to define the input resistance for any one input unless all other inputs are grounded. The circuit diagram for a four-input non-inverting summer is shown in Fig. 1.14(a). To solve for the output voltage, it is convenient to first make Norton equivalent circuits at the v_+ terminal for each of the inputs. The circuit is shown in Fig. 1.14(b). Eq. (1.10) can be used to write the equation for v_O as follows:

$$\begin{aligned} v_O &= \left(1 + \frac{R_F}{R_6}\right) v_+ \\ &= \left(1 + \frac{R_F}{R_6}\right)\left(\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_{I3}}{R_3} + \frac{v_{I4}}{R_4}\right)(R_1 \| R_2 \| R_3 \| R_4 \| R_5) \end{aligned} \tag{1.22}$$

The output resistance of the circuit is zero. If the v_{I2} through v_{I4} inputs are grounded, the input resistance to the v_{I1} node is given by

$$r_{\mathrm{IN}} = R_1 + R_2 \| R_3 \| R_4 \| R_5 \tag{1.23}$$

The input resistance to the other inputs can be written similarly.

Example 8 *Design a two-input non-inverting summer which has an output voltage given by* $v_O = 8\,(v_{I1} + v_{I2})$. *With either input grounded, the input resistance to the other input is specified to be* 10 *k*Ω. *In addition, the current which flows in the grounded input lead is to be* 0.1 *times the current that flows in the ungrounded lead.*

Solution. The circuit diagram is shown in Fig. 1.15. By symmetry, it follows that $R_1 = R_2$. For $r_{\mathrm{IN1}} = 10$ kΩ when $v_{I2} = 0$, we have $R_1 + R_1 \| R_3 = 10$ kΩ. For $v_{I2} = 0$, i_2 is given by $i_2 = -i_1 R_3 / (R_3 + R_1)$. Thus, for $i_2 = -0.1 i_1$, we must have $R_3 / (R_3 + R_1) = 0.1$.

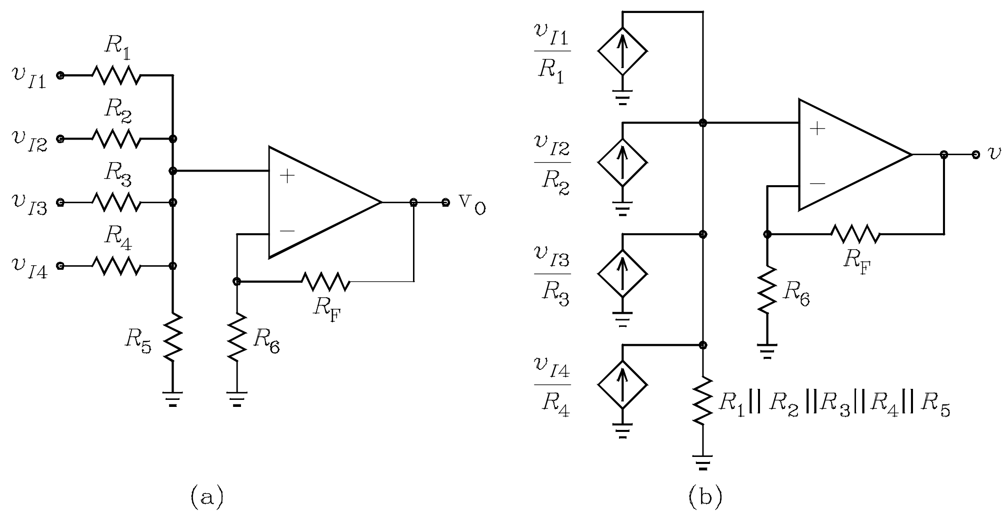

Figure 1.14: (a) Four input non-inverting summer. (b) Equivalent circuit.

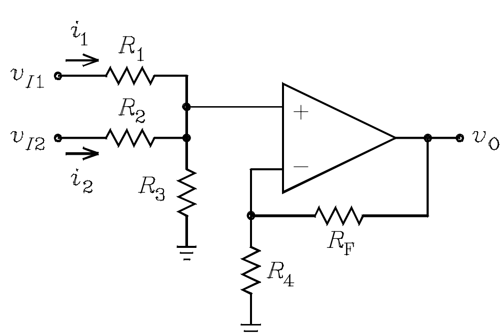

Figure 1.15: Figure for Example 8.

It follows from these two equations that $R_3 = 10/9.9\ \text{k}\Omega = 1.01\ \text{k}\Omega$ and $R_1 = R_2 = 9R_3 = 10/1.1\ \text{k}\Omega = 9.09\ \text{k}\Omega$. If $v_{I1} = v_{I2} = v_I$, we can write $v_O/v_I = 16$. Thus we can write the design equation

$$16 = \frac{v_+}{v_I} \times \frac{v_O}{v_+} = \frac{R_3}{R_3 + R_1 \| R_2}\left(1 + \frac{R_F}{R_4}\right)$$

It follows from this equation that $1 + R_F/R_4 = 88$. This is satisfied if we choose $R_4 = 270\ \Omega$ and $R_F = 23.5\ \text{k}\Omega$.

1.5 Differential Amplifiers

1.5.1 The Single Op-Amp Diff-Amp

A *differential amplifier* or *diff amp* is an amplifier which has two inputs and one output. When a signal is applied to one input, it operates as a non-inverting amplifier. When a signal is applied to the other input, it operates as an inverting amplifier. The circuit diagram of a single op-amp diff amp is shown in Fig. 1.16. Superposition can be used to write the equation for v_O as follows:

$$v_O = v_+\left(1 + \frac{R_F}{R_3}\right) - v_{I2}\frac{R_F}{R_3} = v_{I1}\frac{R_2}{R_1 + R_2}\left(1 + \frac{R_F}{R_3}\right) - v_{I2}\frac{R_F}{R_3} \tag{1.24}$$

where Eqs. (1.3) and (1.10) have been used.

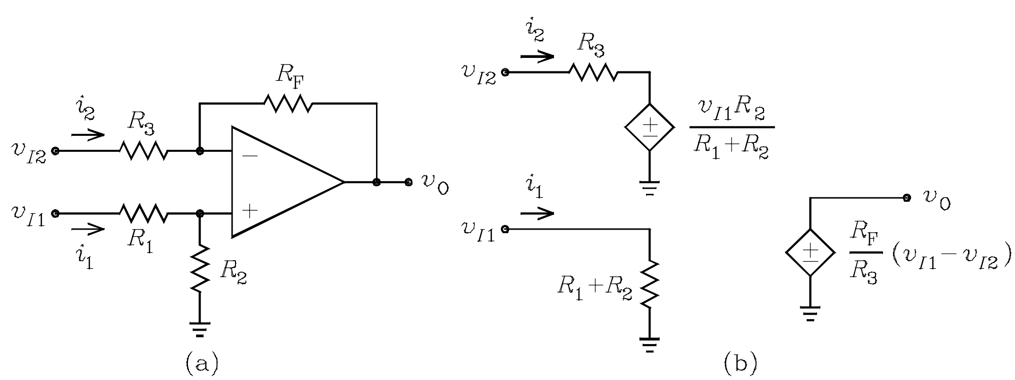

Figure 1.16: (a) Single op-amp differential amplifier. (b) Equivalent circuit for the true diff amp.

The diff-amp output resistance is zero. The input resistance to the v_{I1} node is

$$r_{\text{IN1}} = R_1 + R_2 \tag{1.25}$$

The current i_2 which flows in the v_{I2} input lead is a function of the voltage at the v_{I1} input and is given by

$$i_2 = \frac{v_{I2} - v_-}{R_3} = \frac{1}{R_3}\left(v_{I2} - v_{I1}\frac{R_2}{R_1 + R_2}\right) \tag{1.26}$$

where $v_- = v_+$ has been used. The input resistance to the v_{I2} node is given by $r_{\text{IN2}} = v_{I2}/i_2$, which depends of v_{I1}. For example, $v_{I1} = 0$ gives $r_{\text{IN2}} = R_3$, $v_{I1} = -v_{I2}$ gives $r_{\text{IN2}} = R_3\left(R_1 + R_2\right)/\left(R_1 + 2R_2\right)$, $v_{I1} = +v_{I2}$ gives $r_{\text{IN2}} = R_3\left(1 + R_2/R_1\right)$, etc. In the case that v_{I2} is non-zero and independent of v_{I1}, $r_{\text{IN2}} = R_3$ but an additional current flows in the v_{I2} input that is due to v_{I1}.

1.5.2 The True Diff-Amp

The output voltage of a *true diff amp* is zero if $v_{I1} = v_{I2}$. It follows from Eq. (1.24) that the condition for a true diff amp is

$$\frac{R_2}{R_1} = \frac{R_F}{R_3} \tag{1.27}$$

To achieve this condition, it is common to make $R_1 = R_3$ and $R_2 = R_F$. In this case, the output voltage can be written

$$v_O = \frac{R_F}{R_3}\left(v_{I1} - v_{I2}\right) \tag{1.28}$$

The controlled-source equivalent circuit of the true diff amp is shown in Fig. 1.5.1(b).

Example 9 *For the diff-amp circuit of Fig. 1.16, it is given that $R_1 = R_3 = 10$ kΩ and $R_2 = R_F = 20$ kΩ. Solve for the output voltage of the circuit, the input resistance to the v_{I1} terminal, and the input resistance to the v_{I2} terminal for the three cases: $v_{I1} = 0$, $v_{I1} = -v_{I2}$, and $v_{I1} = +v_{I2}$.*

Solution. Because $R_F/R_3 = R_2/R_1$, the output voltage is given by Eq. (1.28). It is $v_O = 2\left(v_{I1} - v_{I2}\right)$. The input resistance to the v_{I1} node is 30 kΩ. As described above, the input resistance to the v_{I2} terminal is a function of v_{I1}. For $v_{I1} = 0$, it is 10 kΩ. For $v_{I1} = -v_{I2}$, it is 6 kΩ. For $v_{I1} = +v_{I2}$, it is 40 kΩ.

1.5.3 Differential and Common-Mode Voltage Gains

Figure 1.17 shows a diff-amp circuit with three sources at its input. The two input voltages are given by

$$v_{I1} = v_{CM} + \frac{v_D}{2} \tag{1.29}$$

$$v_{I2} = v_{CM} - \frac{v_D}{2} \tag{1.30}$$

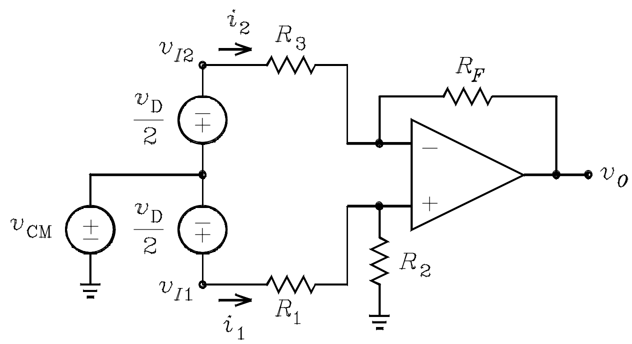

Figure 1.17: Diff amp with differential and common-mode inputs.

The voltage v_{CM} is called the *common-mode input voltage* because it appears equally at both inputs. The voltage v_D is called the *differential input voltage* because one-half of its value appears at each input with opposite polarities.

It is often convenient to analyze diff-amp circuits by expressing the input voltages in terms of common-mode and differential components. The voltages v_D and v_{CM} can be expressed in terms of v_{I1} and v_{I2} as follows:

$$v_D = v_{I1} - v_{I2} \tag{1.31}$$

$$v_{CM} = \frac{v_{I1} + v_{I2}}{2} \tag{1.32}$$

These two equations can be used to resolve any two arbitrary input voltages into differential and common-mode components. For example, $v_{I2} = 0$ gives $v_D = v_{I1}$ and $v_{CM} = v_{I1}/2$, $v_{I2} = -v_{I1}$ gives $v_D = 2v_{I1}$ and $v_{CM} = 0$, $v_{I2} = v_{I1}$ gives $v_D = 0$ and $v_{CM} = v_{I1}$, etc.

By Eq. (1.24), the output voltage of the diff amp in Fig. 1.17 can be written

$$\begin{aligned} v_O &= \left(v_{CM} + \frac{v_D}{2}\right)\frac{R_2}{R_1 + R_2}\left(1 + \frac{R_F}{R_3}\right) - \left(v_{CM} - \frac{v_D}{2}\right)\frac{R_F}{R_3} \\ &= v_{CM}\frac{R_2}{R_1 + R_2}\left(1 - \frac{R_F R_1}{R_2 R_3}\right) + \frac{v_D}{2}\frac{R_F}{R_3}\left(1 + \frac{R_2\left(R_3 + R_F\right)}{R_F\left(R_1 + R_2\right)}\right) \end{aligned} \tag{1.33}$$

This equation can be used to define the differential and common-mode voltage gains, respectively, as follows:

$$A_d = \frac{v_O}{v_D} = \frac{R_F}{2R_3}\left(1 + \frac{R_2\left(R_3 + R_F\right)}{R_F\left(R_1 + R_2\right)}\right) \tag{1.34}$$

$$A_{cm} = \frac{v_O}{v_{CM}} = \frac{R_2}{R_1 + R_2}\left(1 - \frac{R_F R_1}{R_2 R_3}\right) \tag{1.35}$$

If $R_F/R_2 = R_3/R_1$, these equations give $A_d = R_F/R_3$ and $A_{cm} = 0$.

1.5.4 The Common-Mode Rejection Ratio

For a true diff amp, the common-mode voltage gain is zero. In practice, it is difficult to achieve a common-mode gain that is exactly zero because of resistor tolerances and non-ideal op-amp characteristics. A figure of merit for the true diff amp is the ratio of its differential voltage gain to its common-mode voltage gain. This is called the *common-mode rejection ratio* or $CMRR$. Ideally, it is infinite. The $CMRR$ of the circuit in Fig. 1.17 is given by

$$CMRR = \frac{A_d}{A_{cm}} = \frac{\frac{R_F}{2R_3}\left(1 + \frac{R_2(R_3+R_F)}{R_F(R_1+R_2)}\right)}{\frac{R_2}{R_1+R_2}\left(1 - \frac{R_F R_1}{R_2 R_3}\right)} \tag{1.36}$$

This is often expressed in decibels by the relation $20\log(CMRR)$.

Example 10 *For the diff-amp circuit of Fig. 1.18, solve for v_O, the current i, the resistance seen by the generator, the input voltages v_{I1} and v_{I2}, and the common-mode input voltage.*

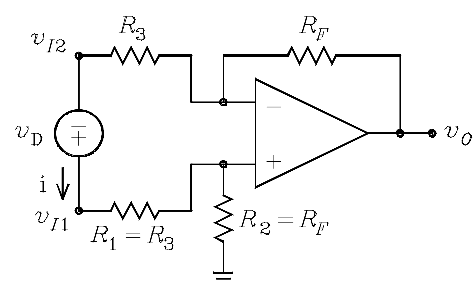

Figure 1.18: Circuit for Example 10.

Solution. By Eq. (1.28), v_O is given by

$$v_O = \frac{R_F}{R_3} v_D$$

Because there is a virtual short circuit between the op-amp inverting and non-inverting inputs, it follows that i is given by

$$i = \frac{v_D}{2R_3}$$

Thus the generator sees the resistance $2R_3$.

To solve for v_{I1} and v_{I2}, we can write

$$v_{I1} = i\,(R_3 + R_F) = \frac{v_D}{2R_3}(R_3 + R_F) = \frac{v_D}{2}\left(\frac{R_F}{R_3} + 1\right)$$

$$v_{I2} = v_{I1} - v_D = \frac{v_D}{2}\left(\frac{R_F}{R_3} - 1\right)$$

The common-mode component of v_{I1} and v_{I2} is given by

$$v_{CM} = \frac{v_{I1} + v_{I2}}{2} = \frac{R_F}{R_3} \times \frac{v_D}{2} = \frac{v_O}{2}$$

Thus the op amp forces a common-mode voltage at the two diff-amp inputs that is equal to one-half the output voltage.

1.5.5 The Switch Hitter

The single op-amp diff amp circuit of Fig. 1.19(a) is known as a *switch hitter*. The signal applied to the v_+ op-amp input is taken from the wiper of a potentiometer. To solve for the output voltage as a function of the position of the wiper, we denote the potentiometer resistance from wiper to ground by xR_p, where $0 \le x \le 1$. By voltage division, it follows that $v_+ = xv_I$. The circuit is redrawn in Fig. 1.19(b) with separate sources driving the inverting and the non-inverting inputs. By superposition of the two sources, the output voltage can be written

$$v_O = 2v_+ - v_I = (2x - 1)\, v_I \tag{1.37}$$

where Eqs. (1.3) and (1.10) have been used. It follows that the voltage gain of the circuit is $2x - 1$. The gain is -1 for $x = 0$, 0 for $x = 0.5$, and $+1$ for $x = 1$. Thus the gain can be varied from -1 through 0 to $+1$ as the position of the potentiometer wiper is varied. Such a circuit might be used when it is desired to change the polarity of a signal when it is summed with other signals, e.g. in a sound mixing console.

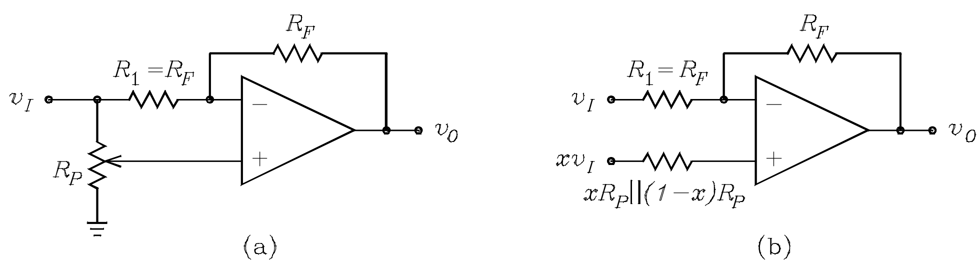

Figure 1.19: (a) Switch hitter. (b) Equivalent circuit.

1.5.6 The Two Op-Amp Diff-Amp

A two op-amp diff amp is shown in Fig. 1.20. By superposition, the output voltage is given by

$$v_O = -\frac{R_{F2}}{R_3} v_{01} - \frac{R_{F2}}{R_2} v_{I2} = \frac{R_{F1} R_{F2}}{R_1 R_3} v_{I1} - \frac{R_{F2}}{R_2} v_{I2} \tag{1.38}$$

where Eq. (1.3) has been used. The circuit operates as a true diff amp if one of two conditions is satisfied. One condition is $R_1 = R_{F1}$ and $R_3 = R_2$. The other is $R_1 = R_2$ and $R_{F1} = R_3$. Under either condition, v_O is given by

$$v_O = \frac{R_{F2}}{R_2}(v_{I1} - v_{I2}) \tag{1.39}$$

The input resistance to the v_{I1} input is R_1. The input resistance to the v_{I2} input is R_2. The output resistance is zero.

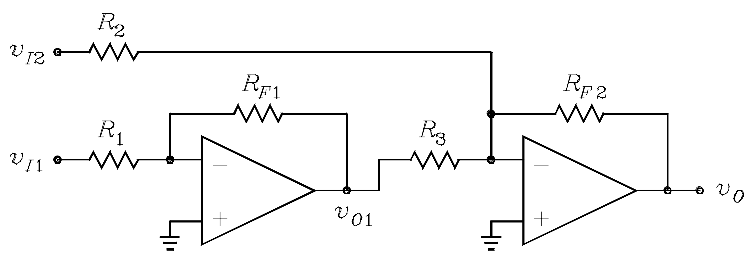

Figure 1.20: Two op-amp diff amp.

The two op-amp diff amp has several advantages over the single op-amp diff amp. The input resistance to either input is not a function of the voltage at the other input. The common-mode voltage at the inputs is not a function of the output voltage. When the circuit is used as a true diff amp, the differential voltage gain can be varied by varying a single resistor. This resistor is R_{F2}. The single op-amp diff amp does not have this feature.

Example 11 *Design a two op-amp diff amp which has a differential voltage gain of* 20*, a common-mode voltage gain of* 0*, and an input resistance to each input of* 10 *k*Ω.

Solution. For the circuit of Fig. 1.20, the input resistance specifications can be met with $R_1 = R_2 = 10$ kΩ. For the differential gain specification, it follows from Eq. (1.39) that $R_{F2}/R_2 = 20$. Thus we must have $R_{F2} = 200$ kΩ. For a common-mode gain of zero, we must have either $R_1 = R_{F1}$ and $R_3 = R_2$ or $R_1 = R_2$ and $R_{F1} = R_3$. Because we have already specified that $R_1 = R_2$, we must have $R_{F1} = R_3$. The value for these resistors is arbitrary. Let $R_{F1} = R_3 = 200$ kΩ.

1.5.7 The Instrumentation Amplifier

The diff-amp circuit of Fig. 1.21 is known as an *instrumentation amplifier*. In some applications, it is called an *active transformer*. To solve for v_O, we use superposition of the inputs v_{I1} and v_{I2}. With $v_{I2} = 0$, the v_- terminal of op amp 2 is at virtual ground and op amp 1 operates as a non-inverting amplifier. By Eq. (1.10), its output voltage is given by

$$v_{O1} = \left(1 + \frac{R_{F1}}{R_1}\right) v_{I1} \tag{1.40}$$

Because there is a virtual short circuit between the v_+ and v_- inputs of op amp 1, the voltage at the lower node of R_1 is v_{I1}. It follows that op amp 2 operates as an inverting amplifier. By Eq. (1.3), its output voltage is given by

$$v_{O2} = -\frac{R_{F1}}{R_1} v_{I1} \tag{1.41}$$

Op-amp 3 operates as a true diff amp. By Eq. (1.28), its output voltage is given by

$$v_O = \frac{R_{F2}}{R_2}(v_{O1} - v_{O2}) = \frac{R_{F2}}{R_2}\left(1 + 2\frac{R_{F1}}{R_1}\right) v_{I1} \tag{1.42}$$

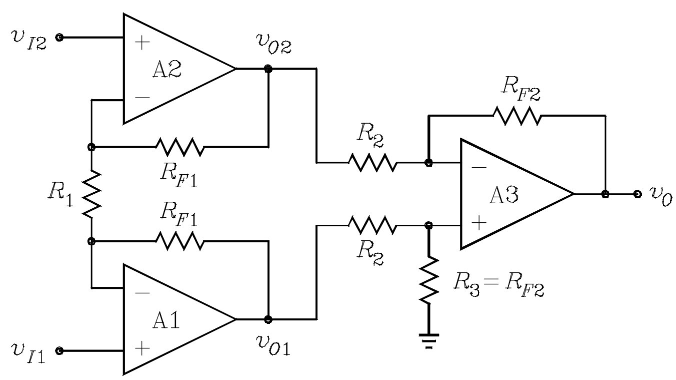

Figure 1.21: Instrumentation amplifier.

Similarly, for $v_{I1} = 0$, v_O is given by

$$v_O = -\frac{R_{F2}}{R_2}\left(1 + 2\frac{R_{F1}}{R_1}\right) v_{I2} \tag{1.43}$$

By superposition, the total output voltage is

$$v_O = \frac{R_{F2}}{R_2}\left(1 + 2\frac{R_{F1}}{R_1}\right)(v_{I1} - v_{I2}) \tag{1.44}$$

This is the voltage output of a true diff amp. The input resistance to each input of the amplifier is infinite. The output resistance is zero.

The instrumentation amplifier can be thought of as the cascade connection of two amplifiers. The first stage consists of op amps 1 and 2. Let its voltage gain be denoted by A_1. The second stage consists of op amp 3. Let its voltage gain be denoted by A_2. The two gains are given by

$$A_1 = \frac{v_{O1} - v_{O2}}{v_{I1} - v_{I2}} = 1 + 2\frac{R_{F1}}{R_1} \tag{1.45}$$

$$A_2 = \frac{v_O}{v_{O1} - v_{O2}} = \frac{R_{F2}}{R_2} \tag{1.46}$$

It can be seen that A_1 represents the ratio of a differential output voltage to a differential input voltage and A_2 represents the ratio of a single-ended output voltage to a differential input voltage.

The instrumentation amplifier is used in applications where a true diff amp is required with a very high input resistance and a very high common-mode rejection ratio. A potentiometer connected as a variable resistor in series with R_1 can be used to adjust the voltage gain. A potentiometer connected as a variable resistor in series with R_3 can be used to optimize the $CMRR$. To do this experimentally, the two inputs are connected together and a common-mode signal voltage applied. The potentiometer in series with R_3 is adjusted for minimum output voltage.

Example 12 *Design an instrumentation amplifier which has a differential voltage gain of* 100 *(a decibel gain of* 40 *dB) and a common-mode voltage gain of zero.*

Solution. The gain of 100 must be divided between the two stages of the circuit. It is convenient to give the input stage, consisting of op amps 1 and 2, a gain of 10 and the second stage, consisting of op amp 3, a gain of 10. Using Eqs. (1.45) and (1.46), we can write the two design equations

$$1 + 2\frac{R_{F1}}{R_1} = 10 \qquad \text{and} \qquad \frac{R_{F2}}{R_2} = 10$$

With two equations and four unknowns, it is necessary to assign values to two of the resistors. Let $R_{F1} = R_{F2} = 10$ kΩ. It follows that $R_2 = 1$ kΩ and $R_1 = 10/4.5$ kΩ $= 2.22$ kΩ.

1.5.8 The Differential Output Amplifier

Figure 1.22 shows the circuit diagram of a *differential output amplifier*. This circuit has two output voltages which have opposite polarities. That is, if v_{O1} is positive, v_{O2} is negative, and vice versa. Because the lower node of resistor R_1 is at virtual ground, Eq. (1.10) can be used to write for v_{O1}

$$v_{O1} = \left(1 + \frac{R_{F1}}{R_1}\right) v_I \tag{1.47}$$

Because there is a virtual short between the inverting and non-inverting inputs to op amp 1, the upper node of R_1 sees the input voltage v_I. Thus Eq. (1.3) can be use to write for v_{O2}

$$v_{O2} = -\frac{R_{F2}}{R_1} v_I \tag{1.48}$$

In most applications of the differential output amplifier, the condition $v_{O2} = -v_{O1}$ is desired. When this is satisfied, the amplifier is said to be a *balanced* differential output amplifier. This requires the condition $1 + R_{F1}/R_1 = R_{F2}/R_1$ which reduces to

$$R_{F1} = R_{F2} - R_1 \tag{1.49}$$

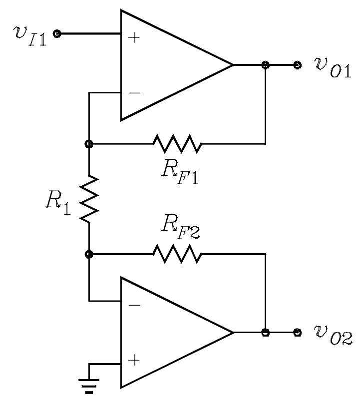

Figure 1.22: Differential output amplifier.

In this case, the output voltages can be written

$$v_{O1} = -v_{O2} = \frac{R_{F2}}{R_1} v_I \tag{1.50}$$

The differential output voltage is given by

$$v_O = v_{O1} - v_{O2} = \frac{2R_{F2}}{R_1} v_I \tag{1.51}$$

Example 13 *Design a balanced differential output amplifier with an open-circuit voltage gain of* 4*, an input resistance of* 10 *k*Ω*, and a balanced output resistance of* 600 Ω*. The amplifier is to drive a* 600 Ω *load. If the maximum peak output voltage from each op amp is* ±12 *V, calculate the maximum peak load voltage and the output level in dBm for a sine wave input signal. (The dBm is the decibel output power referenced to the power $P_{ref} = 1$ mW.)*

Solution. The circuit diagram is shown in Fig. 1.23. For the input resistance specification, we have $R_i = 10$ kΩ. For an open-circuit voltage gain of 4, it follows from Eq. (1.51) that $2R_{F2}/R_1 = 4$. This can be satisfied by choosing $R_{F2} = 20$ kΩ and $R_1 = 10$ kΩ. Eq. (1.49) gives $R_{F1} = 10$ kΩ. To achieve a 600 Ω balanced output resistance, we must have $R_{O1} = R_{O2}$ and $R_{O1} + R_{O2} = 600$. It follows that $R_{O1} = R_{O2} = 300$ Ω. If the voltage output of op amp 1 peaks at +12 V, the voltage output from op amp 2 peaks at −12 V and the peak load voltage is $v_P = 24 \times 600/(600 + 600) = 12$ V, where a voltage divider relation has been used. The output level in dBm is given by

$$\text{Output Level} = 10 \log \left[\frac{v_P^2 / 2R_L}{P_{ref}} \right] = 10 \log \left[\frac{12^2/1200}{0.001} \right] = 20.8 \text{ dBm}$$

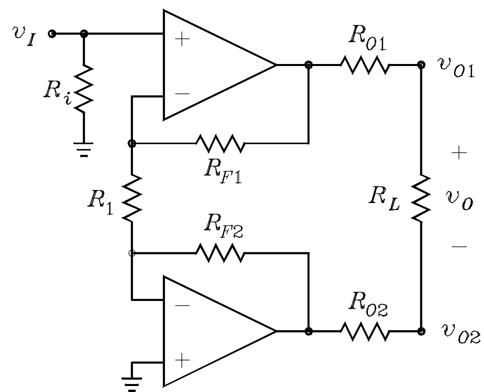

Figure 1.23: Circuit for Example 13.

1.6 Op-Amp Differentiators

1.6.1 The Ideal Differentiator

A *differentiator* has an output voltage that is proportional to the time derivative of its input voltage. Fig. 1.24 gives the circuit diagram of the op-amp differentiator. The circuit is similar to the inverting amplifier in Fig. 1.3 with the exception that resistor R_1 is replaced by a capacitor. It follows that Eq. (1.3) can be used to solve for the voltage gain transfer function by replacing R_1 with the impedance of the capacitor. The transfer function is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{(1/C_1 s)} = -R_F C_1 s \tag{1.52}$$

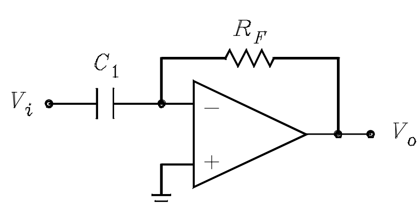

Figure 1.24: Ideal differentiator.

Because a multiplication by s in the complex frequency domain is equivalent to a differentiation in the time domain, it follows from the above equation that the time domain output voltage is given by

$$v_O(t) = -R_F C_1 \frac{dv_I(t)}{dt} \tag{1.53}$$

Thus the circuit has the transfer function of an inverting differentiator with the gain constant $R_F C_1$. Because the gain constant has the units of seconds, it is called the *differentiator time constant*. The output resistance of the circuit is zero. The input impedance transfer function is that of the capacitor C_1 to virtual ground given by

$$Z_{\text{in}} = \frac{1}{C_1 s} \tag{1.54}$$

With $s = j\omega$, it follows that $|Z_{\text{in}}| \to 0$ as ω becomes large. This is a disadvantage because a low input impedance can cause large currents to flow in the input circuit.

1.6.2 The Modified Differentiator

With $s = j\omega$, it follows from Eq. (1.52) that the magnitude of the voltage gain of the differentiator is $\omega R_F C_1$. For large ω, the gain can get very high. This is a disadvantage in circuits where out-of-band high-frequency noise can be a problem. To limit the high-frequency gain, a resistor can be used in series with C_1 as shown in Fig. 1.25(a). This also has the advantage that the high-frequency input impedance does not approach zero. At high frequencies where C_1 is a short, the gain magnitude is limited to the value R_F/R_1 and the input impedance approaches R_1. The voltage gain transfer function of the circuit with R_1 is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + 1/C_1 s} = -R_F C_1 s \times \frac{1}{1 + R_1 C_1 s} \tag{1.55}$$

This is of the form of the transfer function of an ideal differentiator multiplied by the transfer function of a low-pass filter which has a pole time constant $R_1 C_1$.

The Bode magnitude plot for Eq. (1.55) is given in Fig. 1.25(b). For $\omega << 1/R_1 C_1$, the asymptotic plot exhibits a slope of +1 dec/dec and the gain is given by $V_o/V_i \cong -j\omega R_F C_1$. At $\omega = 1$, $|V_o/V_i| \cong R_F C_1$. For $\omega >> 1/R_1 C_1$, the asymptotic slope is 0 and the gain shelves at the value R_F/R_1. It follows that the circuit with R_1 acts as a differentiator only for frequencies such that $\omega << 1/R_1 C_1$. The input impedance transfer function is given by

$$Z_{in} = R_1 + \frac{1}{C_1 s} = R_1 \times \frac{1 + R_1 C_1 s}{R_1 C_1 s} \tag{1.56}$$

This is of the form of a constant multiplied by the reciprocal of a high-pass transfer function. For $s = j\omega$, $|Z_{\text{in}}| \to R_1$ as ω becomes large.

Example 14 *Design a modified differentiator which has a time constant of* 10 *msec and a pole frequency of* 1 *kHz. For a* 1 *V peak sine-wave input signal at* 100 *Hz, calculate the peak sine wave output voltage and the relative phase of the output voltage.*

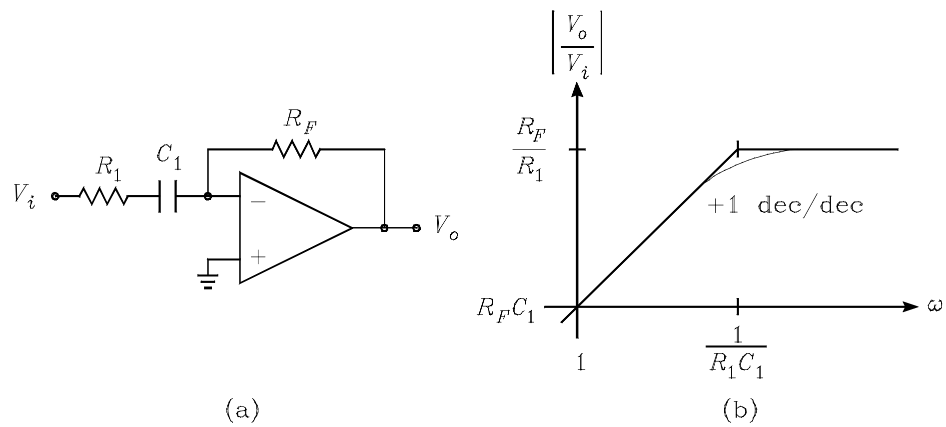

Figure 1.25: (a) Modified differentiator. (b) Bode plot for $|V_o/V_i|$.

Solution. The circuit diagram is shown in Fig. 1.25(a). To meet the time constant specification, we have $R_F C_1 = 0.01$. If we let $C_1 = 0.1\ \mu\text{F}$, it follows that $R_F = 100\ \text{k}\Omega$. For a pole frequency of 1000 Hz, we must have $R_1 C_1 = 1/2\pi 1000$. Thus $R_1 = 10,000/2\pi = 1.59\ \text{k}\Omega$. From Eq. (1.55), the voltage gain at $f = 100$ Hz is given by

$$\left|\frac{V_o}{V_i}\right| = \left|-\frac{R_F C_1 (j2\pi 100)}{1 + j2\pi 100 R_1 C_1}\right| = \frac{0.01 \times 2\pi 100}{\sqrt{1 + 0.1^2}} = 6.25$$

For a 1 V peak input sine wave at 100 Hz, the peak output voltage is 6.25 V.

It follows from Eq. (1.55) that the phase of the output signal with respect to the input signal is

$$\varphi = +90^\circ - \tan^{-1}(2\pi 100 R_1 C_1) = 84.3^\circ$$

A perfect differentiator has a phase of $+90^\circ$. Thus there is a phase error of -5.7°. Note that the negative sign in Eq. (1.55) does not affect the phase. This is because a negative sign indicates an inversion whereas a phase shift is associated with a shift in time. If a sine wave is observed on the screen of an oscilloscope, an inversion flips the sine wave about the time axis. A phase shift causes the position of the zero crossings to shift along the time axis.

1.7 Op-Amp Integrators

1.7.1 The Ideal Inverting Integrator

An *integrator* has an output voltage that is proportional to the time integral of its input voltage. The circuit for the integrator can be obtained by interchanging the resistor and the capacitor in the differentiator of Fig. 1.24. It is shown in Fig. 1.26. The voltage gain transfer function is obtained from Eq. (1.3) by replacing R_F with the complex impedance of the capacitor C_F to obtain

$$\frac{V_o}{V_i} = -\frac{(1/C_F s)}{R_1} = -\frac{1}{R_1 C_F s} \tag{1.57}$$

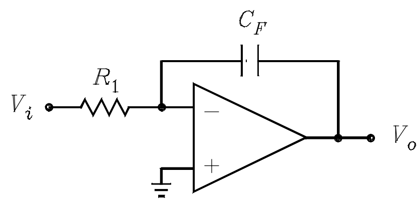

Figure 1.26: Inverting integrator.

Because a division by s in the complex frequency domain is equivalent to an integration in the time domain, it follows from this equation that the time domain output voltage is given by

$$v_O(t) = -\frac{1}{R_1 C_F}\int_{-\infty}^{t} v_I(t')\,dt' \tag{1.58}$$

The circuit has the transfer function of an inverting integrator with the gain constant $1/R_1C_F$. Because R_1C_F has the units of seconds, it is called the *integrator time constant*. The input resistance to the circuit is R_1. The output resistance is zero.

1.7.2 The Modified Inverting Integrator

At zero frequency, C_F is an open circuit and the op amp in the integrator loses feedback. For non-ideal op amps, this can cause an undesirable dc offset voltage at the output. To provide feedback at dc, a resistor can be used in parallel with C_F as shown in Fig. 1.27(a). At low frequencies where C_F is an open circuit, the magnitude of the voltage gain is limited to the value R_F/R_1. The transfer function for the voltage gain of the integrator with R_F is given by

$$\frac{V_o}{V_i} = -\frac{R_F\| (1/C_F s)}{R_1} = -\frac{R_F}{R_S}\times\frac{1}{1+R_F C_F s} = -\frac{1}{R_1 C_F s}\times\frac{R_F C_F s}{1+R_F C_F s} \tag{1.59}$$

where (1.3) has been used. This is of the form of the transfer function of an ideal integrator multiplied by the transfer function of a high-pass filter which has the pole time constant R_FC_F. The Bode magnitude plot is given in Fig. 1.27(b). For $\omega << 1/R_FC_F$, the plot exhibits a slope of 0. For $\omega >> 1/R_FC_F$, the slope is -1 dec/dec. The circuit with R_F acts as an integrator only for frequencies such that $\omega >> 1/R_FC_F$.

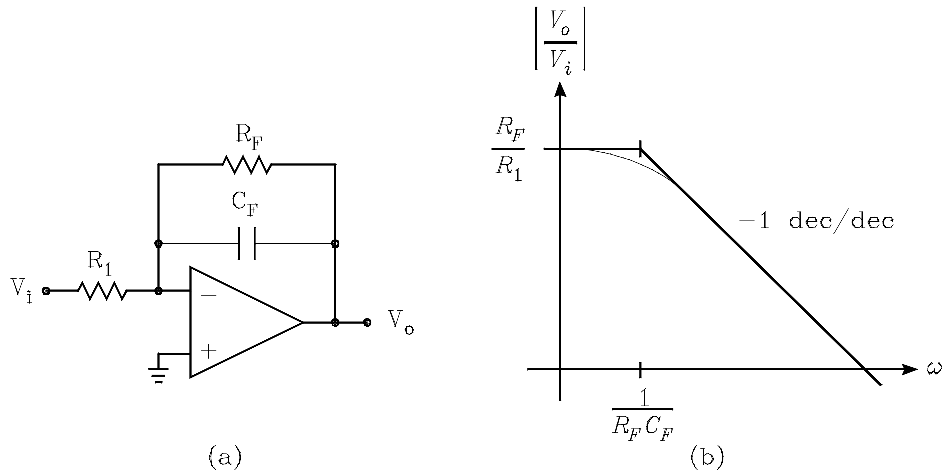

Figure 1.27: (a) Modified inverting integrator. (b) Bode plot for $|V_o/V_i|$.

Example 15 *Design a modified integrator which has a time constant of* 0.1 *sec and a pole frequency of* 1 *Hz. For a* 1 *V peak sine-wave input signal at* 10 *Hz, calculate the peak sine-wave output voltage and the relative phase of the output voltage.*

Solution. The circuit diagram is shown in Fig. 1.27(a). For the time constant specification, we have $R_1 C_F = 0.1$. If we let $C_F = 0.1\ \mu$F, it follows that $R_1 = 1$ MΩ. For the pole frequency of 1 Hz, we must have $R_F C_F = 1/2\pi$. This gives $R_F = 1/(2\pi \times 0.1\mu) = 1.59$ MΩ. From Eq. (1.59), the gain magnitude at $f = 10$ Hz is

$$\left|\frac{V_o}{V_i}\right| = \left|-\frac{1}{j2\pi 10 R_1 C_F} \times \frac{j2\pi 10 R_F C_F}{1 + j2\pi 10 R_F C_F}\right| = \frac{1.59}{\sqrt{1+10^2}} = 0.158$$

For a 1 V peak input sine wave at 100 Hz, the peak output voltage is 0.158 V.

It follows from Eq. (1.59) that the phase of the output signal with respect to the input signal is given by

$$\varphi = -\tan^{-1}(2\pi 10 R_F C_F) = -84.3°$$

A perfect integrator has a phase of $-90°$. Thus there is a phase error of $+5.7°$. As is discussed in Example 15, the negative sign in Eq. (1.59) indicates that the output signal is inverted with respect to the input signal which does not affect the phase.

1.7.3 The Non-Inverting Integrator

The *non-inverting integrator* is shown in Fig. 1.28(a). The voltage output from the op amp is fed back to both its inverting input and to its non-inverting input. Thus the circuit has both positive and negative feedback. To solve for the voltage gain transfer function, it is convenient to make two Norton equivalent circuits at the V_+ node, one looking toward the input through the left R and the other looking toward the output through the right R. The circuit obtained is shown in Fig. 1.28(b), where the two parallel resistors are combined into a single resistor of value $R/2$. Because there is a virtual short between the V_+ and the V_- inputs, we can write

$$\frac{V_o}{2} = \left[\frac{V_i}{R} + \frac{V_o}{R}\right] \times \left[\frac{R}{2}\| \frac{1}{Cs}\right] = (V_i + V_o)\frac{1}{1 + RCs/2} \tag{1.60}$$

This equation can be solved for the voltage gain to obtain

$$\frac{V_o}{V_i} = \frac{2}{RCs} \tag{1.61}$$

This is the transfer function of a non-inverting integrator with the gain constant $2/RC$. The time constant is $RC/2$.

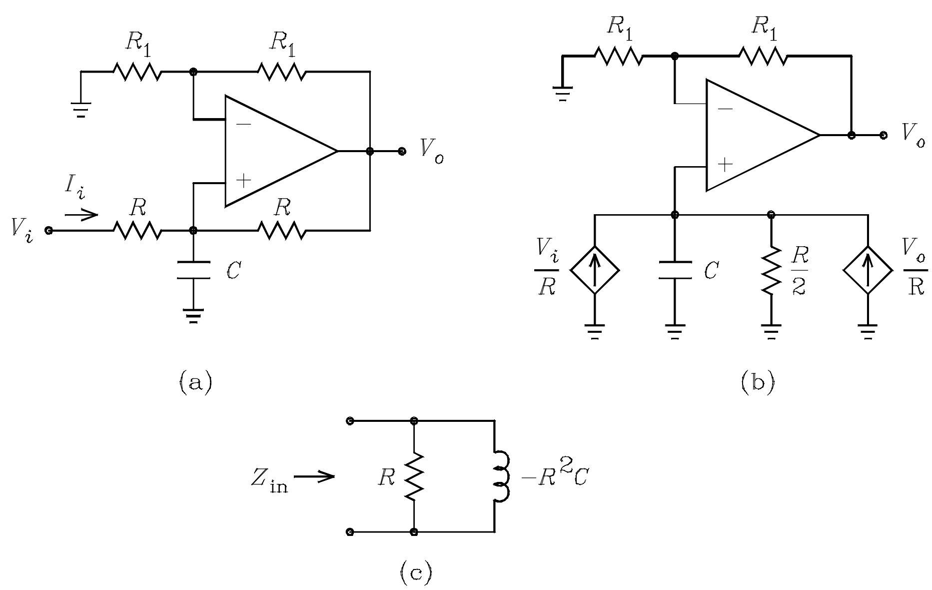

Figure 1.28: (a) Non-inverting integrator. (b) Equivalent circuit for V_o. (c) Equivalent circuit for Z_{in}.

The input current in the circuit of Fig. 1.28(a) is given by

$$I_i = \frac{V_i - V_+}{R} = \frac{V_i - V_-}{R} = \frac{V_i}{R}\left(1 - \frac{V_-}{V_i}\right) = \frac{V_i}{R}\left(1 - \frac{1}{RCs}\right) \tag{1.62}$$

where $V_- = V_o/2 = V_i/RCs$ has been used. This equation can be solved for the input impedance to obtain

$$Z_{in} = \frac{V_i}{I_i} = \frac{R\left(-R^2Cs\right)}{R + (-R^2Cs)} \tag{1.63}$$

The equivalent circuit which has this impedance is a resistor R in parallel with a negative inductor $-R^2C$. The equivalent circuit is given in Fig. 1.28(c). Because the inductor is a short circuit at zero frequency, it follows that the input impedance to the circuit is zero for a dc source.

Example 16 *The non-inverting integrator of Fig. 1.28(a) has the circuit element values* $R = 1$ *k*Ω *and* $C = 1$ μ*F. For a sine wave input signal, calculate the voltage gain of the circuit at the frequency* $f = 100$ *Hz. In addition, calculate numerical values for the circuit elements in the equivalent circuit for the input impedance.*

Solution. The gain at $f = 100$ Hz is calculated from Eq. (1.61) as follows:

$$\frac{V_o}{V_i} = \frac{2}{10^3 \times 10^{-6}} \times j2\pi 100 = -j3.17$$

From Eq. (1.63), it follows that the input impedance circuit consists of a 1000 Ω resistor to ground in parallel with a negative inductor to ground having the value $-1000^2 \times 10^{-6} = -1$ H.

1.8 Low-Pass Amplifiers

1.8.1 The Inverting Low-Pass Amplifier

This section covers several of the many op-amp circuits which have a voltage gain transfer function that is of the form of single-pole low-pass and low-pass shelving transfer functions. Fig. 1.29(a) shows the circuit diagram of an *inverting low-pass amplifier*. The voltage gain is obtained from Eq. (1.3) by replacing R_F with $R_F \| (1/C_F s)$. It is given by

$$\frac{V_o}{V_i} = -\frac{R_F \| (1/C_F s)}{R_1} = -\frac{R_F}{R_1} \times \frac{1}{1 + R_F C_F s} \tag{1.64}$$

This is of the form of a gain constant $-R_F/R_1$ multiplied by a low-pass transfer function having a pole time constant $R_F C_F$. The Bode plot $|V_o/V_i|$ is given in Fig. 1.29(b). The input resistance of the circuit is R_1. The output resistance is zero.

Example 17 *Design an inverting low-pass amplifier circuit which has an input resistance of* 10 *k*Ω*, a low-frequency voltage gain of* -10*, and a pole frequency of* 10 *kHz.*

Solution. The circuit diagram is shown in Fig. 1.29(a). For an input resistance of 10 kΩ, we have $R_1 = 10$ kΩ. The transfer function is given by Eq. (1.64). For a low-frequency gain of -10, we have $R_F = 10R_1 = 100$ kΩ. For a pole frequency of 10 kHz, we have $C_F = 1/\left(2\pi 10^4 R_F\right) = 159$ pF.

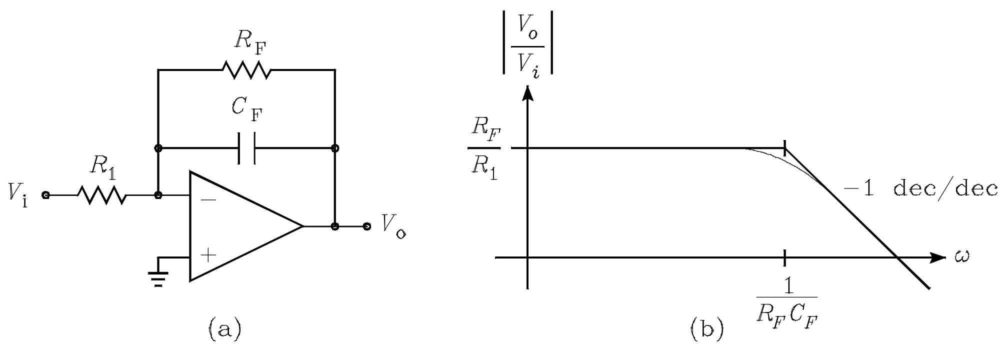

Figure 1.29: (a) Inverting low-pass amplifier. (b) Bode plot for $|V_o/V_i|$.

A second inverting low-pass amplifier is shown in Fig. 18. The currents I_1, I_2, and I_F are given by

$$I_1 = \frac{V_i}{R_1 + (1/Cs)\,\|R_2} \tag{1.65}$$

$$I_2 = I_1 \frac{1/Cs}{R_2 + 1/Cs} = I_1 \frac{1}{1 + R_2 Cs} \tag{1.66}$$

$$I_F = \frac{V_o}{R_F} \tag{1.67}$$

where we assume that the V_- op-amp input is at virtual ground and current division has been used for I_2. The voltage gain is obtained by setting $I_2 + I_F = 0$ to obtain

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + R_2} \times \frac{1}{1 + (R_1\|R_2)\,Cs} \tag{1.68}$$

This is of the form of a gain constant $-R_F/\,(R_1 + R_2)$ multiplied by a low-pass transfer function having a pole time constant $(R_1\|R_2)\,C$. The Bode plot for $|V_o/V_i|$ is given in Fig. 18(b).

The output resistance of the circuit is zero. The input impedance is given by

$$Z_{\text{in}} = R_1 + \left(\frac{1}{Cs}\right)\|R_2 = (R_1 + R_2)\,\frac{1 + (R_1\|R_2)\,Cs}{1 + R_2 Cs} \tag{1.69}$$

This is in the form of a low-pass shelving function having a pole time constant R_2C and a zero time constant $(R_1\|R_2)\,C$. The Bode plot for $|Z_{\text{in}}|$ is given in Fig. 18(c). The low-frequency impedance is $R_1 + R_2$. As frequency is increased, the impedance decreases and shelves at the value R_1.

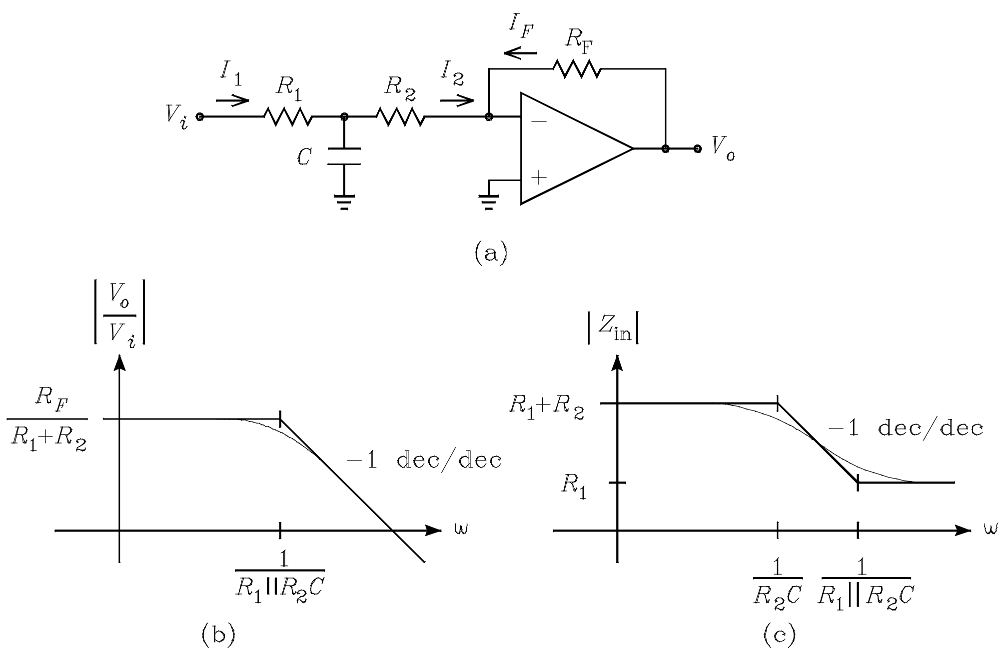

Figure 1.30: (a) Inverting low-pass amplifier. (b) Bode plot for $|V_o/V_i|$. (c) Bode plot for $|Z_{\text{in}}|$.

Example 18 *Specify the circuit element values for the circuit of Fig. 18(a) for an inverting voltage gain of unity and a pole time constant of* 75 μ*s. What is the pole frequency in the transfer function?*

Solution. Let $C = 0.01$ μF and $R_2 = R_1$. It follows from Eq. (1.68) that $(R_1 \| R_2)\, C = (R_1/2)\, C = 75 \times 10^{-6}$. Solution for R_1 and R_2 yields $R_1 = R_2 = 15$ kΩ. For an inverting voltage gain of unity, we must have $R_F = R_1 + R_2 = 30$ kΩ. The pole frequency in the transfer function has the frequency $f = 1/\left(2\pi \times 75 \times 10^{-6}\right) = 2.12$ kHz.

1.8.2 The Non-Inverting Low-Pass Amplifier

Fig. 1.31(a) shows a *non-inverting low-pass amplifier* consisting of a non-inverting amplifier with a RC low-pass filter at its input. The voltage gain transfer function is given by

$$\frac{V_o}{V_i} = \frac{V_+}{V_i} \times \frac{V_o}{V_+} = \frac{1/Cs}{R + 1/Cs}\left(1 + \frac{R_F}{R_1}\right) = \left(1 + \frac{R_F}{R_1}\right)\frac{1}{1 + RCs} \tag{1.70}$$

where a voltage division and Eq. (1.10) have been used. This is of the form of a gain constant $1 + R_F/R_1$ multiplied by the transfer function of a low-pass filter having a pole time constant RC. The Bode magnitude plot is given in Fig. 1.31(b). The output resistance of the circuit is zero. The input impedance is given by

$$Z_{\text{in}} = R + \frac{1}{Cs} = R \times \frac{1 + RCs}{RCs} \tag{1.71}$$

This is of the form of a constant multiplied by the reciprocal of a high-pass transfer function.

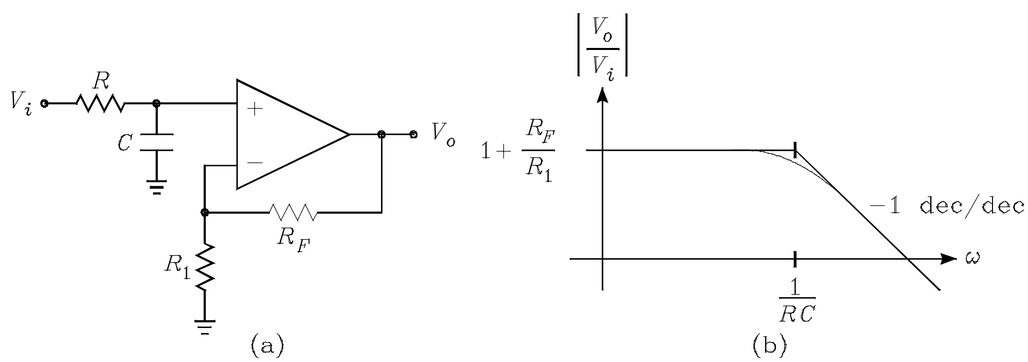

Figure 1.31: (a) Non-inverting low-pass amplifier. (b) Bode plot for $|V_o/V_i|$.

Example 19 *The non-inverting amplifier of Fig. 1.31(a) is to be designed for a voltage gain of* 12*. The input low-pass filter is to have a cutoff frequency of* 100 *kHz. Specify the element values for the circuit.*

Solution. To meet the cutoff frequency specification, it follows from Eq. (1.70) that $RC = 1/\left(2\pi 10^5\right)$. Let $C = 510$ pF. It follows that $R = 3.12$ kΩ. For a gain of 12, we must have $1 + R_F/R_1 = 12$. If we choose $R_1 = 1$ kΩ, it follows that $R_F = 11$ kΩ.

1.8.3 The Non-Inverting Low-Pass Shelving Amplifier

A *non-inverting low-pass shelving amplifier* is shown in Fig. 1.32(a). The voltage gain is obtained from Eq. (1.10) by replacing R_F with $R_F \| (1/C_F s)$. It is given by

$$\frac{V_o}{V_i} = 1 + \frac{R_F \| (1/C_F s)}{R_1} = \left(1 + \frac{R_F}{R_1}\right) \times \frac{1 + (R_F \| R_1) C_F s}{1 + R_F C_F s} \tag{1.72}$$

This is of the form of a gain constant $1 + R_F/R_1$ multiplied by a low-pass shelving transfer function having a pole time constant $R_F C_F$ and a zero time constant $(R_F \| R_1) C_F$. The Bode plot for $|V_o/V_i|$ is shown in Fig. 1.32(b). The low-frequency gain is $1 + R_F/R_1$. As frequency is increased, the gain decreases and shelves at unity.

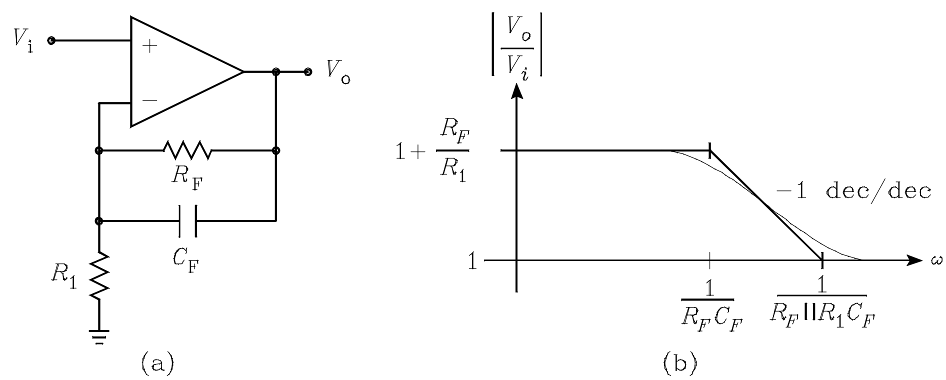

Figure 1.32: (a) Non-inverting low-pass shelving amplifier. (b) Bode plot for $|V_o/V_i|$.

Example 20 *The circuit of Fig. 1.32(a) is to be designed for a low-frequency gain of* 2 *(a* 6 *dB boost). The zero frequency in the transfer function is to be* 100 *Hz. Specify the circuit element values and calculate the frequency at which the voltage gain is* 3 *dB.*

Solution. For a low-frequency gain of 2, it follows from Eq. (1.72) that $1 + R_F/R_1 = 2$ which gives $R_F = R_1$. For the zero in the transfer function to be at 100 Hz, we have $(R_F \| R_1) C_F = 1/(2\pi 100)$. If we choose $C_F = 0.1\ \mu$F, it follows that $R_1 = R_F = 31.8$ kΩ. With $s = j2\pi f$, the transfer function can be written

$$\frac{V_o}{V_i} = 2 \frac{1 + jf/100}{1 + jf/50}$$

At the 3 dB boost frequency, $|V_o/V_i|^2 = 1/2$. This condition gives

$$\frac{1 + (f/100)^2}{1 + (f/50)^2} = \frac{1}{2}$$

This is satisfied for $f = 100/\sqrt{2} = 70.7$ Hz.

1.9 High-Pass Amplifiers

1.9.1 The Inverting High-Pass Amplifier

This section covers several of the many op-amp circuits which have a voltage gain that is of the form of high-pass and high-pass shelving transfer functions. Fig. 1.33(a) shows an *inverting high-pass amplifier*. The voltage gain is obtained from Eq. (1.3) by replacing R_1 with $R_1 + 1/C_1 s$. It is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + 1/C_1 s} = -\frac{R_F C_1 s}{1 + R_1 C_1 s} = -\frac{R_F}{R_1} \times \frac{R_1 C_1 s}{1 + R_1 C_1 s} \tag{1.73}$$

This is of the form of a gain constant $-R_F/R_1$ multiplied by a high-pass transfer function having a pole time constant $R_1 C_1$. The Bode plot for $|V_o/V_i|$ is given in Fig. 1.33(b). The output resistance of the circuit is zero. The input impedance is given by

$$Z_{\text{in}} = R_1 + \frac{1}{C_1 s} = \frac{1 + R_1 C_1 s}{C_1 s} = R_1 \times \frac{1 + R_1 C_1 s}{R_1 C_1 s} \tag{1.74}$$

This is of the form of a constant multiplied by the reciprocal of a high-pass transfer function.

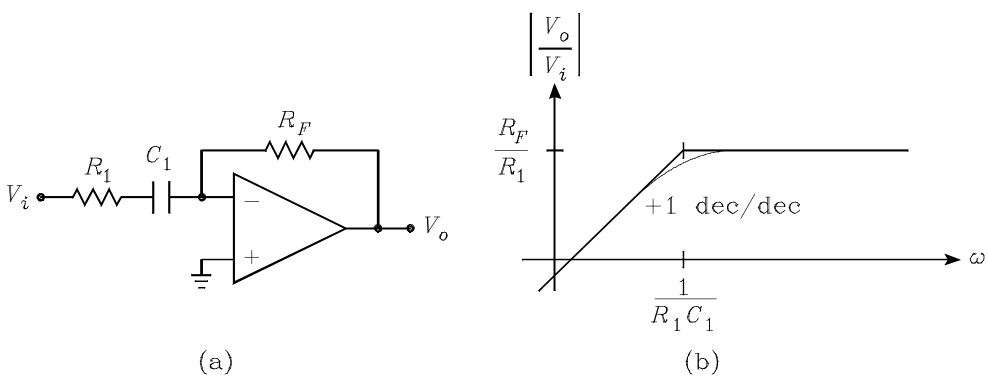

Figure 1.33: (a) Inverting high-pass amplifier. (b) Bode plot for $|V_o/V_i|$.

Example 21 *Design an inverting high-pass amplifier circuit which has a gain of* -10 *and a pole time constant of* 500 μ*sec. The input impedance to the circuit is to be* 10 kΩ *or higher. Calculate the lower half-power cutoff frequency of the amplifier.*

Solution. The circuit diagram is shown in Fig. 1.33(a). The voltage-gain transfer function is given by Eq. (1.73). For the gain specification, we must have $R_F/R_1 = 10$. For the pole time constant specification, we must have $R_1 C_1 = 500 \times 10^{-6}$. Because there are three unknowns and only two equations, one of the circuit elements must be specified before the others can be calculated. Eq. (1.74) shows that the lowest value of the input impedance is R_1. Thus we must have $R_1 \geq 10$ kΩ. If $R_1 = 10$ kΩ, it follows that $C_1 = 0.05$ μF. Let us choose $C_1 = 0.033$ μF. It follows that $R_1 = 15.2$ kΩ and $R_2 = 152$ kΩ. The lower half-power cutoff frequency of the amplifier is $f = 1/\left(2\pi \times 500 \times 10^{-6}\right) = 318$ Hz.

1.9.2 The Non-Inverting High-Pass Amplifier

Fig. 1.341.9.2(a) shows a *non-inverting high-pass amplifier*. The voltage gain transfer function is given by

$$\frac{V_o}{V_i} = \frac{V_+}{V_i} \times \frac{V_o}{V_+} = \frac{R}{R + 1/Cs}\left(1 + \frac{R_F}{R_1}\right) = \left(1 + \frac{R_F}{R_1}\right)\frac{RCs}{1 + RCs} \tag{1.75}$$

where voltage division and Eq. (1.10) have been used. This is of the form of a gain constant $1+R_F/R_1$ multiplied by a single-pole high-pass transfer function having a pole time constant RC. The Bode plot for $|V_o/V_i|$ is given in Fig. 1.34(b). The output resistance of the circuit is zero. The input impedance is given by

$$Z_{\text{in}} = R + \frac{1}{Cs} = R \times \frac{1 + RCs}{RCs} \tag{1.76}$$

This is of the form of a constant multiplied by the reciprocal of a high-pass transfer function.

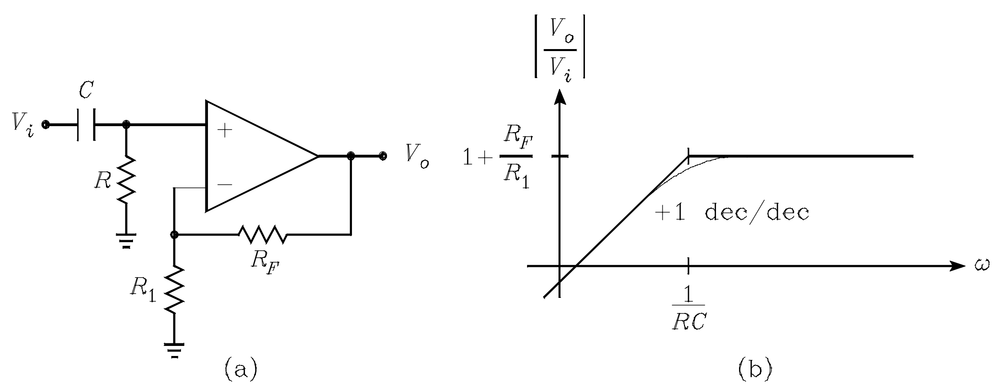

Figure 1.34: (a) Non-inverting high-pass amplifier. (b) Bode plot for $|V_o/V_i|$.

Example 22 *Design a non-inverting high-pass amplifier which has a gain of* 15 *and a lower cutoff frequency of* 20 *Hz. The input resistance is to be* 10 *k*Ω *in the passband.*

Solution. The circuit diagram is shown in Fig. 1.34(a). In the passband, C is a short circuit. To meet the input resistance specification, we must have $R = 10$ kΩ. The voltage-gain transfer function is given by Eq. (1.75). For a lower half-power cutoff frequency of 20 Hz, we must have $RC = 1/(2\pi 20)$. Solution for C yields, $C = 0.796$ μF. For the gain specification, we must have $1 + R_F/R_1 = 15$ or $R_1 = R_F/14$. If $R_F = 56$ kΩ, it follows that $R_1 = 4$ kΩ.

1.9.3 The Non-Inverting High-pass Shelving Amplifier

A *non-inverting high-pass shelving amplifier* is shown in Fig. 1.35(a). The voltage gain is given by Eq. (1.10) with R_1 replaced by $R_1 + 1/C_1 s$. It follows that the gain can be written

$$\frac{V_o}{V_i} = 1 + \frac{R_F}{R_1 + (1/C_1 s)} = \frac{1 + (R_F + R_1)\, C_1 s}{1 + R_1 C_1 s} \tag{1.77}$$

This is of the form of a high-pass shelving transfer function having a pole time constant $R_1 C_1$ and a zero time constant $(R_F + R_1)\, C_1$. The Bode plot for $|V_o/V_i|$ is shown in Fig. 1.35(b). It can be seen from the figure that the gain at low frequencies is unity. At high frequencies, the gain shelves at $1 + R_F/R_1$.

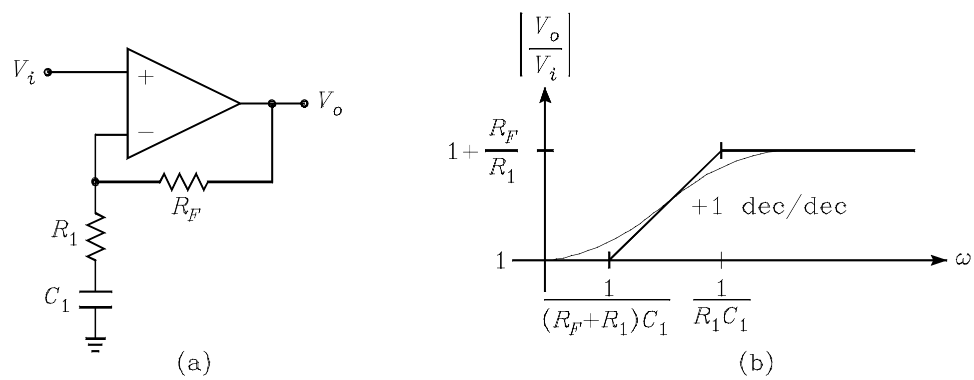

Figure 1.35: (a) Non-inverting high-pass shelving amplifier. (b) Bode plot for $|V_o/V_i|$.

Example 23 *Design a high-pass shelving amplifier which has unity gain at low frequencies, a pole in its transfer function with a time constant of* 75 *μsec, and a zero with a time constant of* 7.5 *μsec. What are the pole and zero frequencies and what is the gain at high frequencies?*

Solution. The circuit diagram is shown in Fig. 1.35(a). The voltage gain is given by Eq. (1.77). For the pole and zero time constant specifications, we must have $R_1 C_1 = 7.5$ μsec and $(R_1 + R_F)\, C_1 = 75$ μsec. Because there are three circuit elements and only two equations, we must specify one element in order to calculate the other two. Let $C_1 = 0.001$ μF. It follows that $R_1 = 7.5$ kΩ and $R_2 = 75$ kΩ $- R_1 = 67.5$ kΩ. The frequency of the zero is $f_z = 1/\left(2\pi 75 \times 10^{-6}\right) = 2.12$ kHz. The frequency of the pole is $f_p = 1/\left(2\pi 7.5 \times 10^{-6}\right) =$ 21.2 kHz. The gain at high frequencies is given by $1 + R_F/R_1 = 1 + 67.5/7.5 = 10$.

1.10 Op-Amp Comparators

1.10.1 The Inverting Comparator

A *comparator* is a circuit which has two inputs and one output. The output voltage exhibits two stable states which depend on the relative value of one input voltage compared to the other input voltage. The op amp is often used as a comparator. Fig. 1.36(a) shows the circuit diagram of an op amp used as an *inverting comparator*. The voltage applied to the non-inverting input is the dc reference voltage V_{REF}. The output voltage is given by

$$v_O = A\left(V_{\mathrm{REF}} - v_I\right) \tag{1.78}$$

where A is the op-amp gain. For an ideal op amp, we assume that $A \to \infty$. This implies that $v_O \to \infty$ for $v_I < V_{\mathrm{REF}}$ and $v_O \to -\infty$ for $v_I > V_{\mathrm{REF}}$. However, a physical op amp cannot have an infinite output voltage. Let us denote the maximum value of the magnitude of the output voltage by V_{SAT}. We call V_{SAT} the *saturation voltage*.

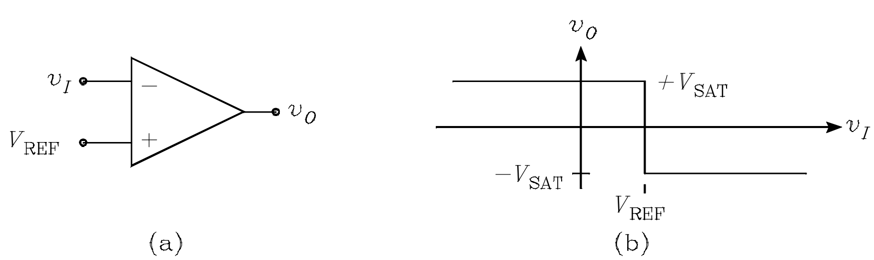

Figure 1.36: (a) Inverting comparator. (b) Plot of v_O versus v_I.

For an ideal op amp that exhibits saturation of its output voltage, the output voltage of the inverting comparator circuit in Fig. 1.36(a) can be written

$$v_O = V_{\mathrm{SAT}}\,\mathrm{sgn}\left(V_{\mathrm{REF}} - v_I\right) \tag{1.79}$$

where $\mathrm{sgn}\,(x)$ is the *signum function* defined by $\mathrm{sgn}\,(x) = +1$ for $x > 0$ and $\mathrm{sgn}\,(x) = -1$ for $x < 0$. The plot of v_O versus v_I for the circuit is given in Fig. 1.36(b).

1.10.2 The Non-Inverting Comparator

Figure 1.37(a) shows the circuit diagram of an op amp used as a *non-inverting comparator*. The output voltage is given by

$$v_O = V_{\mathrm{SAT}}\,\mathrm{sgn}\left(v_I - V_{\mathrm{REF}}\right) \tag{1.80}$$

The graph of v_O versus v_I is given in Fig. 1.37(b).

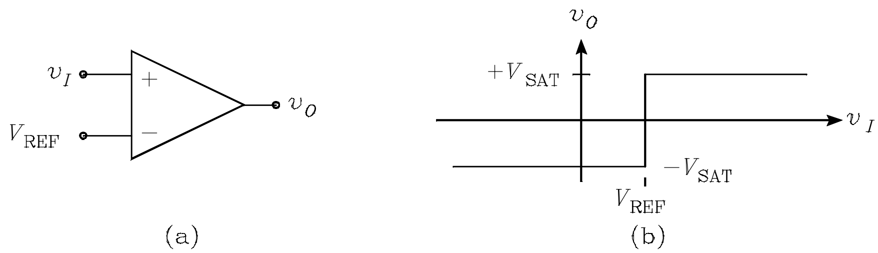

Figure 1.37: (a) Non-inverting comparator. (b) Plot of v_O versus v_I.

1.10.3 The Comparator with Positive Feedback

Positive feedback is often used with comparator circuits. The feedback is applied from the output to the non-inverting input of the op amp. Fig. 1.38(a) shows the circuit diagram of an inverting op-amp comparator with positive feedback. The circuit is also called a *Schmitt trigger*. The capacitor C_F in the figure is assumed to be an open circuit in the following. This capacitor is often used to improve the switching speed of the comparator by increasing the amount of positive feedback at high frequencies. It has no effect on the input voltage at which the op amp switches states.

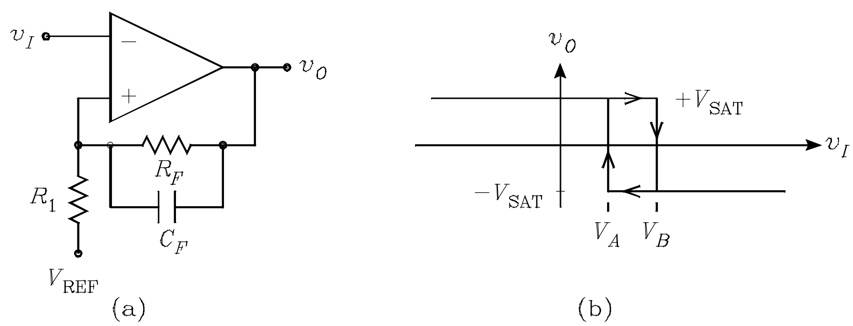

Figure 1.38: (a) Schmitt trigger. (b) Plot of v_O versus v_I.

The output voltage from the circuit of Fig. 1.38(a) can be written

$$v_O = V_{SAT}\,\mathrm{sgn}\,(v_+ - v_I) \tag{1.81}$$

Because v_O has the two stable states $v_O = +V_{SAT}$ and $v_O = -V_{SAT}$, it follows that v_+ can have two stable states given by

$$V_A = V_{REF}\frac{R_F}{R_F + R_1} - V_{SAT}\frac{R_1}{R_F + R_1} \tag{1.82}$$

$$V_B = V_{\text{REF}} \frac{R_F}{R_F + R_1} + V_{\text{SAT}} \frac{R_1}{R_F + R_1} \tag{1.83}$$

where superposition and voltage division have been used for each equation. For $v_I < V_A$, it follows that $v_O = +V_{\text{SAT}}$. For $v_I > V_B$, it follows that $v_O = -V_{\text{SAT}}$. For $V_A < v_I < V_B$, v_O can have two stable states, i.e. $v_O = \pm V_{\text{SAT}}$. The graph of v_O versus v_I is shown in Fig. 1.38(b).

The value of v_O for $V_A < v_I < V_B$ depends on whether v_I increases from a value less than V_A or v_I decreases from a value greater than V_B. That is, the circuit has memory. If $v_I < V_A$ initially and v_I begins to increase, v_O remains at the $+V_{\text{SAT}}$ state until v_I becomes greater than V_B. At this point v_O switches to the $-V_{\text{SAT}}$ state. If $v_I > V_B$ initially and v_I begins to decrease, v_O remains at the $-V_{\text{SAT}}$ state until v_I becomes less than V_A. Then v_O switches to the $+V_{\text{SAT}}$ state. The path for v_O on the graph in Fig. 1.38(b) is indicated with arrows. The loop in the graph is commonly called a *hysteresis loop.*

Example 24 *The Schmitt trigger circuit of Fig. 1.38(a) has the element values $R_F = 1$ MΩ and $R_1 = 33$ kΩ. If $V_- = 3$ V and the op amp saturation voltage is $V_{SAT} = 12$ V, calculate the two threshold voltages V_A and V_B.*

Solution. By Eqs. (1.82) and (1.83), we have

$$V_A = 3 \times \frac{1}{1 + 0.033} - 12 \times \frac{0.033}{1 + 0.033} = 2.52 \text{ V}$$

$$V_B = 3 \times \frac{1}{1 + 0.033} + 12 \times \frac{0.033}{1 + 0.033} = 3.29 \text{ V}$$