A Four-Stage FM Broadcast Audio Peak Limiter

W. Marshall Leach, Jr., *Senior Member, IEEE*
Georgia Insititute of Technology, Atlanta, GA 30332–0250, USA

***Abstract*—The design of a peak limiter processor for FM broadcast audio is described. The limiter has four gain control stages. The basic peak limiting function is performed in the first and second stages by a slow-attack slow-release stage followed by a fast-attack fast-release stage. Pre-emphasis control is performed in the third and fourth stages which are part of a filter that emulates the transmitter pre-emphasis network. A peak clipper at the output of the pre-emphasis controller provides protection from overmodulation by short duration peaks that are not controlled by the four limiter stages.**

I. Introduction

THE AVERAGE loudness levels of FM broadcast signals have increased dramatically over the years as more sophisticated electronic signal processors have become available to broadcasters who compete for the same listeners. These processors include compressors, limiters, peak clippers, phase scramblers, etc. Many processors are multi-band units which process the audio signal by filtering it into two to as many as six frequency bands, processing the signal in each band, combining the processed multi-band signals, and then peak processing the combined signal. The effect of such processing is to generate a signal which peaks consistently at the 100% modulation level and sounds loud and dense to the listener. In some markets, the processing is so intense that an oscilloscope used to observe demodulated air signals reveal their frequent resemblance to low-pass filtered square waves.

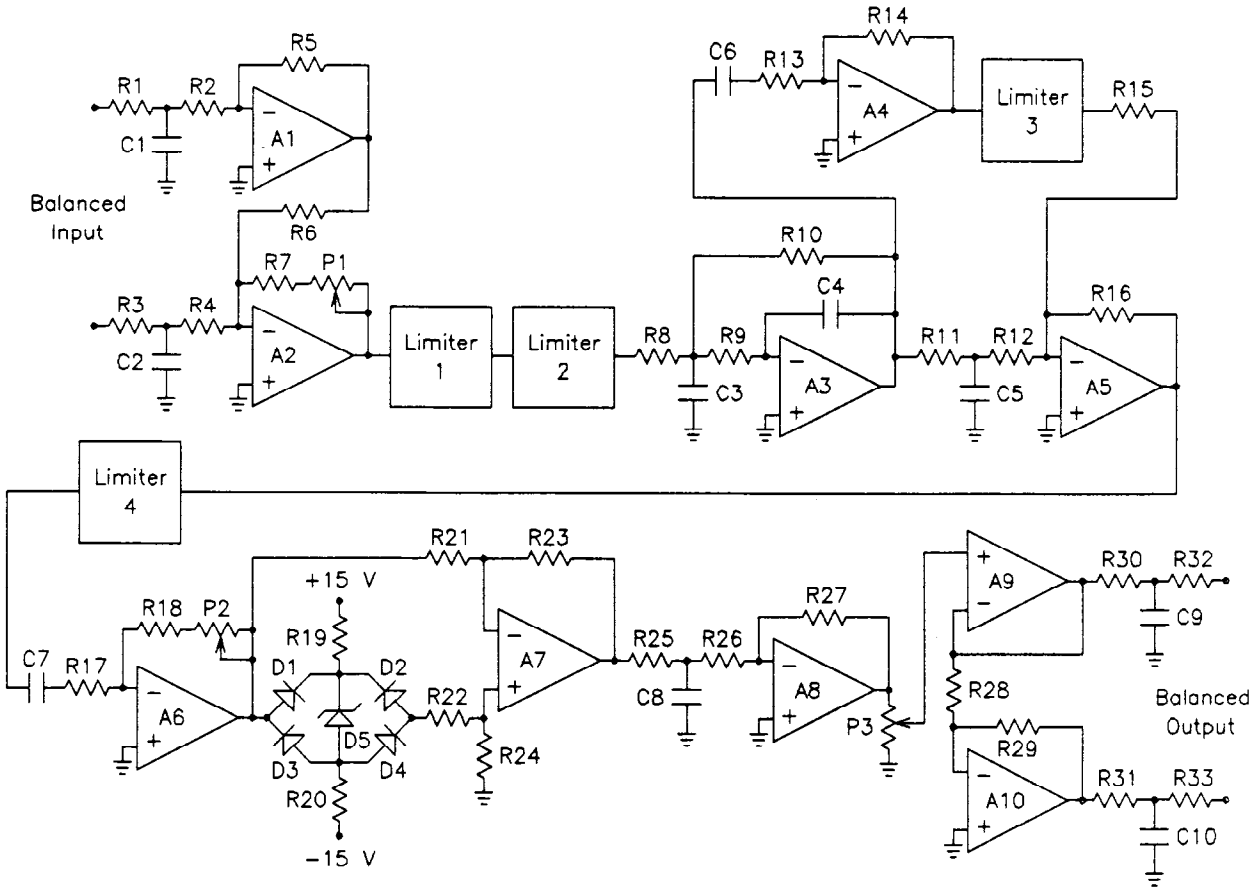

Fig. 1. Circuit diagram of the processor with the four limiter stages represented by block diagrams.

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II. Description of the Processor

A system level description of the overall processor is given in this section. The pre-emphasis controller and the peak limiter circuit are described in more detail in following sections.

Fig. 1 shows the circuit diagram of the processor with the four limiter stages represented by block diagrams. The input stage consists of op-amps A_1 and A_2 which realize a variable-gain balanced input stage. It is followed by two peak limiter stages in cascade which perform the basic peak limiting function. Limiter 1 is a slow-attack slow-release unit which performs the major gain control. Because of its slow attack time, its output contains significant overshoots. These are controlled by limiter 2 which has a fast-attack fast-release time. The limiting on low-frequency signals is performed primarily by the first stage. Its slow release time provides low distortion at low frequencies. Transient high-frequency peaks are limited primarily by the second stage. Its fast release time prevents audible "gaps" in the signal after gain reduction on fast peaks. Each limiter has a limit threshold of 1 V and an inverting gain below threshold of unity.

The Federal Communications Commission (FCC) specifies that the audio input signal to FM transmitters and TV aural transmitters be boosted at high frequencies by a pre-emphasis network that has a voltage-gain transfer function of the form

$$F(s) = 1 + \tau_1 s \qquad (1)$$

where $s = j2\pi f$ is the complex frequency and $\tau_1 = 75$ μsec. The gain of the pre-emphasis network is specified to follow this transfer function for frequencies up to 15 kHz. At low frequencies, the gain of the network is unity (0 dB). At 2.12 kHz, the gain is 1.41 (3 dB). At 15 kHz, the gain increases to 7.14 (17.1 dB). Because of the frequency dependent gain in the pre-emphasis network, a peak-limited signal is no longer peak limited after it is pre-emphasized. Therefore, it is necessary to process the signal in a way which prevents overmodulation after the signal input to the transmitter is pre-emphasized.

Pre-emphasis control in the processor is performed by limiters 3 and 4 which are part of a circuit that emulates the voltage-gain transfer function of the transmitter pre-emphasis network. Each limiter has a limit threshold of 1 V and an inverting gain below threshold of unity. The signal input to limiter 3 is the signal output of limiter 2 multiplied by the $\tau_1 s$ in the transfer function of Eq. (1). The $\tau_1 s$ voltage-gain transfer function is realized by A_3 and A_4. The output of limiter 3 and the output of limiter 2 multiplied by the 1 in Eq. (1) are added by A_5. This sum signal is limited by limiter 4. Limiter 4 is necessary because the output of A_5 can have peaks that are 3 dB above the 1 V limit threshold of the preceding limiters.

Although the output signal from limiter 4 has well defined peak levels, a peak clipper is used as a safety clipper to prevent transient overshoots from exceeding the 1 V limit threshold. The peak clipper function is realized by diodes D_1 through D_5 and A_7. Because the output signal from the clipper is pre-emphasized, i.e. it is multiplied by F(s) of Eq. (1), a de-emphasis network having a voltage-gain transfer function equal to the reciprocal of F(s) must be used to restore the original frequency balance to the signal. This is accomplished by resistors R_{25} and R_{26} and capacitor C_8. A_9 and A_{10} form a balanced line driver output stage.

III. The Pre–Emphasis Controller

This section describes the design of the pre-emphasis controller circuits. The first stage of pre-emphasis control is provided by A_3 through A_5 and limiter 3. A block diagram which models the function of this circuit is given in Fig. 2. The voltage at the input is applied to a second-order low-pass filter. The voltage at the output of the filter drives two parallel paths.

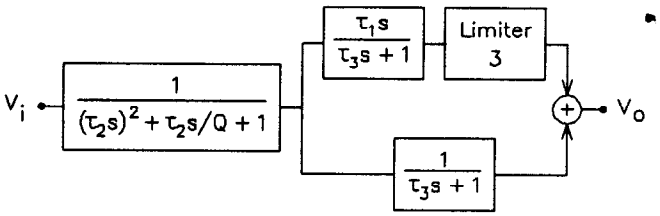

Fig. 2. Block diagram representation of the pre–emphasis controller filters.

One path consists of a high-pass filter with gain followed by limiter 3. The second path consists of a low-pass filter. The outputs from the two parallel paths are summed to form the output voltage. The overall voltage-gain transfer function of the circuit is given by

$$\frac{V_o}{V_i} = \frac{1}{(\tau_2 s)^2 + \tau_2 s/Q + 1} \times \left[\frac{1}{\tau_3 s + 1} + \frac{\tau_1 s}{\tau_3 s + 1} \times k_3 \right] \qquad (2)$$

where $\tau_1 = 75$ μs, $\tau_2 = 8.92$ μs, $\tau_3 = 13.03$ μs, $Q = 1.46$, and k_3 is the absolute value of the voltage gain of limiter 3 ($0 \le k_3 \le 1$). The transfer function is of the form $(1 + k_3\tau_1 s)$ multiplied by the transfer function of a 3rd-order 0.2 dB ripple Chebyshev low-pass filter having a cutoff frequency of 15 kHz.

Fig. 3 illustrates the frequency responses of the circuits diagramed in Fig. 2. The gain of limiter 3 is taken to be unity for the figure. Curve a gives the frequency response from the input through the lower path in Fig. 2 to the output. Curve b gives the frequency response from the input through the upper path to the output. Curve c gives the frequency response from the input to the output for the two paths simultaneously. The vertical line in the figure is at 15 kHz. Curve c follows the Bode plot for the pre-emphasis transfer function of Eq. (1) within 0.2 dB from 0 to 15 kHz.

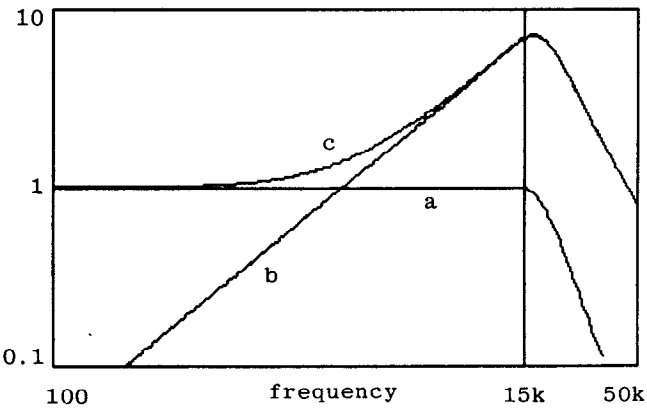

Fig. 3. Calculated gain versus frequency of the pre–emphasis controller filters. Both axes use log scales.

For signal frequencies below 15 kHz, the 3rd-order Chebyshev transfer function has essentially unity gain so that the effective overall transfer function of the circuit diagramed in Fig. 2 can be considered to be $(1 + k_3\tau_1 s)$. If $k_3 = 1$, this is the pre-emphasis transfer function of Eq. (1). If gain reduction in limiter 3 occurs on high-frequency signals, the effect is to momentarily reduce the pre-emphasis time constant so that the peak output voltage of limiter 3 cannot exceed 1 V. Thus the two input voltages to the summer in Fig. 2 are each peak limited to 1 V. Because the two signals differ in phase by 90°, the

output of the summer can have peak levels 3 dB above the 1 V limit threshold of the preceding limiters. This follows because 1 + j1 has a magnitude equal to the square root of 2 or +3 dB on a decibel scale. The purpose of limiter 4 is to limit the output of the summer to a peak level of 1 V.

An important consideration in the design of the circuit diagramed in Fig. 2 is that the two parallel paths preceding the summer have equal phase delays. If the delays are not the same, a delay equalizer would be required in one path in order for the signals to add with the correct 90° phase difference in the summer. Otherwise, the frequency response of the circuit would not be correct. To achieve equal delays, a pole in one path must be duplicated in the other path. This is achieved by factoring the first-order pole term $(1 + \tau_3 s)$ from the 3rd-order Chebyshev low-pass transfer function and realizing this pole in each path. In the upper path of Fig. 2, the pole is realized as part of a high-pass filter having the gain $\tau_1/\tau_3 = 5.76$ (15.2 dB). In the lower path, the pole is realized as part of a low-pass filter. It follows that the signal inputs to the summer in the figure differ in phase by precisely 90° at all frequencies. The pole frequency for the $(1 + \tau_3 s)$ term is 12.2 kHz.

Because the output of limiter 4 can contain transient peak overshoots above the 1 V limit threshold, a peak clipper is used to prevent these from exceeding 1 V. The peak clipper is realized in Fig. 1 by A_6 and A_7 and D_1 through D_5. A_6 is a gain stage that drives both a center clipper consisting of diodes D_1 through D_4 and the inverting input of a differential amplifier realized by A_7. The threshold of the center clipper is set by the voltage across zener diode D_5. The output from the center clipper drives the non-inverting input of the differential amplifier. The differential amplifier subtracts the two signals, thus realizing a peak clipper function. To obtain a hard clipper characteristic, the non-inverting gain of the differential amplifier is approximately 5% higher than the inverting gain.

Under conditions of no gain reduction in limiter 3, the signal output of A_7 is pre-emphasized according to the transfer function of Eq. (1). To restore the frequency balance to the signal, it must be low-pass filtered by a circuit with the voltage-gain transfer function given by the reciprocal of Eq. (1). This is realized by R_{25}, R_{26}, and C_8. The filter also removes transient distortion produced by the safety clipper. A_8 drives P_3 which sets the input level to the balanced line driver realized by A_9 and A_{10}.

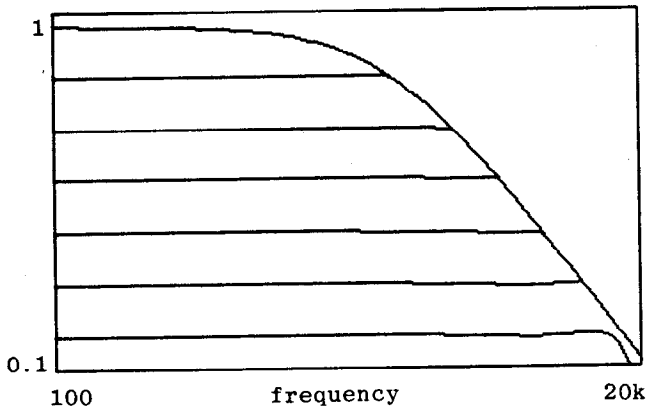

Fig. 4. Calculated gain versus frequency of the overall pre-emphasis controller circuit for seven different input levels. Both axes use log scales.

Fig. 4 illustrates the frequency responses of the pre-emphasis controller for seven different input signal levels. The upper curve is calculated for a 1 V peak input signal. This curve corresponds to the Bode plot for the reciprocal of the pre-emphasis transfer function of Eq. (1). The lower curve is calculated for a 0.125 V peak input signal. Because limiters 3 and 4 do not limit at this signal level, the lower curve corresponds to the Bode plot of the third-order Chebyshev low-pass filter. The frequency responses illustrated in Fig. 4 are calculated for a continuous sine-wave input signal. For an audio signal input, the bandwidth of the circuit varies dynamically with the signal in such a way that the signal is peak limited when pre-emphasized.

IV. The Peak Limiter Circuit

This section describes the design of the four limiter circuits used in the processor. Fig. 5 gives the basic circuit diagram of the limiters. The gain control element is a p-channel JFET operated in the triode region as a variable resistor. Although a voltage controlled amplifier (VCA) or an analog multiplier are also used in such applications, the JFET was selected because of the simplicity of the circuit. R_1 through R_3 give A_1

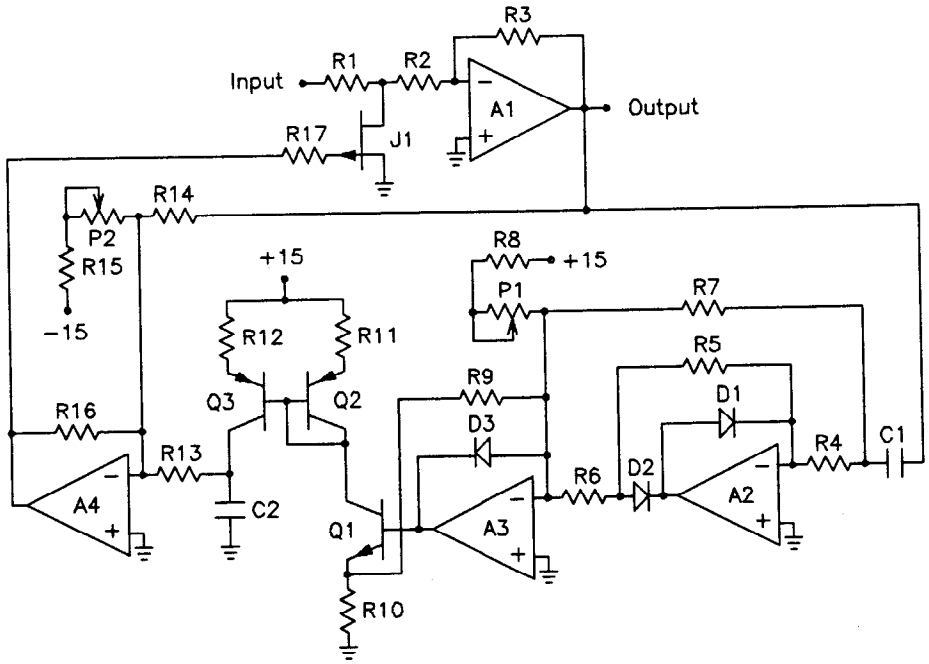

Fig. 5. Circuit diagram of the four limiter circuits.

an inverting gain of 1.06 (0.5 dB) with JFET J_1 omitted. Potentiometer P_2 adjusts the DC gate voltage on J_1 so that the quiescent gain of A_1 is unity. This biases J_1 just into the triode region. The signal output of A_1 is detected by A_2 and A_3 and BJT's Q_1 through Q_3 which form a full-wave rectifier voltage-to-current converter with threshold. P_1 sets the threshold voltage of the detector to 1 V. If the absolute value of the peak output voltage of A_1 exceeds 1 V, A_3 forces Q_1 to conduct. The collector current in Q_1 is mirrored into the collector of Q_3 by the current mirror formed by Q_2 and Q_3. The current output of Q_3 charges C_2 causing the output voltage of A_4 to decrease from the quiescent level set by P_2. This causes the drain-to-source resistance of J_1 to decrease, thus decreasing the gain of the circuit.

The JFET is not a linear resistor in its triode region unless one-half the drain-to-source voltage is fed back into the gate. This is accomplished by the addition of R_{14}. The condition for linearization of the JFET is $R_3R_{16}/R_2R_{14} = 1/2$. In case the required value for R_{14} exceeds available value resistors, a three-resistor T-network can be used in place of R_{14}.

With P_2 adjusted as described and $R_{16} = R_{13}$, the small-signal gain of A_1 as a function of the control voltage V_C on C_2 is given by

$$\frac{v_o}{v_i} = \frac{-1}{1 + V_C/V_A} \tag{3}$$

where $V_A = V_P^2R_3/2R_1R_2I_{DSS}$. In this equation, I_{DSS} is the JFET drain-to-source saturation current and V_P is the pinch-off voltage (V_P is a negative number). It is assumed that the absolute value of the drain-to-source voltage is less than about $|V_P|/10$ so that the JFET is in its triode region. The condition that the absolute value of the drain-to-source voltage equal $|V_P|/10c$ is $R_2 = R_3|V_P|/10cV_T$, where c is a constant and V_T is the limiter threshold voltage. In the realization of the four limiters, R_2 and R_3 were chosen to satisfy this condition with $c = 5.8$ and $V_T = 1$ V. This allows transient overshoots of 15.3 dB above the detector threshold before the absolute value of the drain-to-source voltage reaches $|V_P|/10$.

Eq. (3) can be used to calculate the ratio of the maximum to the minimum gain for A_1. Maximum gain occurs when $V_C = 0$ and minimum gain occurs when $V_C = |V_P|$. It follows that the ratio of the maximum to the minimum gain for A_1 is given by $1 + 2I_{DSS}R_1R_2/|V_P|R_3$. In the realization of the four limiters, this was taken to be 20 (26 dB).

In order to calculate the attack time constant of the limiter, Eq. (3) must be approximated by an equation that is linear in V_C. This is taken to be

$$\frac{v_o}{v_i} \simeq -(k - V_C/V_B) \tag{4}$$

Fig. 6 shows the actual attenuator gain and two approximations. Curve a gives the actual gain calculated from Eq. (3) with $V_A = 0.153$ V. Curve b gives the approximate gain calculated from Eq. (4) with $k = 1$ and $V_B = 2V_A = 0.307$ V. Curve c gives the approximate gain calculated from Eq. (4) with $k = 0.625$ and $V_B = 8V_A = 1.226$ V. Curve b approximates curve a for a gain in the range of 1 to 0.5 (0 to 6 dB of gain reduction) and curve c approximates curve a for a gain in the range of 0.5 to 0.25 (6 dB to 12 dB of gain reduction).

C_1 in Fig. 5 is a DC blocking capacitor which can be replaced by a short circuit for purposes of defining the attack time constant of the circuit. It is assumed that the input voltage is initially at zero, that the initial voltage on C_2 is zero, and that curve b in Fig. 6 can be used to model the gain. For an input voltage step having an absolute value of V_1, where V_1 is greater than the detector threshold voltage of 1 V, the differential equation for the control voltage on C_2 is

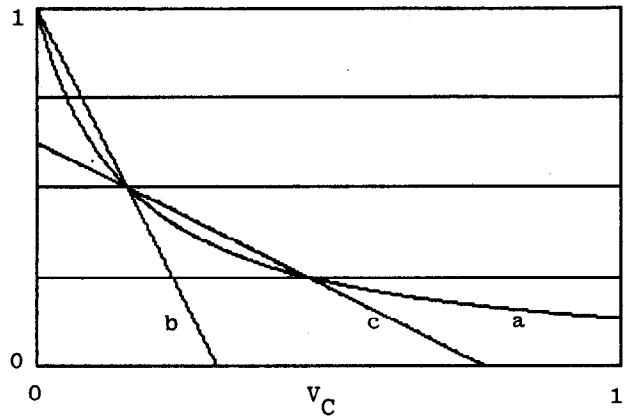

Fig. 6. Calculated gain of the JFET attenuator as a function of control voltage and two straight–line approximations to the curve.

$$\frac{dV_C}{dt} + \frac{1}{\tau_a}V_C = \frac{V_1 - 1}{R_9\|R_{10}C_2} \tag{5}$$

In this equation, τ_a is the attack time constant of the circuit which is given by

$$\tau_a = \frac{R_{13}C_2}{1 + (R_{13}/R_9\|R_{10})(V_1/V_B)} \tag{6}$$

This equation shows that the attack time constant decreases as V_1 increases. This is a desirable characteristic for a limiter. For purposes of calculations in the design phase, V_1 was taken to be 2 V, i.e. twice the detector threshold voltage. This value causes the gain reduction to be 6 dB so that curve b in Fig. 6 represents an acceptable approximation. If the input voltage drops from V_1 to some value less than 1 V, the detector cuts off and the release time constant is given by

$$\tau_r = R_{13}C_2 \tag{7}$$

The transient response of the limiter is illustrated in the SPICE simulation of the circuit given in Fig. 7. The attack time constant for the circuit simulated was $\tau_a = 0.1$ ms. Curve a shows the input signal which is a 1 kHz sine wave with a peak amplitude of 2 V. Curve b shows the limiter output signal which overshoots the limiter threshold of 1 V by about 40% on the first half cycle. By the fourth half cycle, the peak output voltage has been reduced to approximately 1 V. Curve c shows the voltage at the emitter of Q_1 multiplied by 2. The current which charges C_2 is proportional to this voltage. Curve d shows the gain control voltage on C_2 multiplied by 5. This voltage increases only during the intervals that Q_1 conducts.

The JFET type used in the realization of the four limiters is the 2N5462. The units used were approximately matched and had the average parameters $I_{DSS} = 6.2$ mA and $V_P = -2.9$ V. The attack and release time constants used for the four limiters are as follows: limiter 1 – $\tau_a = 0.5$ ms and $\tau_r = 0.51$ s, limiter 2 – $\tau_a = 10$ μs and $\tau_r = 51$ ms, and limiters 3 and 4 – $\tau_a = 2$ μs and $\tau_r = 16$ ms.

Not shown in Fig. 5 are the circuits which drive the front panel meters that indicate the amount of limiting in each channel of the processor. To derive a meter drive signal, the Q_2–Q_3 current mirror is modified by the addition of a third PNP BJT. The current in Q_2 is mirrored into the added transistor. The collectors of the four added BJT's in each channel are connected in parallel to the inverting input of an op–amp used as a current-to-voltage converter with an integrating capacitor

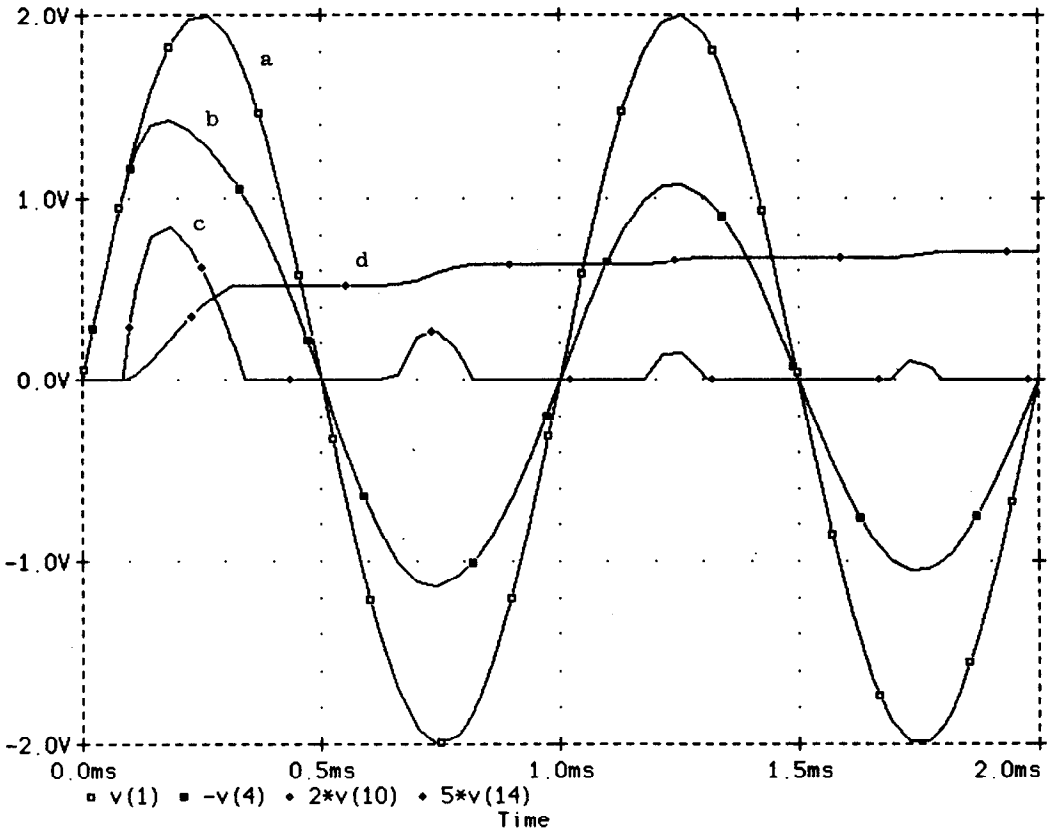

Fig. 7. SPICE simulations illustrating the transient attack of the limiter with a sine wave input signal.

in parallel with the feedback resistor. Separate current-to-voltage converters are used to drive the two front panel meters. Each meter reading is a weighted average of the total gain reduction in that channel.

V. Conclusions

Both the system design and the circuit design details of a peak-limiter processor for FM broadcasting have been presented. Although limiters which perform similar functions are currently used in broadcasting, it is difficult or impossible to find design details published in the technical literature. This paper documents some of these details. The design of the pre-emphasis controller filter by factoring a third-order Chebyshev low-pass filter transfer function is believed to be original. The circuit described has the desired feature that the phase delays are equal in two parallel paths which are summed to form an output signal. The peak limiter circuit described is an extremely simple but very effective circuit which can be realized with a single quad op–amp.

The distortion produced by overmodulation of FM transmitters by sibilant sounds is discussed in [1] where the use of a peak clipper after the pre–emphasis network is recommended. An identical solution to the pre–emphasis problem is described in [2]. Because of the distortion produced by peak clipping, it is believed that a pre–emphasis controller such as the one described here is a much more elegant solution to this problem than a simple peak clipper.

References

[1] J. G. Lourens, "On the Sibilance Problem in FM Sound Transmission", *IEEE Trans. Broadcasting*, Vol. 37, No. 2, pp. 64–68, June 1991.

[2] R. F. Abt, "Automatic Audio Signal Processing", *RCA Engineer*, Vol. 13, No. 5, pp 63–66, Feb./Mar. 1968.

W. Marshall Leach, Jr., (S'63–M'64–M'72–SM'81) received the B.S. and M.S. degrees in electrical engineering from the University of South Carolina, Columbia, in 1962 and 1964, and a Ph.D. degree in electrical engineering from the Georgia Institute of Technology in 1972.

In 1964 he worked at the National Aeronautics and Space Administration in Hampton, VA. From 1965 to 1968 he served as an officer in the U.S. Air Force. Since 1972 he has been a faculty member at the Georgia Institute of Technology where he is presently professor of electrical engineering. Dr. Leach teaches courses in applied electromagnetics, electronic design, and electroacoustics. He is a fellow of the Audio Engineering Society.