An FET Audio Peak Limiter

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***Abstract*— A high-quality peak limiting amplifier is described which uses a p-channel field-effect transistor as the variable gain element.**

I. Introduction

Peak limiter and compressor amplifiers are basic audio signal processing tools that are found in recording studios, broadcast installations, public address systems, etc., where the automatic control of audio signal levels is desired. A peak limiter is a circuit which monitors the peak level of a signal. If the peak exceeds a preset limit threshold, the gain of the circuit is reduced so as to prevent the peak from exceeding the threshold. Some of the applications of peak limiters are to prevent over modulation of broadcast transmitters, to prevent distortion caused by overload of audio recorders, to prevent overdrive of analog-to-digital converters, and to protect loudspeakers in public address systems.

A compressor amplifier is similar to a limiter amplifier in that it reduces gain when the input signal exceeds a preset threshold. However, compressors are usually designed to have attack and release times that are slower than those of limiters so that a compressor cannot be used to reliably control the peak levels in a signal. The principle application of a compressor is to maintain the average level of an audio signal constant. In broadcast applications, a compressor and a limiter in combination are used to maintain consistently high modulation levels without over modulation. Indeed, most radio stations engage in "loudness wars" by multi-stage processing the signal so that it sounds louder than the competition. This is one of the principal reasons that broadcast audio quality is often so poor.

This paper describes the design of a high-quality, low-noise limiter which is virtually transparent in its operation. The circuit uses a field-effect transistor (FET) as a variable resistor in the shunt arm of a voltage variable attenuator. Feedback is used to linearize the square-law term in the FET characteristic for low distortion operation. The peak level of the limiter output is detected by a threshold detector which has a current output as opposed to the usual voltage output. This provides improved stability of the feedback detector control circuit with less peak overshoot of the output signal.

Some limiters and compressors use a feedforward detector for the gain reduction scheme. If the level of the input signal increases above a preset threshold, the gain is reduced. The problem with such circuits is that the detector does not know what the output signal is doing. It is like adjusting the temperature of the water in a shower without being in the shower where you can feel the water. Feedforward compressors and limiters have an irritating audible signature, especially if they are not adjusted correctly. They can invert the loudness of a signal. That is, louder sounds come out sounding less loud that quieter sounds. These very annoying effects can be commonly heard in the audio on many cable TV channels. The limiter described here does not exhibit any of these effects because it uses a feedback detector which monitors the level of the output signal.

Feedback detector limiters and compressors can be unstable if the gain of the detector circuit is made too high. This is often done to minimize the output overshoot when gain reduction occurs. The instability causes the gain reduction to overshoot or to exhibit a "motorboating" effect. The circuit described here does not exhibit these problems. This

is primarily because the circuit uses a detector with a current source output rather than a voltage source output. The current output from the detector charges a capacitor which acts as an integrator for the error signal. A feedback control system with an integrator characteristic exhibits very low steady-state error. Thus the level to which the output signal is limited does not increase as the input level increases.

I have seen some very complicated FET limiter circuit designs. In contrast, the one described here is very simple, requiring only a single quad op amp, one FET, and three BJTs. The simplicity of the circuit should not be interpreted as an indicator of any performance limitations. It is very effective in its operation and very clean sounding.

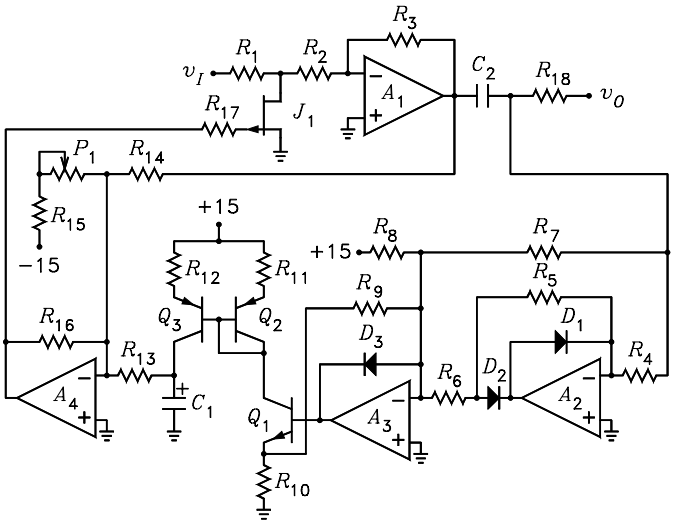

Fig. 1. Circuit diagram of the limiter.

II. Circuit Description

The circuit diagram of the limiter is shown in Fig. 1. FET J_1 is operated in its triode region as a variable resistor. Under conditions of no limiting, J_1 has a high resistance and op amp A_1 operates as a unity-gain inverting amplifier. The output voltage v_O is monitored by a full-wave detector circuit consisting of op amps A_2 and A_3 and transistor Q_1, which is normally cut off. The limit threshold is set by the current through resistor R_8. When the output voltage v_O exceeds the threshold voltage in either the positive or negative direction, A_3 drives the base of Q_1 positive so that collector current flows in Q_1. This current is mirrored into capacitor v_I by the current mirror consisting of transistors Q_2 and Q_3. This makes the voltage on C_1 to go positive, forcing the voltage output of op amp A_4 to decrease from its quiescent value. This causes the resistance of J_1 to decrease, thus decreasing the input signal to A_1 and causing v_O to be peak limited. Resistors R_{11} and R_{12} in the current mirror improve the current tracking between the two transistors. A typical value for these resistors is $100\,\Omega$.

After a peak is limited, C_1 discharges through R_{13} causing the resistance of J_1 to increase at a controlled rate until the gain of A_1 is again unity. With J_1 removed from the circuit, R_1 through R_3 are chosen to give A_1 a gain that is 1% to 5% larger than unity. Potentiometer P_1 is adjusted so that the resistance of J_1 is decreased just enough to give A_1 a quiescent gain of unity. This biases J_1 just into its active region so that it is not cut off quiescently. Otherwise, there could be a delay in the reaction time of the circuit when v_O exceeds the limit threshold.

Figure 2 illustrates the operation of the limiter. If the peak output voltage exceeds the threshold voltage V_L, the gain is reduced so as to limit the peak to the threshold level. The gain decrease or attack is indicated in the figure by the clockwise rotation of the $|v_O|$ versus $|v_I|$ curve. After a peak is limited, the gain recovers or releases at a relatively slow rate to the original level so that the curve rotates slowly back to its original slope.

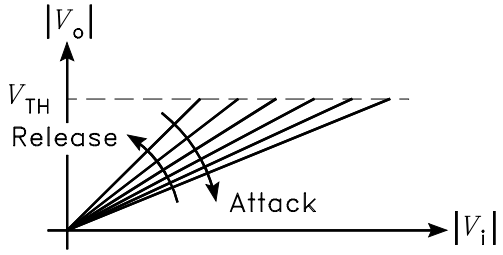

Fig. 2. Illustration of the operation of the limiter.

For minimum distortion, the FET drain-to-source voltage v_{DS} should not exceed about one-tenth of its pinch-off voltage. Maximum v_{DS} occurs when J_1 has a high resistance. The maximum fraction of the input voltage which appears on J_1 is set by the ratio of R_2 to R_1. The FET has a square law term in its characteristic that must be canceled for minimum distortion. This is achieved by feeding back one-half the drain-to-source voltage, i.e. $v_{DS}/2$, into the FET gate.

Let the FET pinch off voltage and drain-to-source

saturation current, respectively, be denoted by V_P and I_{DSS}. The design equations presented here assume that the limit threshold voltage is $V_L = 1\,\mathrm{V}$ peak, the maximum attenuation of the limiter is $20.8\,\mathrm{dB}$ (a factor of 11), and that the maximum drain-to-source voltage is $|V_P|/10$ for $|v_O| = 4$ (a $12\,\mathrm{dB}$ overshoot above the limit threshold). The equations do not apply if these specifications are changed. With these specifications, resistors R_1 through R_3 must satisfy

$$R_1 \| R_2 = \frac{9\,|V_P|}{2 I_{DSS}}$$

$$R_2 = \frac{|V_P|}{40 V_L} R_3 = \frac{|V_P|}{40} R_3$$

$$R_3 = k\,(R_1 + R_2)$$

where $k = 1.01$ to 1.05. Typical values for the 2N5464 p-channel JFET are $I_{DSS} = 6\,\mathrm{mA}$ and $|V_P| = 3\,\mathrm{V}$. With $k = 1.01$, the design equations give $R_1 = 33\,\mathrm{k\Omega}$, $R_2 = 2.7\,\mathrm{k\Omega}$, and $R_3 = 36\,\mathrm{k\Omega}$.

A maximum limiting of $20.8\,\mathrm{dB}$ might be considered to not be that great for a peak limiter. However, the amount of limiting in normal use would rarely exceed $6\,\mathrm{dB}$, which is small compared to $20.8\,\mathrm{dB}$. The circuit can be designed so that the maximum limiting is greater than $20.8\,\mathrm{dB}$. However, this would result in larger resistor values for R_1, R_2, and R_3. Because the thermal noise voltage generated by a resistor is proportional to the square root of the resistance, larger resistors could result in a decreased signal-to-noise ratio.

For $v_{DS}/2$ to be fed back into the FET gate, the following condition must be satisfied

$$\frac{R_3}{R_2} \times \frac{R_{16}}{R_{14}} = \frac{1}{2}$$

The circuit is designed with $R_{16} = R_{13}$ so that A_4 operates as a unity-gain inverter for the control voltage on C_1. The release time constant of the circuit is $\tau_r = R_{13} C_1$. For minimum distortion, this must not be too small. The value chosen for R_{13} is $75\,\mathrm{k\Omega}$. This is large enough so that C_1 does not have to be too large, because a large C_1 makes it difficult to obtain a small attack time constant. With this value, it follows that $R_{16} = 75\,\mathrm{k\Omega}$ and $R_{14} = 2\,\mathrm{M\Omega}$. R_{17} is in the circuit to limit the gate current in J_1 in the event that the gate-to-channel junction becomes forward biased. The channel is normally reverse biased so that the gate current is zero. A suitable value is $R_{17} = 1\,\mathrm{k\Omega}$.

The quiescent gate voltage on J_1 must be approximately equal to its pinch-off voltage, i.e. about $3\,\mathrm{V}$ for the 2N5464. R_{15} and P_1 set this voltage. With $R_{15} = 300\,\mathrm{k\Omega}$ and $P_1 = 200\,\mathrm{k\Omega}$, the quiescent gate voltage on J_1 can be adjusted in the range from $2.25\,\mathrm{V}$ to $3.75\,\mathrm{V}$.

A_2, A_3, and Q_1 operate as a full-wave rectifier with a current output. With R_8 omitted, the circuit is designed so that the voltage at the emitter of Q_1 is $|v_O|$, i.e. a full-wave rectified v_O, where C_2 is assumed to be an ac short. This condition can be met with $R_4 = R_5 = R_7 = R_9 = 20\,\mathrm{k\Omega}$ and $R_6 = 10\,\mathrm{k\Omega}$. The addition of R_8 causes A_2 to have a negative offset voltage at its output so that Q_1 is cut off quiescently. This causes the detector not to put out a current unless $|v_O|$ exceeds the limit threshold voltage given by

$$V_L = V^+ \frac{R_7}{R_8}$$

For $V_L = 1\,\mathrm{V}$, $V^+ = 15\,\mathrm{V}$, and $R_8 = 20\,\mathrm{k\Omega}$, this equation yields $R_8 = 300\,\mathrm{k\Omega}$. Although not a part of the rectifier, D_3 is necessary to prevent the output voltage from A_3 from ever going more negative than about $0.7\,\mathrm{V}$ when Q_1 is cut off. This protects Q_1 from reverse breakdown of its base-to-emitter junction.

For a peak input voltage that is twice the limiting threshold ($6\,\mathrm{dB}$ limiting) and a limiting threshold of $V_L = 1\,\mathrm{V}$, the value of $R_9 \| R_{10}$ required for an attack time constant τ_a of the circuit is approximately given by

$$R_9 \| R_{10} = \frac{2 R_{13} I_{DSS} V_L R_1 \| R_2}{V_P^2\,(\tau_r/\tau_a - 1)} = \frac{2 R_{13} I_{DSS} R_1 \| R_2}{V_P^2\,(\tau_r/\tau_a - 1)}$$

where $\tau_r = R_{13} C_1$ is the release time constant. A typical limiter might be designed for a release time constant of 0.5 seconds and an attack time constant of 0.1 millisecond. For the numerical values given above, this would require $C_2 = 6.8\,\mu\mathrm{F}$ and $R_{10} = 51\,\Omega$.

III. Practical Considerations

Capacitor C_2 is in the circuit to block any dc offset from the detector input, for a dc offset would cause asymmetrical limiting. A typical value for C_2 might be $10\,\mu\mathrm{F}$. It should be a non-polar capacitor. C_2 can

be eliminated if the offset voltage at the output of A_1 is very low. Alternately, an offset null potentiometer can be used with A_1.

The limiter input should be driven from a low output resistance source such as a unity-gain buffer or a gain stage. An input level control should not be connected between that stage and the limiter input because its output resistance would affect the limiter. A level control should either precede the input stage or be a part of the feedback network of that stage.

The input to the limiter must be ac coupled with a non-polar capacitor if there is any dc offset at the output of the input stage. A typical value for this capacitor might be $10\,\mu\mathrm{F}$. Alternately, an offset null potentiometer could be added to the input stage. Resistor R_{18} is in series with the output to isolate any load capacitance from A_1, e.g. the capacitance of a cable. A suitable value for R_{18} is $100\,\Omega$. This resistor can be omitted if the circuit drives another stage on the same circuit board.

The power supply voltages should be regulated, for changes in the supply voltages cause changes in the limiter threshold and in the quiescent bias on the FET gate. The recommended op amp for the circuit is a TL074. This is a quad op amp so that the limiter can be realized with a single integrated circuit. The TL074 is a low-noise bifet op amp that has a wide bandwidth and a high slew rate. In addition, it has very low input bias currents for minimum offset voltage problems. The diodes must be fast switching diodes. The 1N4148 is a good choice. General purpose rectifier diodes, such as the 1N4000 series, cannot be used because they do not switch fast enough at the higher audio frequencies. Recommended transistors are the 2N4401 for Q_1 and the 2N4403 for Q_2 and Q_3.

The circuit is designed for a p-channel FET. A n-channel device cannot be used because the polarity of the control voltage is not correct. Best performance is obtained with a FET that does not have too low a pinch-off voltage. The 2N5464 is recommended. The parameters V_P and I_{DSS} can be measured easily if they are not known. Put the FET on a solderless breadboard. Connect its gate to the circuit ground. Connect a $1\,\mathrm{k}\Omega$ potentiometer as a variable resistor between the FET source and the ground. Connect a mA meter in series with the FET drain to a negative dc voltage of $10\,\mathrm{V}$ or so. With the potentiometer set at zero resistance, the mA meter will read I_{DSS}. To determine V_P, adjust the potentiometer until the mA meter reads $I_{DSS}/4$. Without disturbing the potentiometer, measure the FET gate-to-source voltage. The pinch-off voltage is given by $V_P = 2V_{GS}$.

Many stereo limiters have the channels strapped together so that limiting in one channel also causes limiting in the other channel. Because of the fast attack and release characteristics of a limiter, this can cause audible intermodulation distortion effects between the channels. For this reason, strapping of the limiter circuit is not recommended. In contrast, the two channels of a stereo compressor should generally be strapped. The intermodulation distortion effects are minimized because of the slower time constants used in compressors.

Most limiters and compressors have a meter to indicate the amount of gain reduction. It is common to set these meters up so that the needle reads full scale with no gain reduction and deflects toward zero when the gain is reduced. The voltage output of A_4 can be used to drive a meter in this way. This voltage is quiescently positive and decreases toward zero when gain reduction occurs. The quiescent voltage at the output of A_4 is set by adjusting P_1 for unity gain below the limit threshold. This setting is a function of the characteristics of J_1. An adjustment must be provided to set the meter reading at full scale once P_1 is set. A potentiometer connected as a variable resistor in series with the meter can be used for this.

There is one potential problem in setting up a meter. The damping factor is a function of the source resistance it sees. As the source resistance increases, the damping factor decreases, causing the meter to overshoot and exhibit damped oscillations in its response. This can make it very difficult to obtain objective readings from a meter. A meter should see its optimum source resistance. Its value can be determined by alternately connecting and disconnecting a variable dc voltage in series with a variable resistor to the meter. When the resistor has the optimum value, the needle will swing from zero to its final position with about 10% overshoot. A smaller source resistance causes a sluggish response. A larger source resistance causes more overshoot. I have seen some meters which exhibit a large overshoot with a zero source resistance. These meters are worthless.

For proper response, a meter should see its optimum source resistance. Thus the ideal solution is to use an op amp stage to drive the meter with the optimum resistance connected in series between the two. The op amp must have a potentiometer gain control

so that the quiescent meter reading can be set to full scale after P_1 is set. A dc offset control can be added to the meter driver so that a zero meter reading can be calibrated to correspond to a particular gain reduction. For example, it might be set to correspond to $14\,\mathrm{dB}$, i.e. a factor of 5. The meter driver gain and offset must be set experimentally after P_1 is set. A disadvantage is that the setting of one affects the setting of the other.

In use, the input level to the limiter should be set so that it does not exhibit continuous limiting with an audio signal. Ideally, the purpose of a limiter is to prevent unanticipated peaks from overloading the system following the limiter. If it is set for frequent limiting of 3 to $4\,\mathrm{dB}$, the effective loudness of a signal can be enhanced with no audible side effects. If the limiter is driven too hard, the gain recovery during quiet passages can make low level background sounds too loud. Unfortunately, these effects are all too common in radio, TV, and cable broadcasting.

IV. Circuit Using an N-Channel JFET

It is possible to design the circuit using an n-channel JFET for the gain control element. The circuit is shown in Figure 3. The same design equations given above apply to this circuit. It is preferable to choose a JFET with a high drain-source saturation current I_{DSS}. That of the 2N5464 p-channel device is about $6\,\mathrm{mA}$. I have used a 2N5457 n-channel JFET in this circuit and found that it gave acceptable results. This device has an I_{DSS} about one-half of that of the 2N5457. I would prefer one with a larger value of I_{DSS} if available.

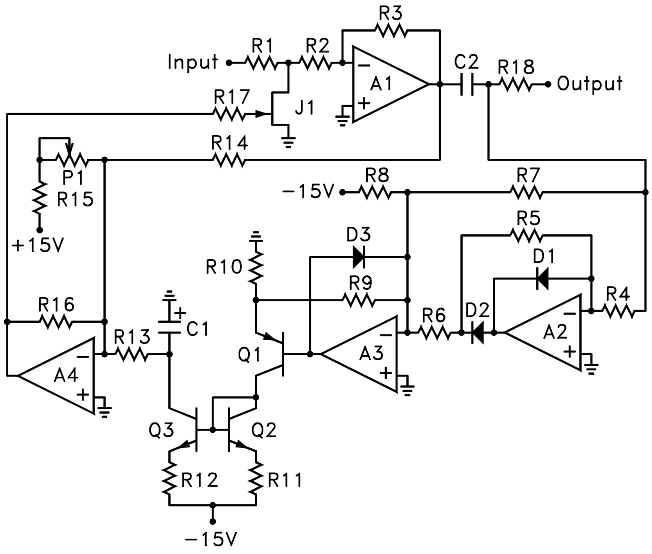

Fig. 3. Circuit with an n-channel JFET.