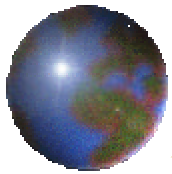
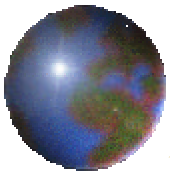


A Comparison of Five Different Multiprocessor SoC Bus Architectures

Kyeong Keol Ryu, Eung Shin and Vincent J. Mooney III
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, USA
{kkryu, eung, mooney}@ece.gatech.edu

Georgia Institute of Technology

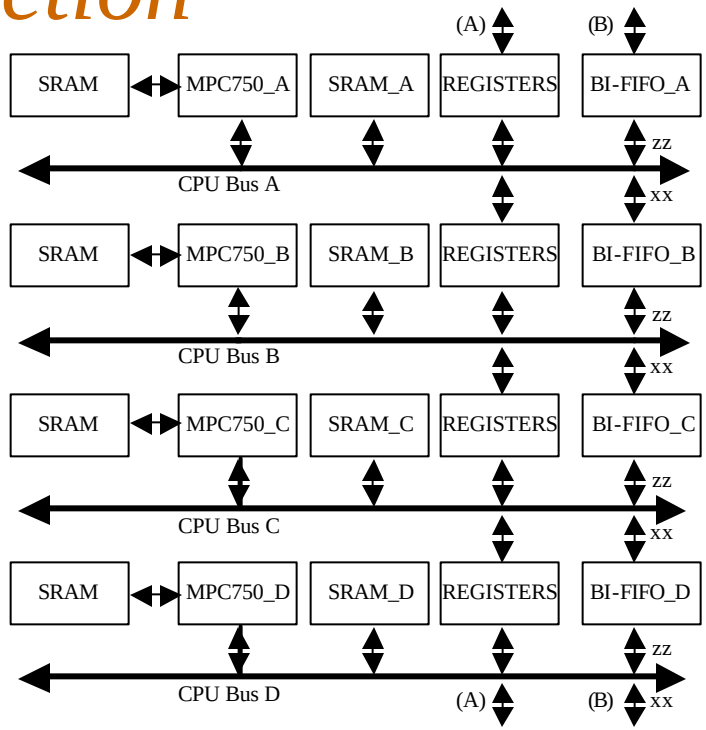


Outline

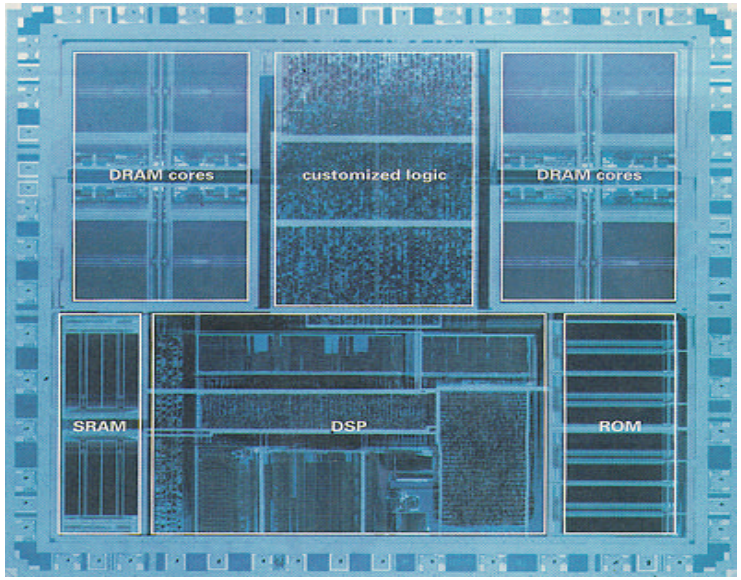
- Introduction
- Motivation and Previous Work
- Five Bus Architectures for SoC:
  - BFBA, GBIA, GBIIA, CSBA, and CCBA
- Application Examples:
  - OFDM transmitter and MPEG2 decoder
- Experiment Environment
- Comparison in View of Algorithm and Architecture
- Comparison of Throughput of the Bus Architectures
- Conclusion

Georgia Institute of Technology

Introduction



PCB

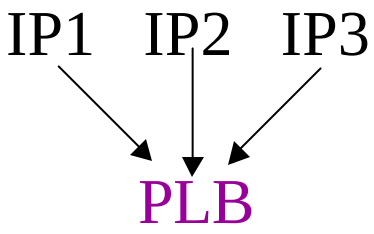


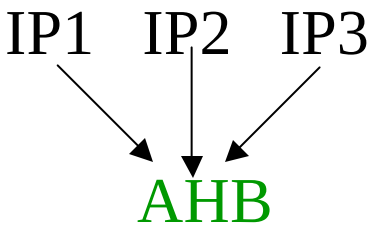
Motivation and Previous Work (I)

CoreConnect (IBM):
Processor Local Bus (PLB)
On-chip Peripheral Bus (OPB)

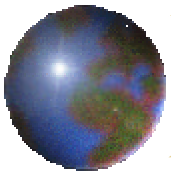
Intellectual Propery (IP)

AMBA (ARM):
Advanced High-performance Bus (AHB)
Advanced Peripheral Bus (APB)





Georgia Institute of Technology

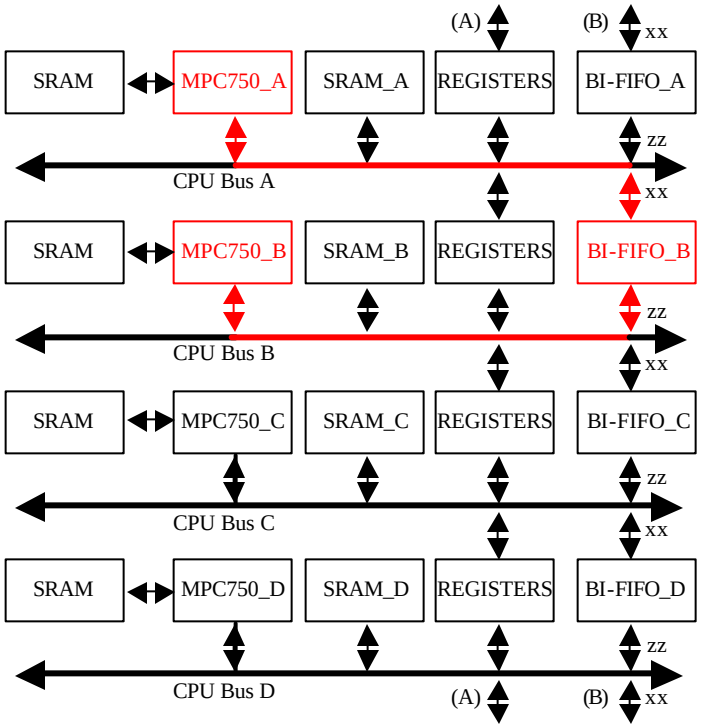


Motivation and Previous Work (II)

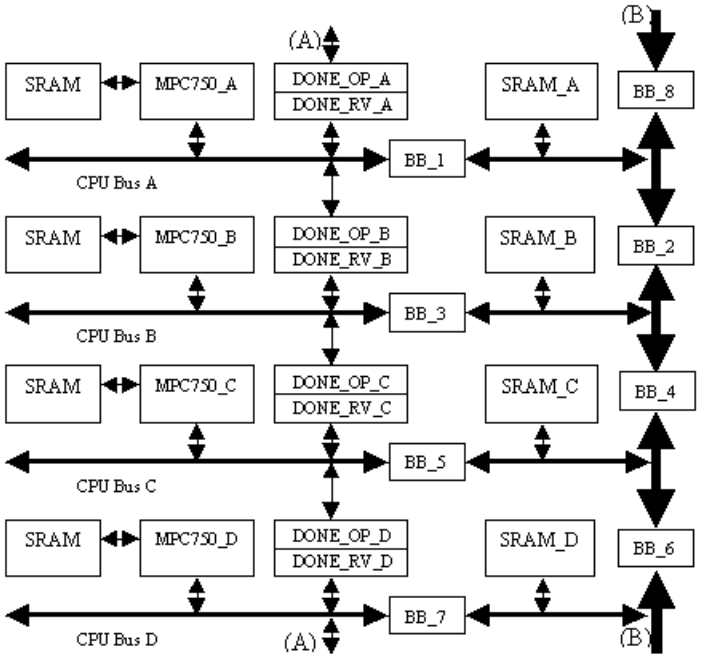
- Sonics uNetwork
  - TDMA arbitration
  - IP reuse and integration
- Whisbone architecture (Silicore)
  - one bus for all
  - supports multiple masters
- In terms of bus topology, uNetwork and Whisbone are similar to AMBA and CoreConnect

Five Bus Architectures for 4 processor System (I)

- Bi-FIFO Bus Architecture (BFBA)



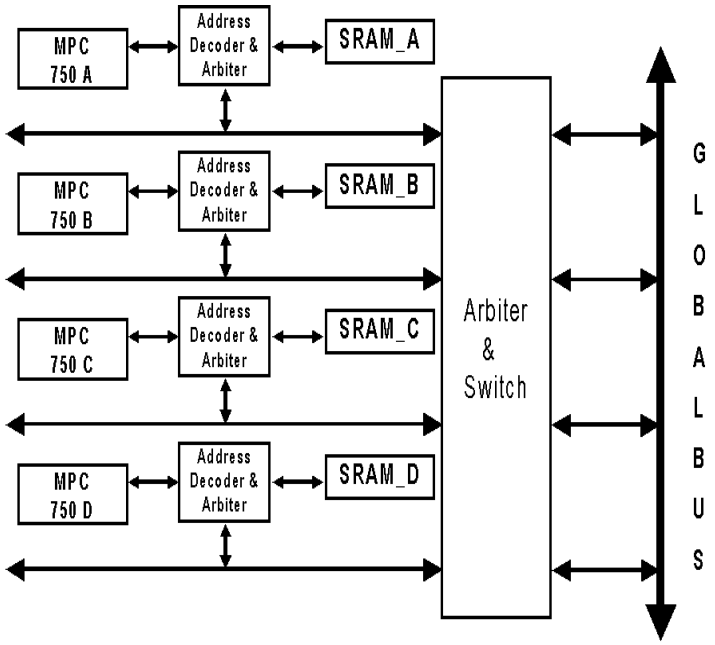
- Global Bus I Architecture (GBIA)



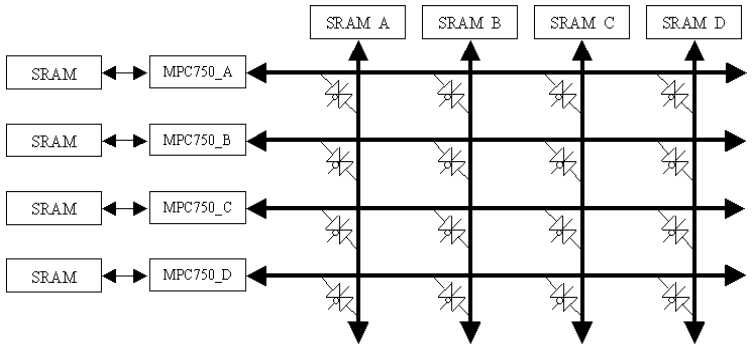
Georgia Institute of Technology

Five Bus Architectures for 4 processor System (II)

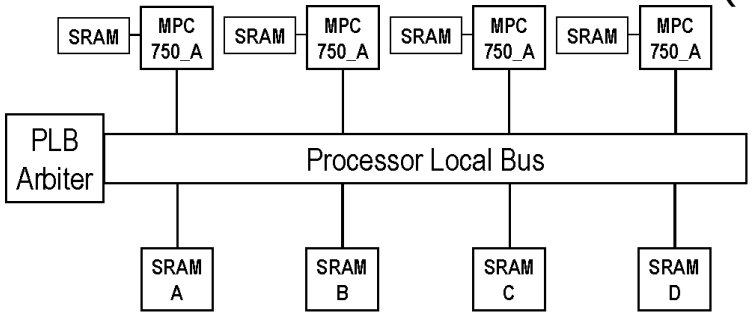
- Global Bus II Architecture (GBIIA)



- Crossbar Switch Bus Architecture(CSBA)



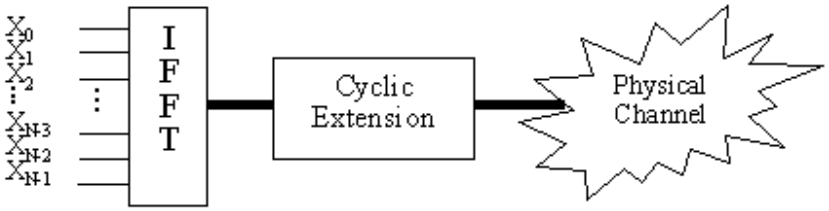
- IBM CoreConnect Bus Architecture(CCBA)



Georgia Institute of Technology

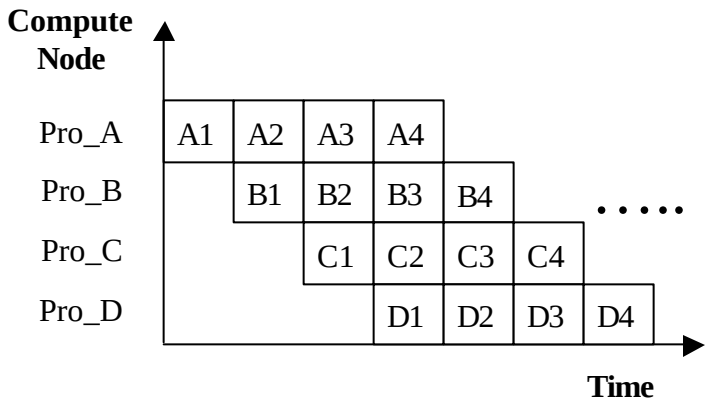
Application Examples (I)

- OFDM Transmitter
  - Block Diagram



  - Data Format: 32 guard samples and 128 data samples
  - Function Assignment

Compute Node	Assigned Functions
A	*Initialization (channel parameter, etc)* *Train Pulse Generation* *Symbol Generation* Data Generation & Symbol Mapping Bit Reversal for Inverse FFT
B	Inverse FFT
C	Normalizing IFFT
D	Normalization Insertion of Guard Signal

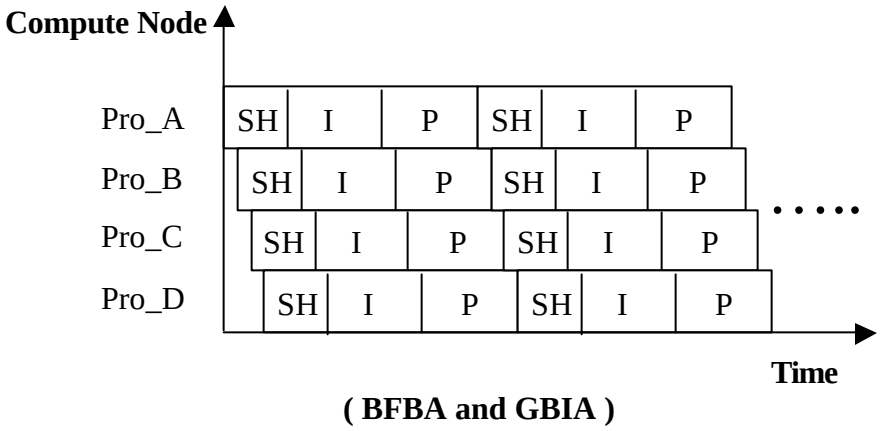


Reference: D. Kim and G. L. Stüber, "Performance of Multiresolution OFDM on Frequency-selective Fading Channels," IEEE Transaction on Vehicular Technology, vol. 48, no. 5, pp. 1740-1746, September 1999.

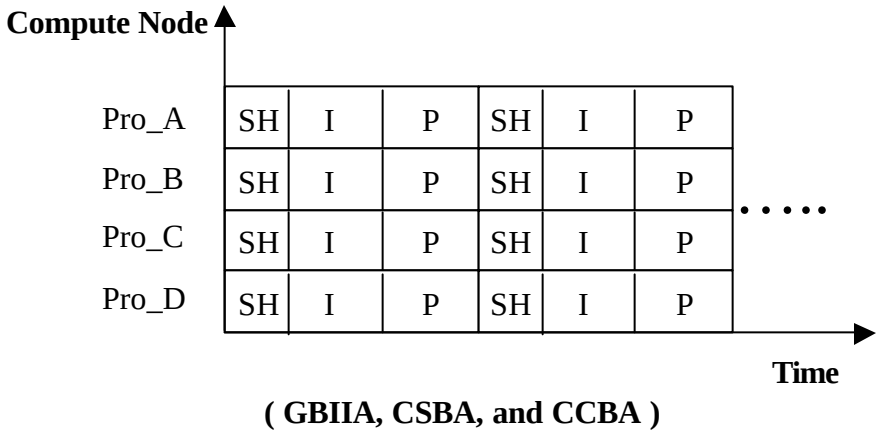
Application Examples (II)

- MPEG2 Decoder
  - Video Processing Example

    16 x 16 pixel resolution, M=1, N=2



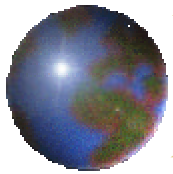
(BFBA and GBIA)



(GBIIA, CSBA, and CCBA)

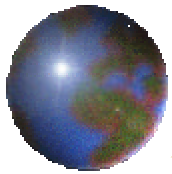
SH: Sequence header, I: Intra decoding frame, P: Predictive decoding frame

Georgia Institute of Technology



Experiment Environment

- Co-simulation Environment
  - Seamless CVE
    - co-simulator from Mentor Graphics
  - VCS
    - A Verilog HDL simulator from Synopsys
  - XRAY
    - A High-level debugger from Mentor Graphics
  - PowerPC C cross compiler
    - GCC
  - External Clock of PowerPC 750
    - 83.33 MHz (the internal clock speed can be much faster, e.g., 400MHz)



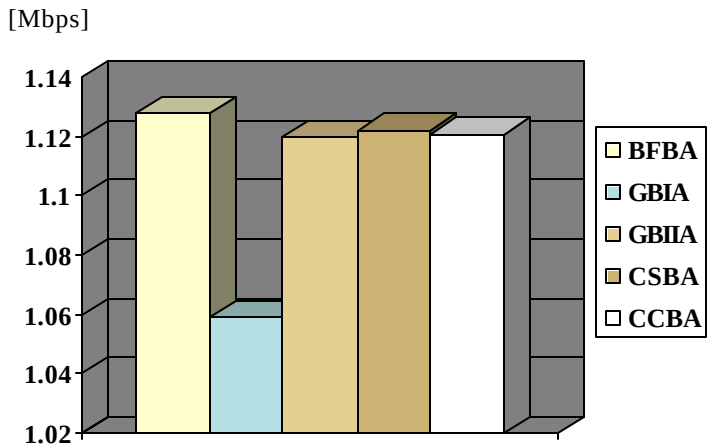
Comparison in View of Algorithm and Architecture

- Algorithm
  - OFDM Transmitter
    - Strong output-data dependency between functions using many local variables
    - Many short loops
    - Few global variables
  - MPEG2 Decoder
    - Many global variables for header information
    - Hierarchical data structure which has a long loop with many nested loops
- Architecture
  - BFBA and GBIA
    - No method to access global data
    - Fast data transfer between processor blocks
  - GBIIA, CSBA, and CCBA
    - Efficient access of global data

Comparison of Throughput of the Bus Architectures (I)

- OFDM Transmitter

Bus Architecture	Exe. Cycles / Packet	Exe. Time / Packet	Throughput
BFBA	378,348	4.5402 ms	1.1277Mbps
GBIA	403,000	4.8360 ms	1.0588Mbps
GBIIA	381,061	4.5727 ms	1.1197Mbps
CSBA	380,199	4.5624 ms	1.1222Mbps
CCBA	380,686	4.5682 ms	1.1208Mbps



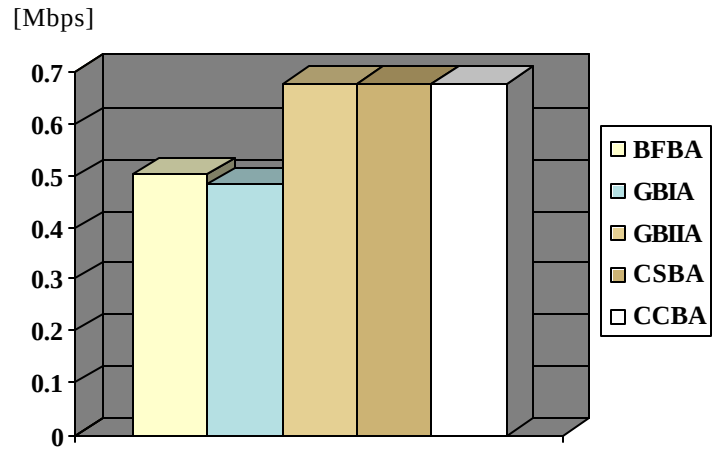
Reference: 128 data samples and 32 guard samples per packet

Georgia Institute of Technology

Comparison of Throughput of the Bus Architectures (II)

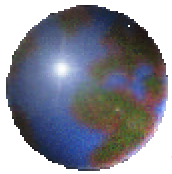
- MPEG2 Decoder

Bus Architecture	Exe. Cycles/Packet	Exe. Time/Packet	Throughput
BFBA	507,853	6.0942 ms	0.5041Mbps
GBIA	527,545	6.3305 ms	0.4852Mbps
GBIIA	377,562	4.5307 ms	0.6780Mbps
CSBA	377,548	4.5306 ms	0.6781Mbps
CCBA	378,181	4.5382 ms	0.6769Mbps



Reference: 128 data samples and 32 guard samples per packet

Georgia Institute of Technology



Conclusion

- Five bus architectures evaluated
  - BFBA, GBIA, GBIIA, CSBA, and CCBA
- Two application programs
  - OFDM transmitter and MPEG2 decoder
- Pipeline or parallel operation improves performance
- BFBA best for OFDM
  - pipelined applications
- CSBA best for MPEG2
  - parallel applications
- bus architecture performance heavily dependent on
  - distribution of computation load
  - algorithm style
- Future work: combine the bus architectures with switching logic to maximize performance according to application characteristics

Georgia Institute of Technology