# Error-Rate Prediction for Probabilistic Circuits with More General Structures

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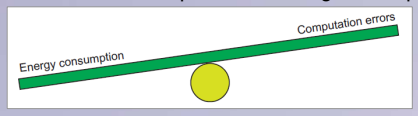
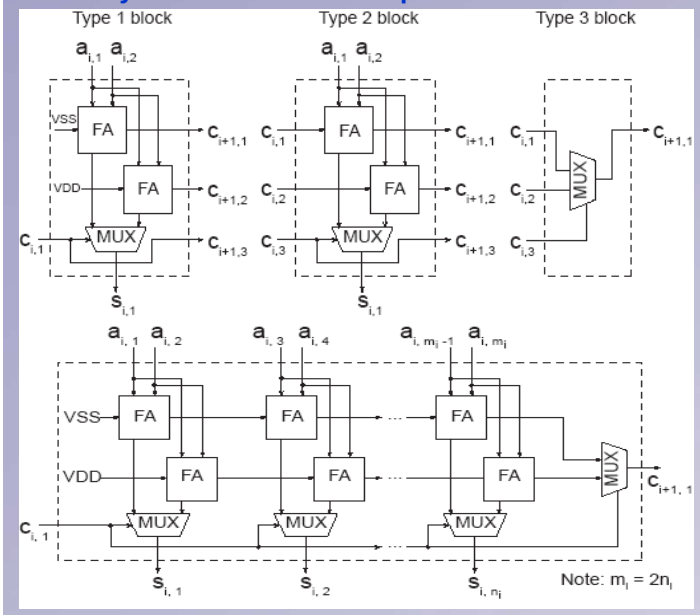
**Abstract.** A methodology has been proposed recently to predict error-rates of probabilistic circuits having a cascade structure. The objective of this poster is two fold. First, the methodology is applied, for the first time in the literature, to a probabilistic carry select adder, which has a more complex structure than the adders mentioned in previous papers. Second, it shows that the methodology is also applicable to some seemingly non-cascade circuits. The key technique is to appropriately group circuit components into various blocks before applying the methodology.

## 0. What is probabilistic computing?

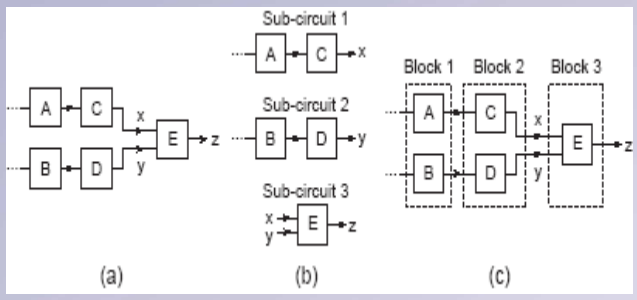
- Technology that allows computation with occasional erroneous arithmetic operations [1].
- Trading correctness of circuit operations for significant power saving.



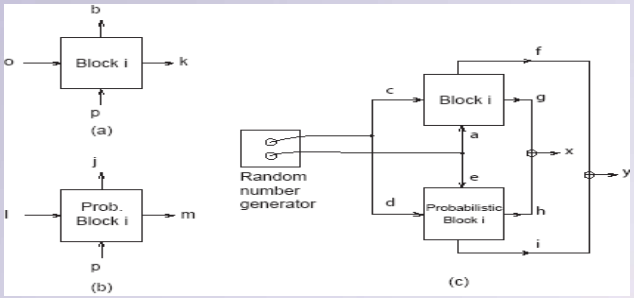

## II. Carry Select Adder Decompositions



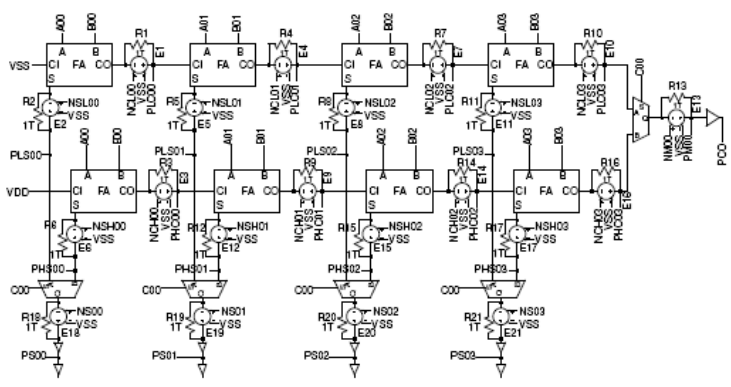

## I. Cascade structure transformation



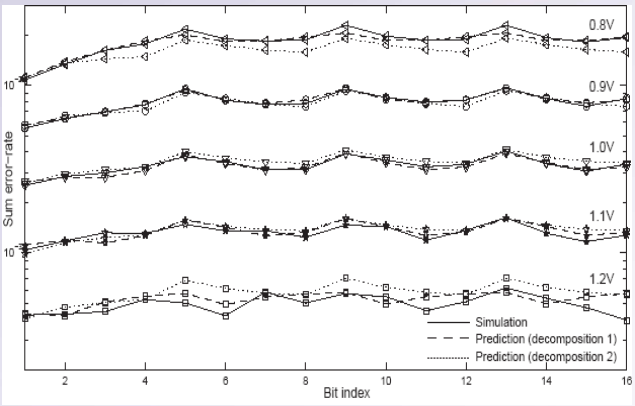

## III. Characterizing a Probabilistic Block




## IV. HSPICE Setup for Probabilistic Carry Select Adder.



## V. Application to Probabilistic Carry Select Adder




## V. References

[1] Palem, "Energy aware computing through probabilistic switching: a study of limits," IEEE Transactions on Computers, vol. 54, no. 9, pp. 1123-1137, 2005.
[2] George et al., "Probabilistic arithmetic and energy efficient embedded signal processing," Proceedings of CASES 2006, pp. 158-168, 2006.
[3] Lau et al., "Modeling of probabilistic ripple-carry adders," Proceedings of DELTA 2010.
[4] Lau et al., "Error-rate prediction for a class of probabilistic circuits with applications to carry-skip adders," submitted to 16th ASP-DAC.