

## Yamacraw Research Program in Embedded Software

# A Debugger RTOS for Embedded Systems

**Faculty : Vincent Mooney, Vijay Madisetti**

**Students : Tankut Akgul, Pramote Kuacharoen**

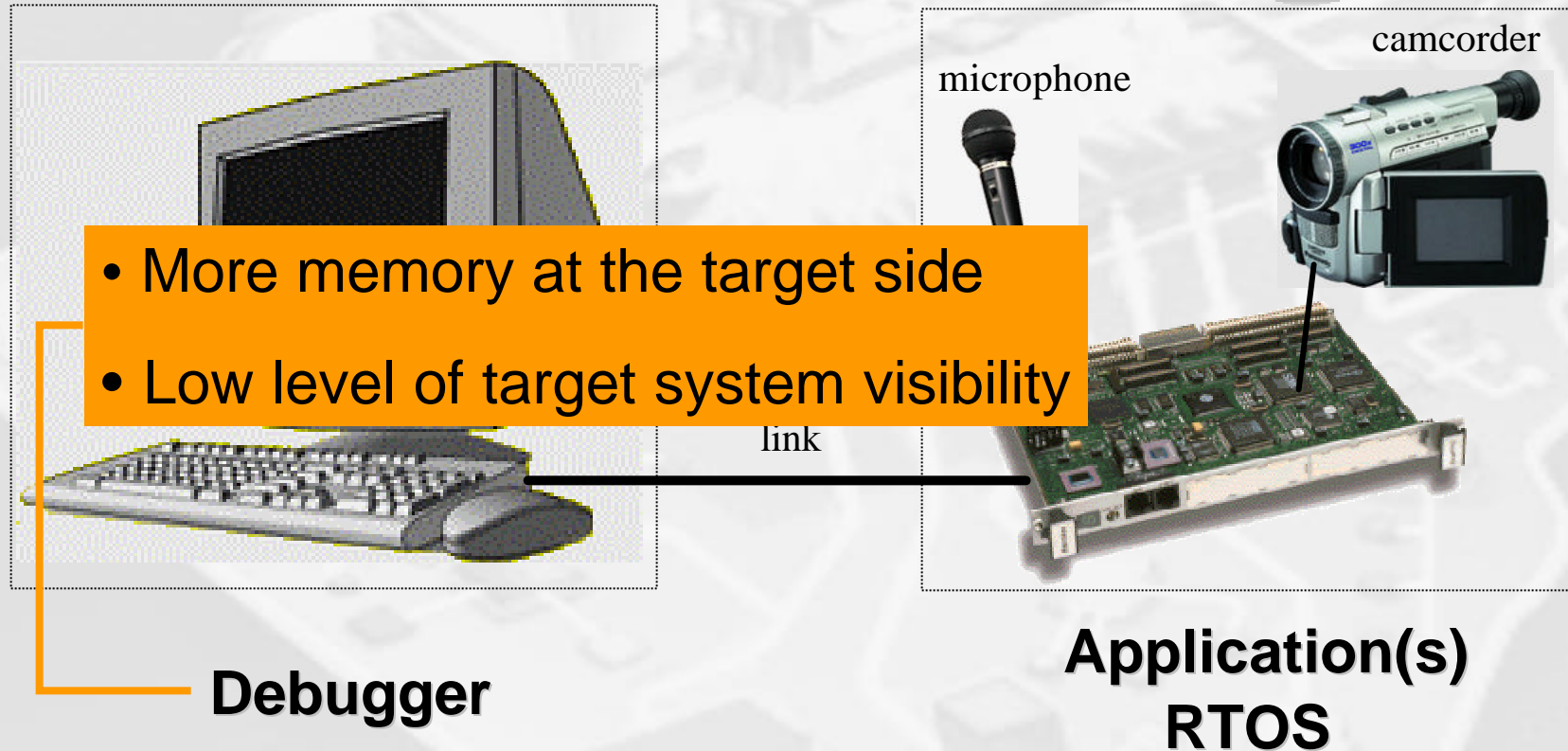
# Outline

- Background and Motivation
- Approach
- Architecture
- Example
- Conclusion

# Background and Motivation

## Host

## Target



# Background and Motivation

## Host

## Target



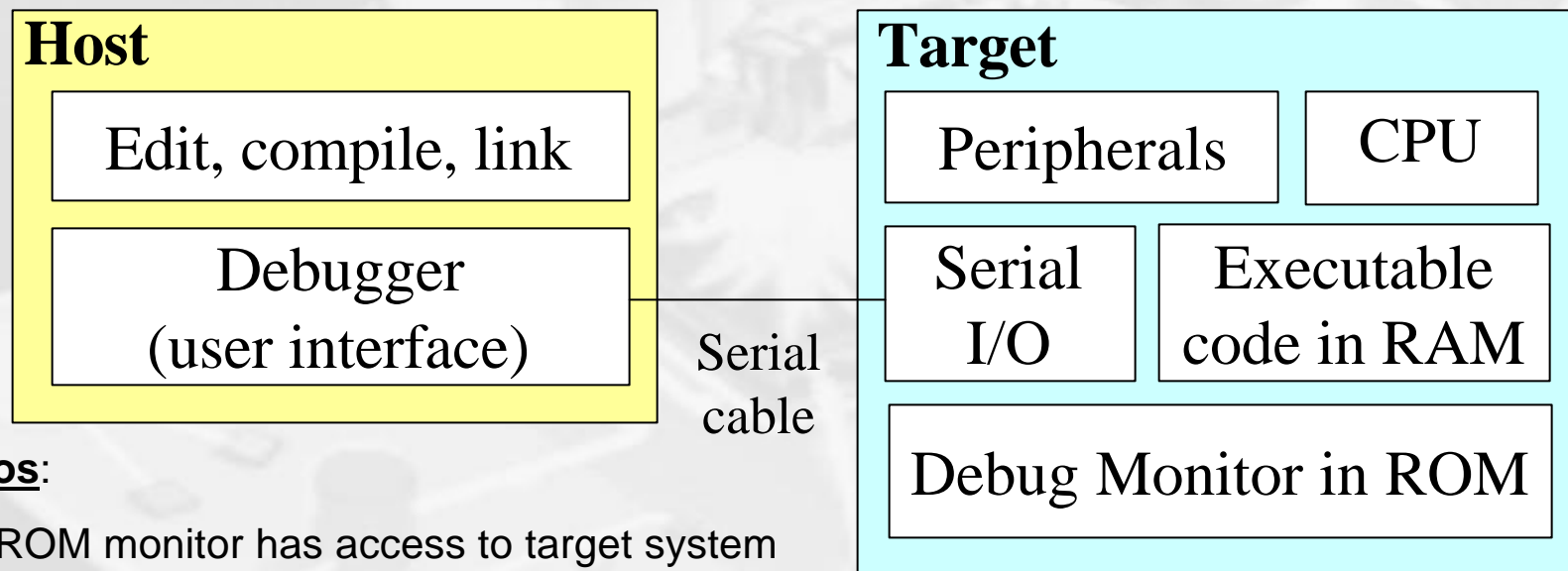
- Less memory at the target side
- High level of target system visibility

communication link

Application(s)  
RTOS  
Debugger

# Background and Motivation

## ROM (Debug) Monitor



### Pros:

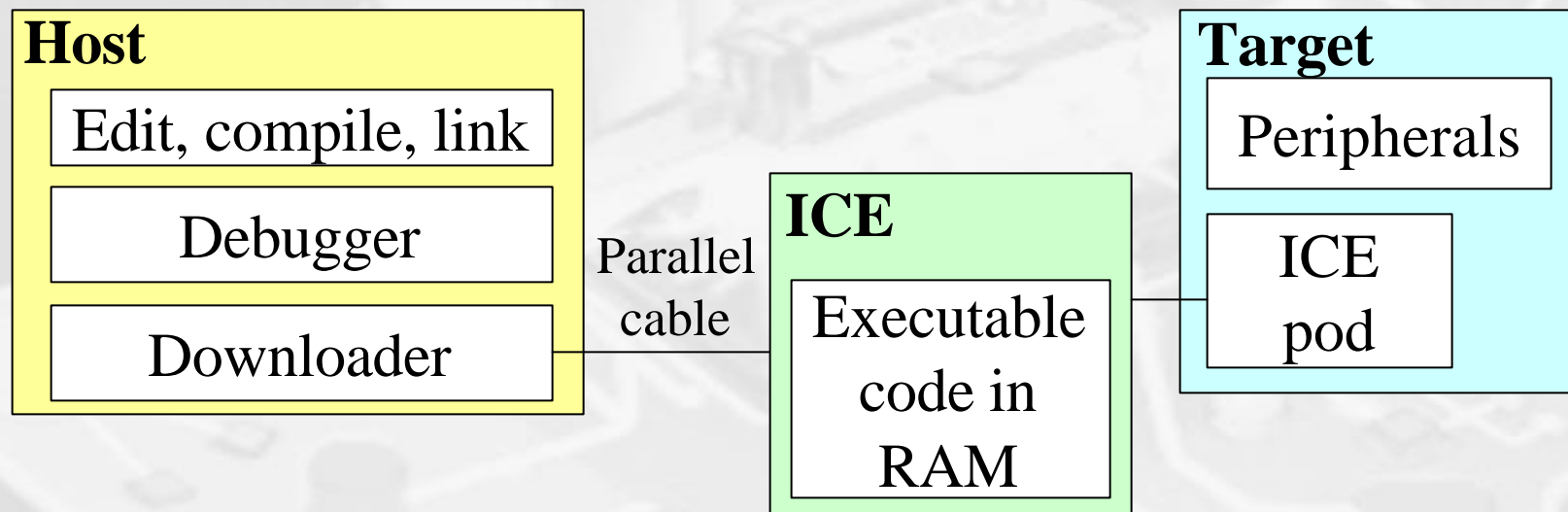
- ROM monitor has access to target system internals

### Cons:

- Hard to remove the ROM monitor from the final product
- Fixed monitor code once burned into ROM

# Background and Motivation

## In-Circuit-Emulator (ICE)



### Pros:

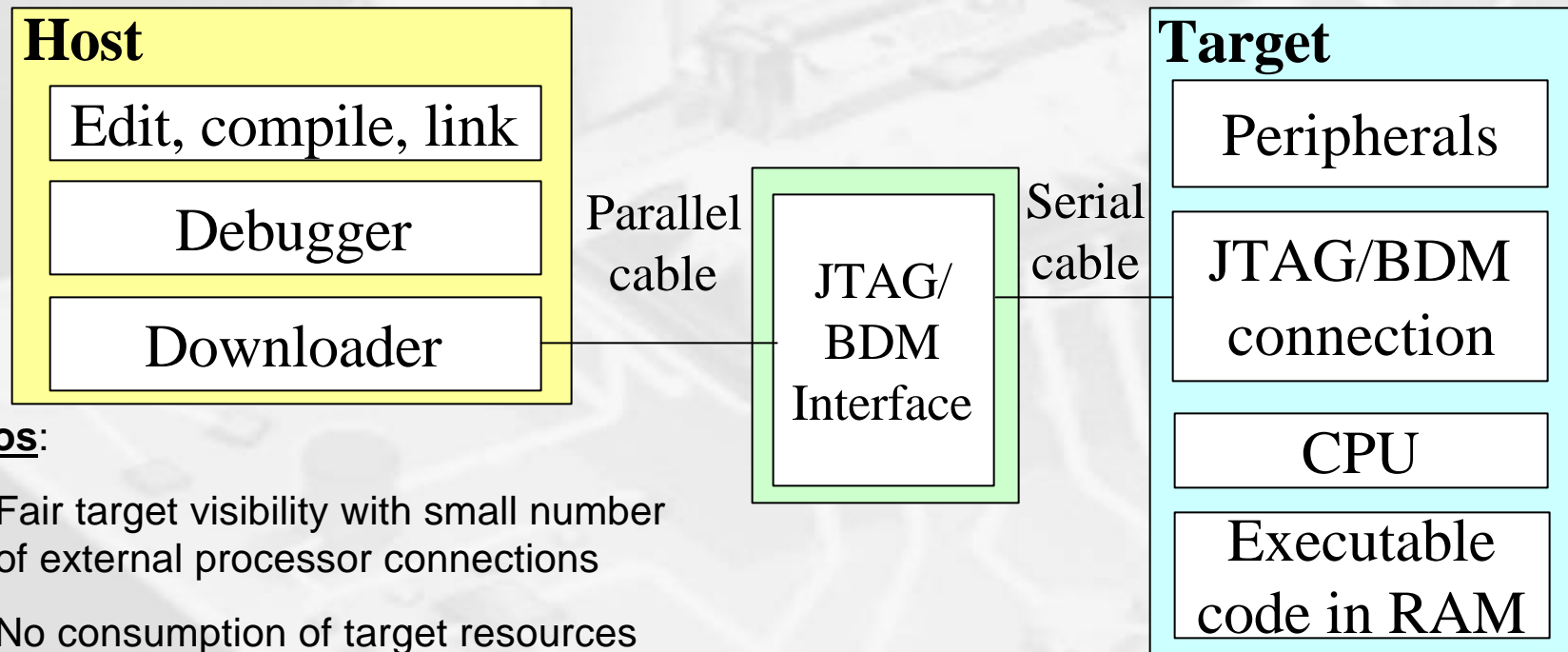
- Real-time event detection, real-time tracing

### Cons:

- Expensive
- Lags processor production time
- Does not work well with high speed signals
- Impractical to use with highly embedded cores

# Background and Motivation

## JTAG/Background Debug Mode (BDM)



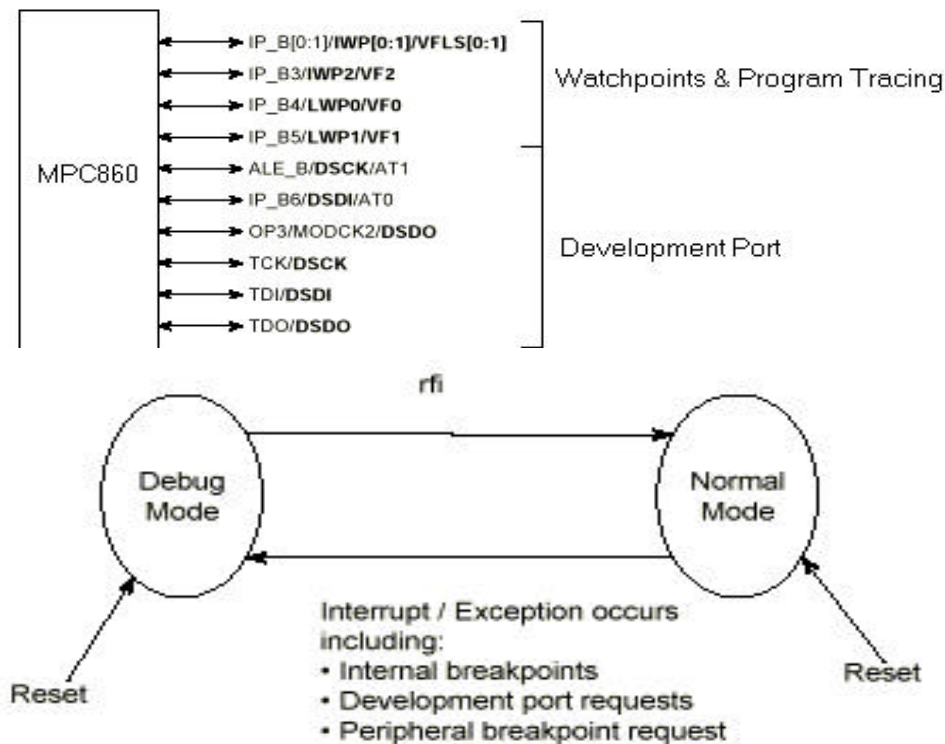
**Pros:**

- Fair target visibility with small number of external processor connections
- No consumption of target resources

**Cons:**

- Requires on-chip hardware support
- Not suitable for real-time debugging

# Example 1: BDM with MPC860



- User can set at most 5 watchpoints in software. Whenever these watchpoints are reached, external pins are asserted.
- The processor, if programmed, goes into the debug mode on exceptions, and stops execution. Then, a remote debugger can send commands to the processor through the processor's external pins.



# Example 2: Incorrect Program Trace

```
...  
If (x>0) {  
  ! sum = sum + x;  
  printf("x is positive");  
  ....  
}  
else {  
  sum = sum - x;  
  printf("x is negative");  
  ....  
}
```

Breakpoint inserted →

- Branch prediction hardware predicts "x>0",
- Pre-fetcher fetches instruction here,
- Traditional host debugger monitors address of this instruction on external signals, breaks there,
- Prediction is wrong, branch not taken ⇒ trace is incorrect !
- On-chip debugger has full knowledge of internal signals, this misbehavior never happens!

# Approach

## Just-in-time Debugging

- Debugger software is a loadable module of the RTOS
- Buggy code runs on the processor until an exception condition or an algorithmic error occurs.
- Debugger is dynamically loaded by the exception handler.

## Automatic Error Detection

- **Algorithmic errors**
  - E.g., functional errors, timing errors, synchronization errors.
- **Hardware Exceptions**
  - E.g., alignment errors, software emulation

# Approach

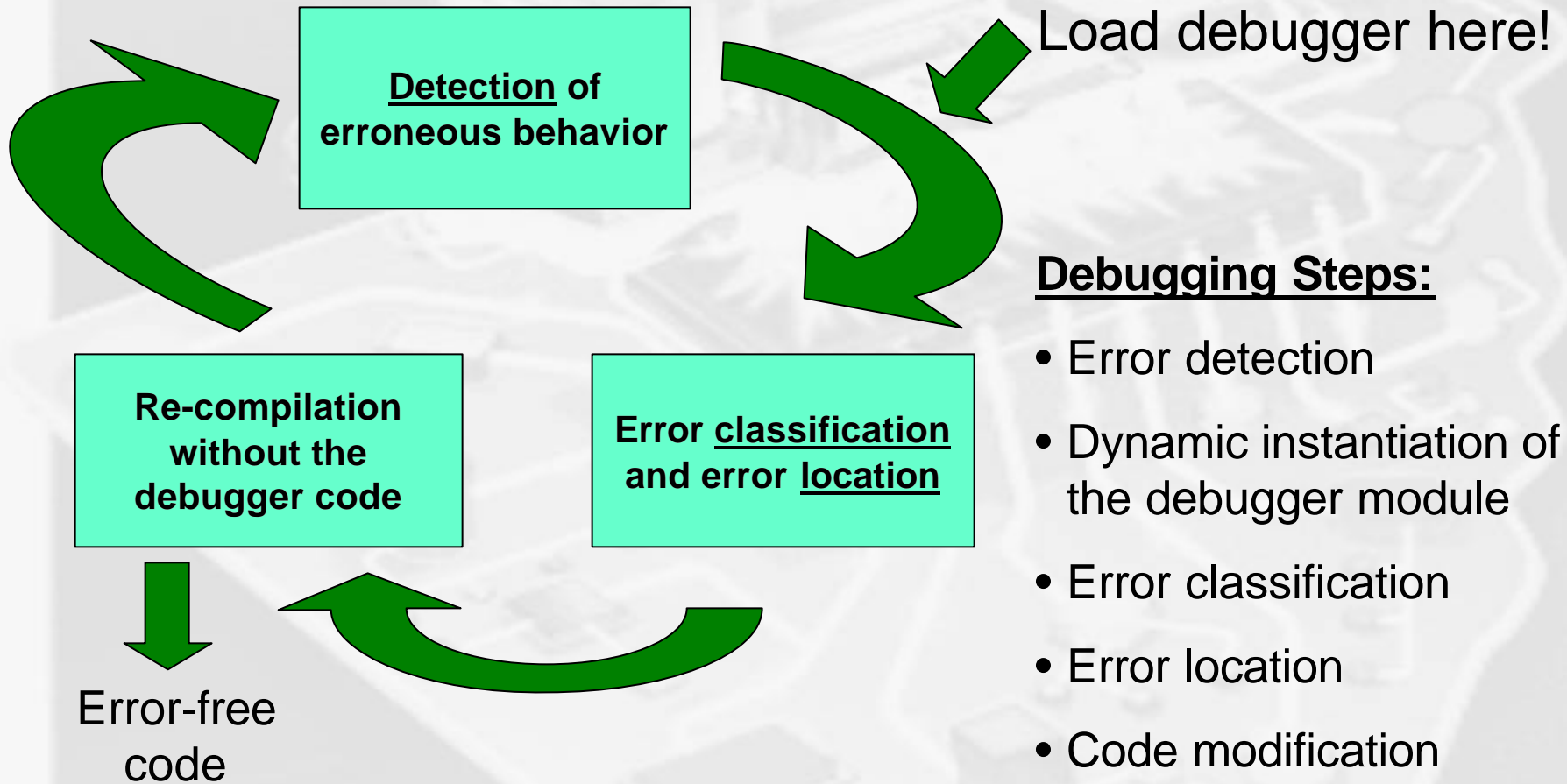
## Error Monitor

- Always resident inside RTOS
- Responsible for the detection of errors and the instantiation of the debugger part

## Debugger Module

- Responsible for classifying, and locating errors in the program
- Provides debugging features such as memory dump, and register display

# Approach



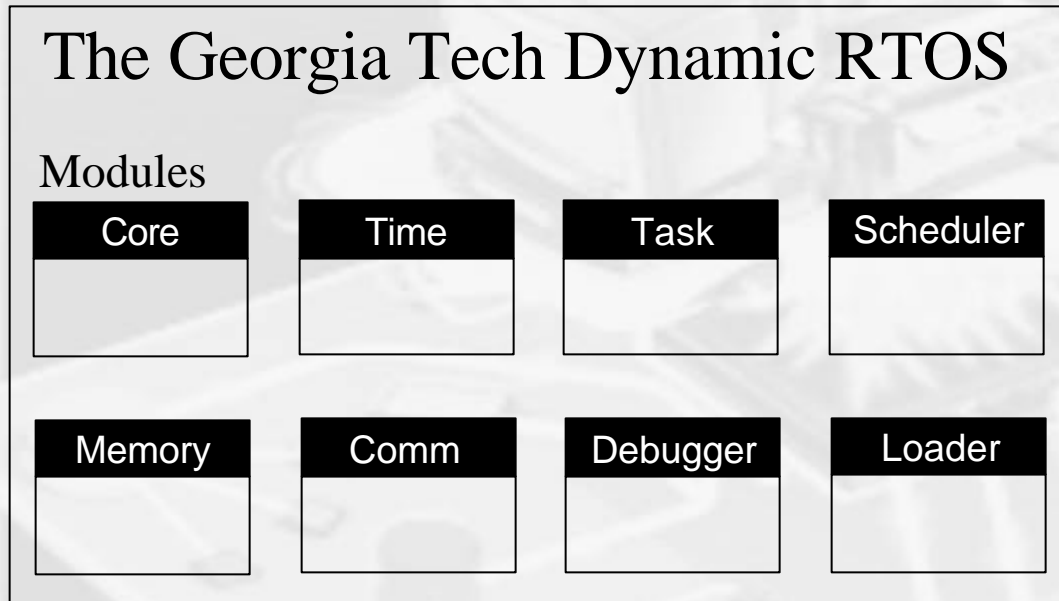
## Debugging Steps:

- Error detection
- Dynamic instantiation of the debugger module
- Error classification
- Error location
- Code modification
- Code re-compilation

# Future Improvements

- Current features of the debugger module:
  - Error classification
  - Error location for immediately locatable errors
  - Display of register values
- Future improvements:
  - Incremental instantiation of additional features
  - Breakpointing
  - Source line stepping
  - On the fly variable query and modification
  - Profiling

# Architecture

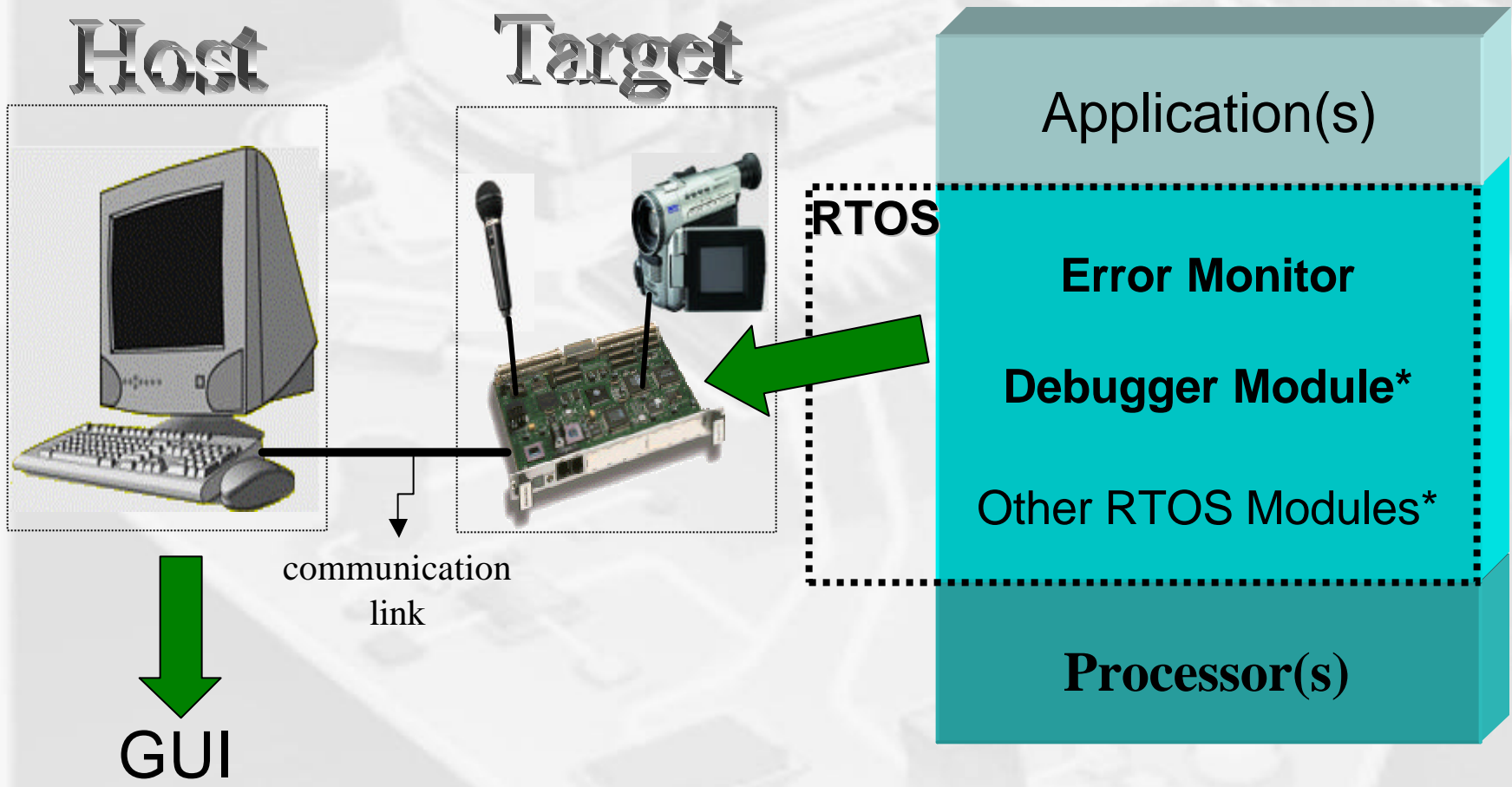


Reference:

P. Kuacharoen, T. Akgul, V. J. Mooney, V. K. Madiseti, "Adaptability, Extensibility, and Flexibility in Real-Time Operating Systems", *Euromicro Symposium on Digital System Design*, September 2001.

Core Module	
Text	Executable code
Data	Module Variables System APIs Core Time Task Scheduler Memory Communication Debugger Loader

# Architecture



\* Dynamically loadable

# Architecture

Module Table

Function name	Address
Debugger	0xFF000000
Scheduler	0xFA000000
...	...

Global Variable Table

Global var.	Address
cur_task_ID	0xFF00A000
TCB_list	0xFFF00B00
...	...

**load\_module\_debugger() {**

①  
}

**init\_module\_debugger() {**

②, ③  
}

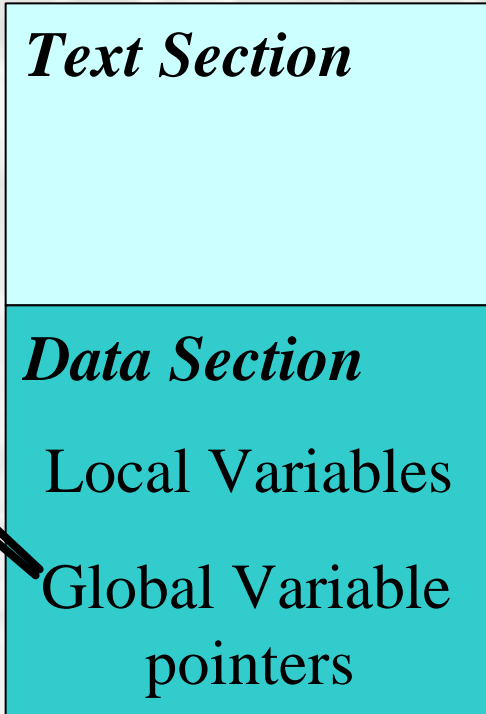
① Load debugger module into memory

②

0xFF000000

③

Debugger Module





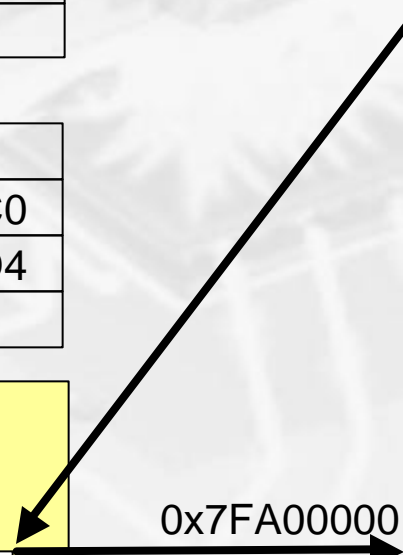
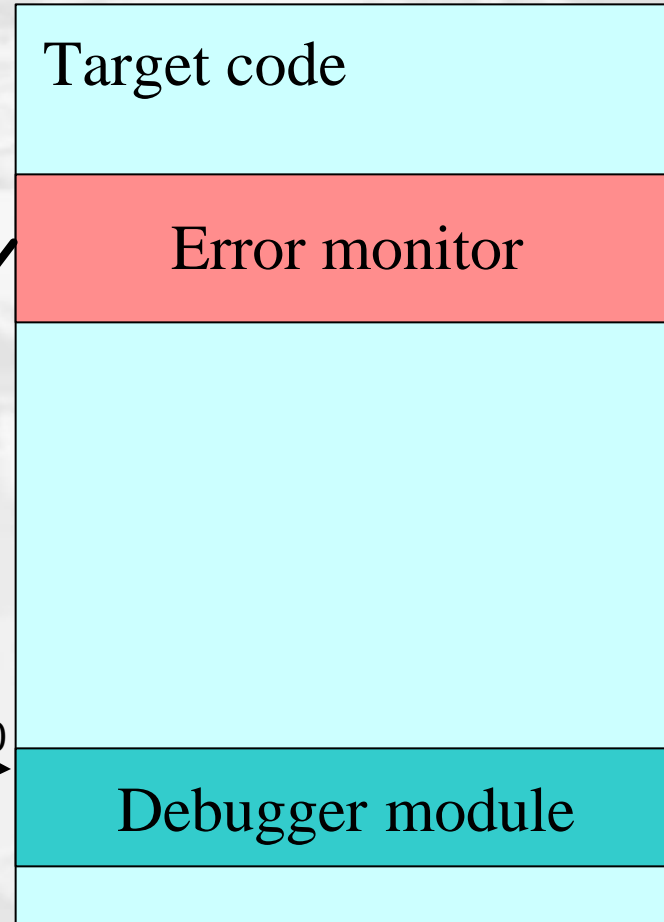
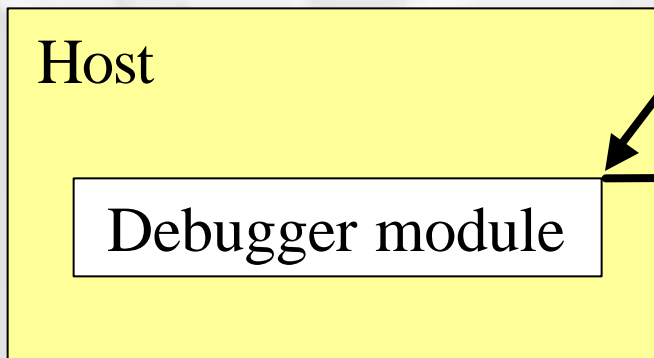
# Example

Module Table

Function name	Address
Debugger	
Scheduler	0x7C00000
...	...

Global Variable Table

Global Var.	Address
cur_task_ID	0x581000C0
TCB_list	0x581000D4
...	...



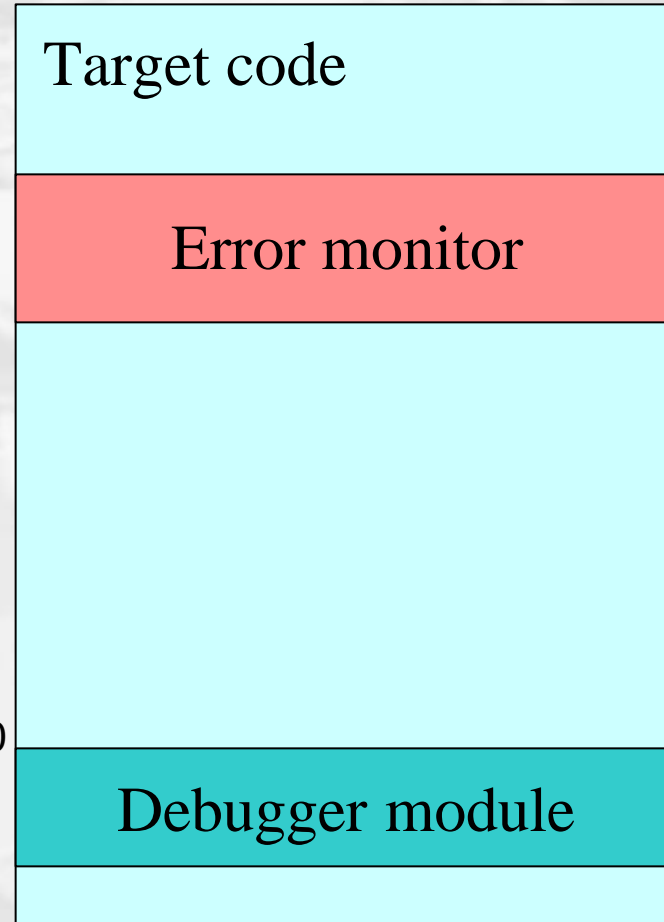
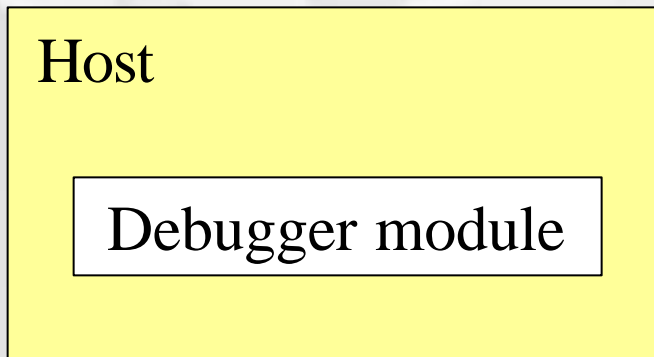
# Example

Module Table

Function name	Address
Debugger	0x7FA00000
Scheduler	0x7C000000
...	...

Global Variable Table

Global Var.	Address
cur_task_ID	0x581000C0
TCB_list	0x581000D4
...	...



0x7FA00000

# Example

Module Table

Function name	Address
Debugger	0x7FA0000
Scheduler	0x7C00000
...	...

Global Variable Table

Global Var.	Address
cur_task_ID	0x581000C0
TCB_list	0x581000D4
...	...

Host

Debugger module

Target code

Error monitor

Debugger module

# Example Application

- Repeatedly gets two floating point voltage samples from two different locations in memory
- Converts collected voltage samples into integer values
- Calculates the ratio of the samples

```
int find_ratio(v1, v2)
```

```
{
```

```
    v1 = (int) get_voltage(loc1);
```

```
    v2 = (int) get_voltage(loc2);
```

```
    return (v1/v2);
```

```
}
```

Creates divide-by-zero  
algorithmic error\* when  $v2 = 0$

\* MPC860 does not have an exception for the integer divide-by-zero error.

# A Snapshot of the GUI

The screenshot displays a software interface with two main panels. The left panel, titled "VIO Stream: 0", contains a text-based error report. The right panel features two vertically stacked graphs with interactive toolbars.

**Error Report:**

```
Error occurred in program at address: 0x35f10
Error type: Divide by zero

R0: 0x35f10   R11: 0x0     R22: 0x0
R1: 0x9160    R12: 0x0     R23: 0x0
R2: 0x4080    R13: 0x4000  R24: 0x0
R3: 0x4074    R14: 0x0     R25: 0x0
R4: 0x0       R15: 0x0     R26: 0x0
R5: 0x0       R16: 0x0     R27: 0x0
R6: 0x0       R17: 0x0     R28: 0x0
R7: 0x0       R18: 0x0     R29: 0x0
R8: 0x0       R19: 0x0     R30: 0x0
R9: 0x0       R20: 0x0     R31: 0x0
R10: 0x0      R21: 0x0
MSR: 0x9002   SRR0: 0x35f10 SRR1: 0x9002
CR: 0xe0e1e2e3 LR: 0x35f2c IAR : 0x3f0c

Current thread ID: 3
Current thread stack address: 0xd0f0

Thread states
-----
Thread 1 : Waiting
Thread 2 : Waiting
Thread 3 : Running
Thread 4 : Ready
```

**Graphs:**

- Time domain:** A plot showing a periodic waveform (sine wave) over a time axis from 0 to 60. The y-axis is unlabeled.
- Power & phase:** A plot showing a signal that starts with high-frequency oscillations and then transitions to a steady linear increase. The x-axis is labeled from 0 to 60, and the y-axis is labeled from 0 to -8.

At the bottom of the interface is a "Command:" input field.

# Conclusion

- ☑ • Efficient Memory Usage
- ☑ • Capability for detecting algorithmic errors
- ☑ • No extra hardware for debugging
- ☑ • Correct debugging in a highly coupled and parallel environment