

Assembly Instruction Level Reverse Execution for Debugging

PhD Dissertation Defense

by

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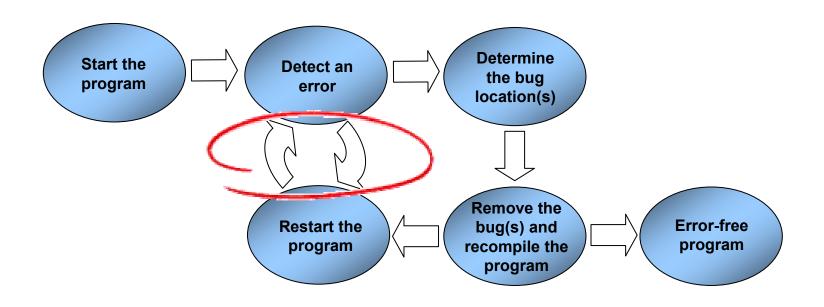


Outline

- Background
- Reverse Execution
 - Definition
 - Previous Work
- Reverse Execution Methodology
- Program Slicing
 - Definition
 - Previous Work
- Program Slicing Methodology
- Experimental Results



Background



Debugging is a repetitive process!



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Definition of Reverse Execution

- **Reverse execution**: Taking a program *T* from its current state S_i to a previous state S_i
- Source code level reverse execution: Reverse execution where S_j can be as early as one source code statement before state S_j
- Instruction level reverse execution: Reverse execution where S_j can be as early as one assembly instruction before state S_j



Previous Work

Debugging

- Optimistic Simulations
- Database Applications
- Interactive Systems
 - Editors
 - Program development environments

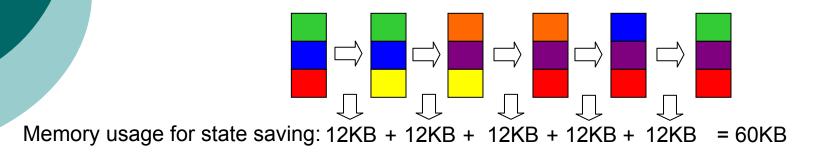


Restore earlier state

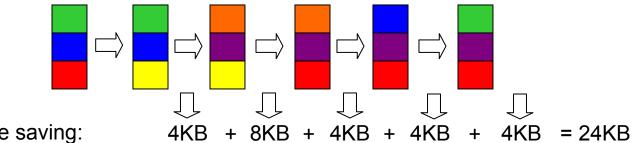
- Periodic checkpointing
- Incremental checkpointing
- Regenerate part of earlier state
 - Source transformation
- Build a reversible processor with reversible circuit elements (Pendulum)



Periodic checkpointing:



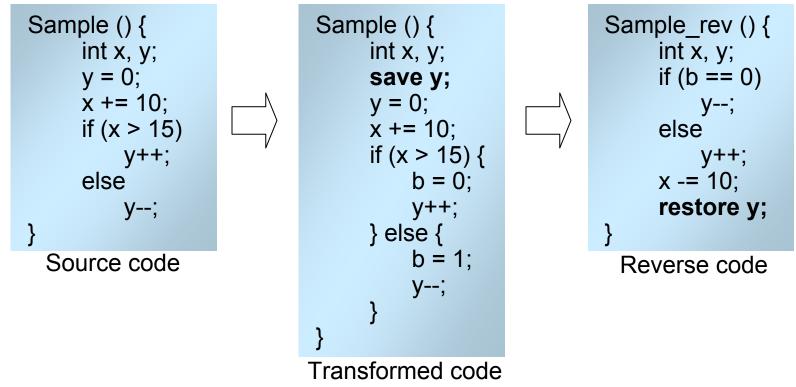
Incremental checkpointing:



Memory usage for state saving:



Source Transformation:



State saved for each *destructive* operation

Destructive operation: An operation whose target operand is different than its source operands

C. Carothers, K. Perumalla and R. Fujimoto, "Efficient Optimistic Parallel Simulations using Reverse Computation," in *Proceedings of ACM/IEEE/SCS Workshop on Parallel and Distributed Simulation (PADS)*, Atlanta, USA, May 1999.



Heavy use of state saving

 State saving = memory and time overheads during forward execution

 No direct instruction level reverse execution support



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Assumptions:

- State that cannot be modified directly does not include debugging information
 - E.g., condition status register
- Physical memory is treated as a uniform entity
 - Exact physical memory state is not preserved
 - E.g., a value not in cache can be brought into cache after recovery
- Sequential execution model
- Indirect calls are made to well-defined target points



We define the state of a processor as follows:

- $\mathsf{S}=(\,\mathsf{PC}\,,\,\mathsf{M}'\,,\,\mathsf{R}'\,)$
- *PC* : program counter
- M' : directly modified memory values
- R': directly modified register values

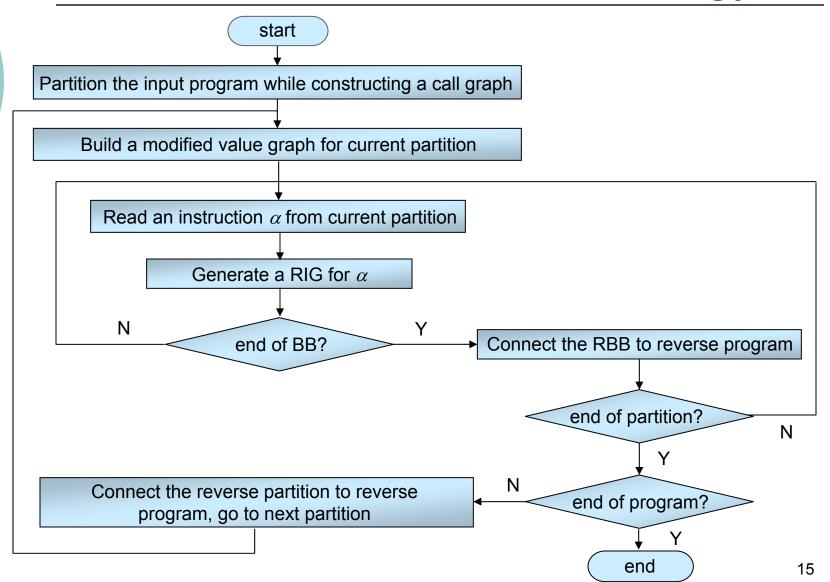
In order to reverse execute a program, do the following:

- Construct a reverse program *RT* for an input program *T*
- Recover M' and R' by executing RT in place of T
- Recover the program counter value by using the correspondence between *T* and *RT*

Reverse Code Generation (RCG) steps:

- 1. Divide the original program into program partitions
- **2.** Generate the reverse of the instructions. The reverse of an instruction is called a *Reverse Instruction Group* (*RIG*)
- **3.** Combine the RIGs
 - **3.a** Combine the RIGs to generate the reverse of each basic block (*RBB*)
 - **3.b** Combine the RBBs to generate the reverse of each partition
 - **3.c** Combine the reverse partitions to generate the reverse of whole program





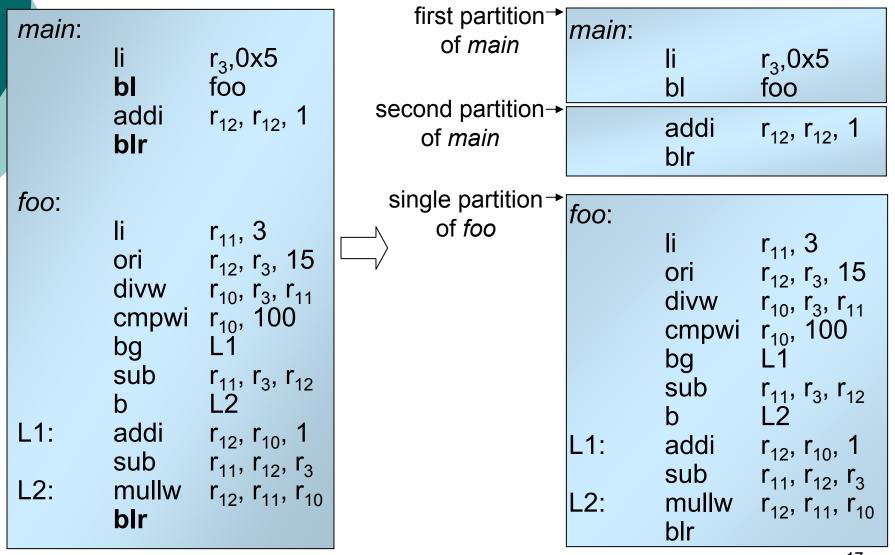


Step 1: Program Partitioning

- Partitions are regions of code delimited by "function call" or "indirect branch" instructions that may exist within the original code
 - e.g., in PowerPC instruction set:
 - *bl* : function call instruction
 - *blr* : branch to link register instruction (indirect)

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Step1: Program Partitioning





Methodology (Continued)

Reverse Code Generation (RCG) steps:

- **1.** Divide the program into program partitions (single entrysingle exit regions).
- **2.** Generate the reverse of the instructions. The reverse of an instruction is called a *Reverse Instruction Group* (*RIG*)
- 3. Combine the RIGs
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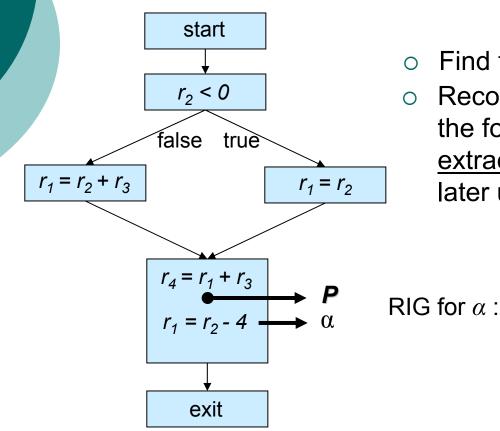


Step 2: RIG Generation

- Three techniques to generate a RIG:
 - 1. Re-define technique
 - 2. Extract-from-use technique
 - 3. State saving technique



Step 2: RIG Generation (Cont.)



Find the definitions of r₁ reaching *P* Recover r₁ by selectively <u>re-executing</u> the found definitions or by selectively <u>extracting</u> the found definitions out of later uses of those definitions

$$r_1 = r_4 - r_3$$
 or

if
$$r_2 < 0$$

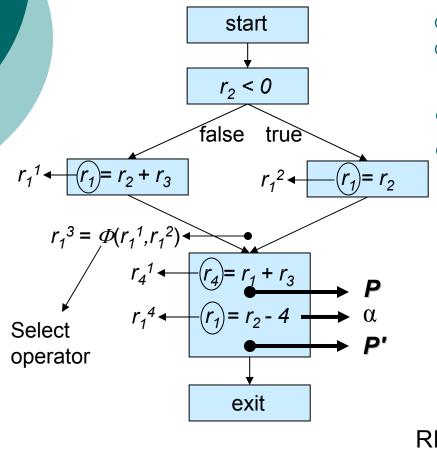
 $r_1 = r_2$
else
 $r_1 = r_2 + r_3$

Extract-from-use

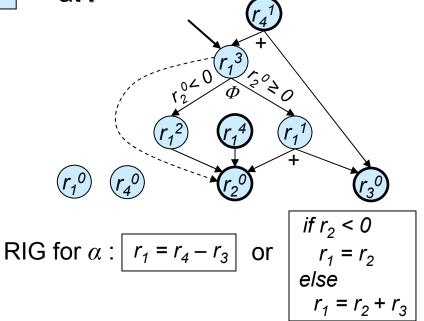
Re-define



Step2: RIG Generation (Cont.)



- Rename Values
- Generate a *directed graph* called modified value graph (*MVG*)
- Find the definition of r₁ reaching *P* Recover r₁ using available nodes at *P*'





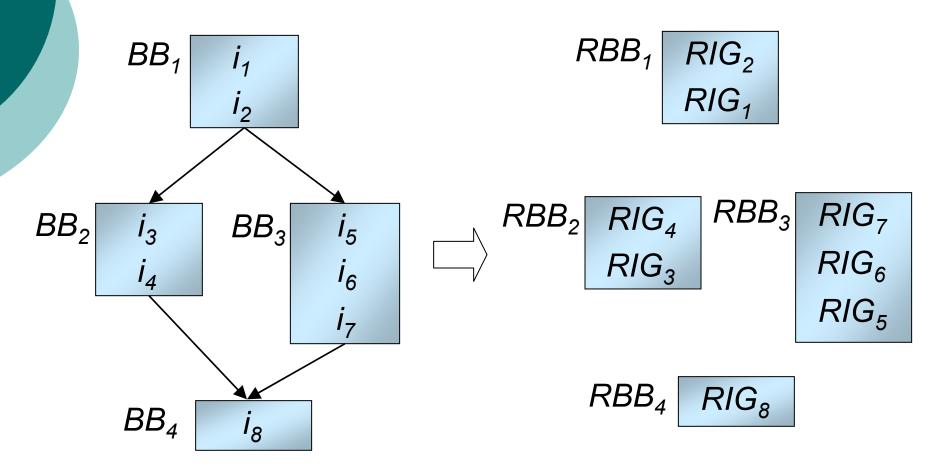
Methodology (Continued)

Three steps to generate a complete reverse program:

- **1.** Divide the program into program partitions (single entrysingle exit regions).
- **2.** Generate the reverse of the instructions. The reverse of an instruction is called a *Reverse Instruction Group* (*RIG*)
- 3. Combine the RIGs
 - **3.a** Combine the RIGs to generate the reverse of each basic block (*RBB*)
 - **3.b** Combine the RBBs to generate the reverse of each partition
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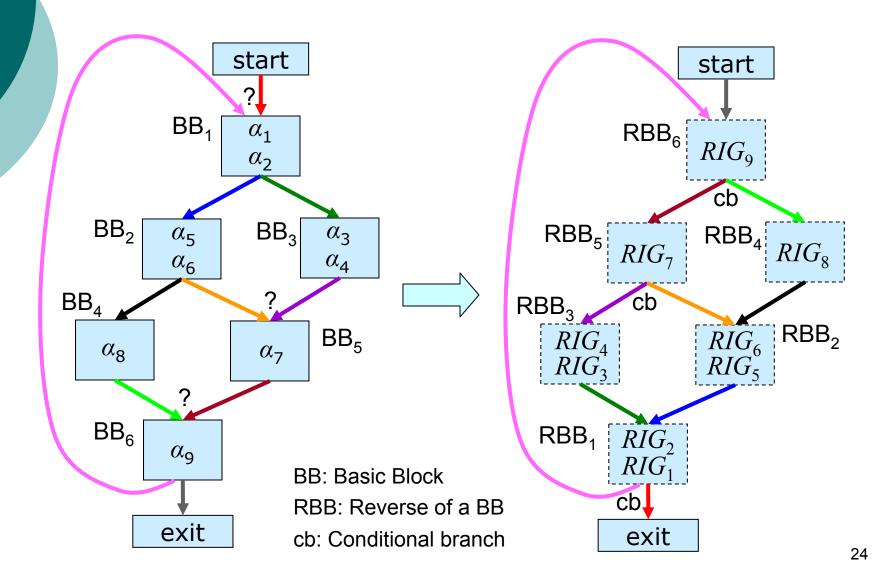
Step 3.a: Constructing the RBBs



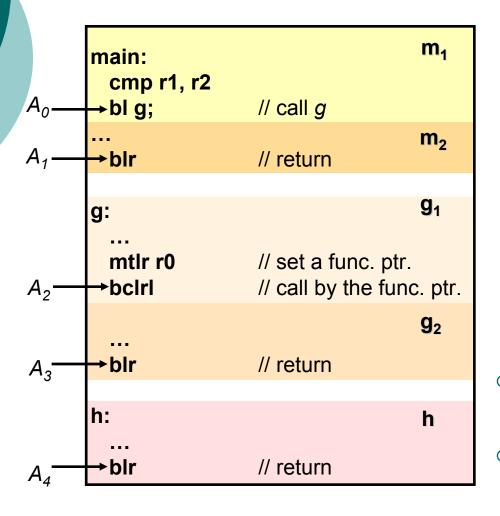
Bottom-up placement order within BBs

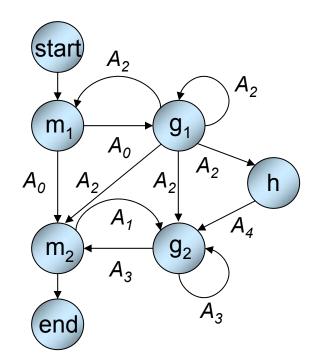


Step 3.b: Combining the RBBs



Step 3.c: Combining the Reverse Partitions

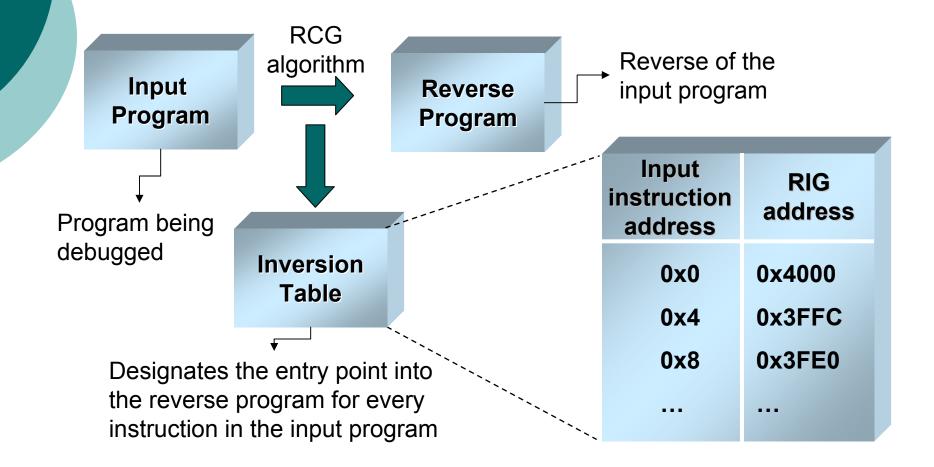




- Push addresses on the dynamically taken edges into stack
- Pop the addresses from stack during reverse execution and branch to reverses of popped addresses



Recovering the Program Counter





Complexity

Byte Recover (Node n)

```
if (n.available == true)
    return true;
\forall m \in children(n) do \{
    stat = Recover(m);
 if stat != available
    break;
\forall m \in parents(n) do \{
    stat = Recover(m);
    if (stat == available) {
         \forall z \in siblings(n) do {
             stat = Recover(z);
             if (stat != available)
                 break;
      (stat == available)
         break;
Write_RIG();
```

- N : number of nodes in an MVG \cong # of assembly instructions in a code
- *M* : average degree of a node (# of neighbors)
- *K* : maximum number of repetitive applications of re-define and extract-from-use techniques allowed
- *M* is independent of total code size for fixed partition size

Complexity = $O(N \times M^{\kappa})$

On a 1 GHz CPU, 1 iteration \cong 1 nsec

 $N = 1,000,000, M = 10, K = 3 \rightarrow 1$ sec



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Program Slicing

 Static Slice: A set of program statements that may influence a variable V at statement S.
 C = (V, S) is a static slicing criterion.

 Dynamic Slice: A set of program statements that influence a variable V at an execution instance q of statement S given a set of program inputs X.

 $C = (X, V, S^q)$ is a dynamic slicing criterion.



Program Slicing

• Two ways to influence a variable:

Data dependency

y = z; x = y + 1;x is data dependent on y and z

Control dependency

if (y < 0)
 x = 1;
x is control dependent on y</pre>

 A slice is a set of all statements that compute dependencies of a variable



Program Slicing

```
Pass = 0;
Fail = 0;
Count = 0:
while (!eof()) {
   TotalMarks=0;
   scanf("%d",Marks);
   if (Marks \geq 40)
          Pass = Pass + 1:
   if (Marks < 40)
          Fail = Fail + 1:
   Count = Count + 1;
   TotalMarks = TotalMarks+Marks ;
average = TotalMarks/Count;
/* This is the point of interest */
printf("The average is %d\n",average);
PassRate = Pass/Count*100;
printf("Pass rate is %d\n",PassRate);
```

```
while (!eof()) {
    TotalMarks=0;
    scanf("%d",Marks);
    Count = Count + 1;
    TotalMarks = TotalMarks+Marks;
}
```

```
average = TotalMarks/Count;
printf("The average is %d\n",average);
```



Original Program



Previous Work in Program Slicing

- Static Slicing (Weiser)
 - Control flow graph analysis
 - No runtime information
- Static Slicing (Ottenstein et al.)
 - Program dependency graph analysis
 - No runtime information
- Dynamic Slicing (Korel and Laski)
 - Control flow graph analysis
 - Program execution trajectory
- Dynamic Slicing (Agrawal et al.)
 - Dynamic dependence graph (DDG) analysis
 - Program execution trajectory



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Reverse Execution Methodology

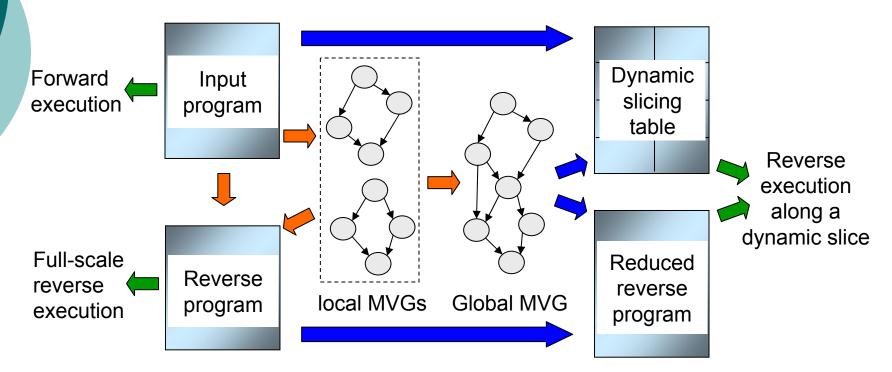
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Program Slicing Methodology

Experimental Results



RCG with Slicing (RCGS)



Orange arrows indicate the base static analysis performed only once per program Blue arrows indicate the extended static analysis performed for each dynamic slice Green arrows indicate the actions performed by the debugger



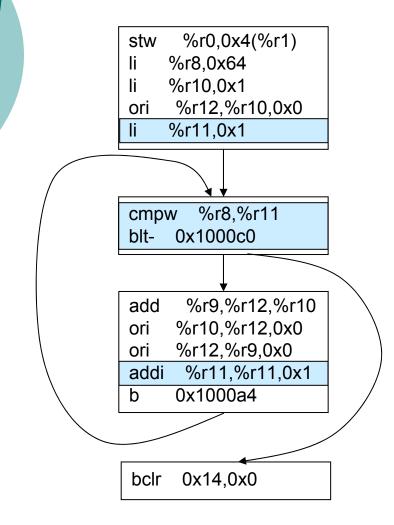
Contributions of RCGS

• Reverse execution along a dynamic slice

- Faster reverse execution
- No complete execution trajectory is required
 - Less runtime memory usage
- Not only reveals dynamic slice instructions but also obtains runtime values of variables
 - More efficient debugging

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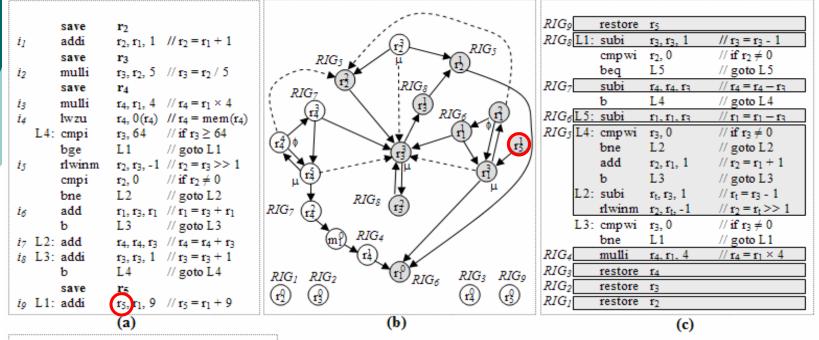
Reverse Execution Along a Dynamic Slice

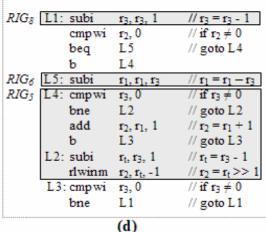


- Determine data dependencies statically
- Determine control flow dynamically
- Merge static information with dynamic information to reverse execute along the dynamic slice

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Generation of a Reduced Reverse Program

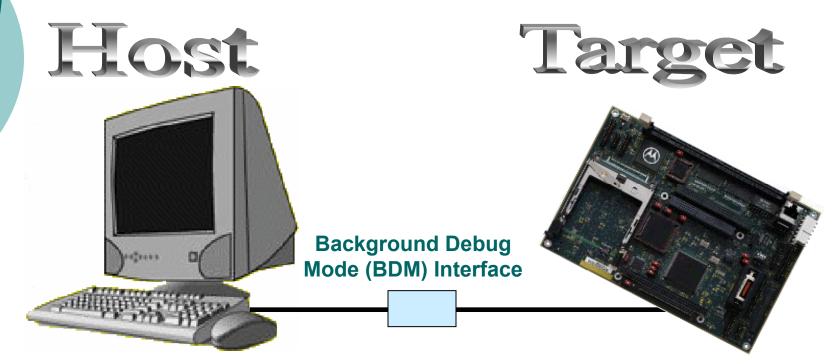




- (a): original program
- (b): corresponding MVG
- (c): reverse program
- (d): reduced reverse program



Experimentation Platform



PC

Windows 2000

MBX860

MPC860 processor 4MB DRAM, 2MB Flash RTC, four 16-bit timers, watchdog



Comparisons

- Reverse Execution with Incremental State Saving (ISS)
 - Save state before each instruction
- Reverse Execution with Incremental State Saving for Destructive Instructions (ISSDI)
 - Save state before each destructive instruction
- Reverse Execution with RCG



Benchmarks

Benchmark	Executable object size (bytes)
Selection sort	3104
Matrix multiply	3308
ADPCM encoder	6908
LZW	4636

ADPCM: Adaptive Differential Pulse Code Modulation

LZW: Lempel Ziv Welch

Benchmarks

Benchmark	Raw Execution Time (decrementer ticks)
Selection sort (100 inputs)	21,187
Selection sort (1000 inputs)	2,000,202
Selection sort (10000 inputs)	198,539,130
Matrix multiply (4x4)	650
Matrix multiply (40x40)	472,044
Matrix multiply (400x400)	457,183,831
ADPCM (32KB input data)	378,294
ADPCM (64KB input data)	751,280
ADPCM (128KB input data)	1,496,649
LZW (1KB input data)	1,380,413
LZW (4KB input data)	16,063,096
LZW (16KB input data)	194,451,339

1 tick = 0.4 microseconds on MBX860



- Instrument each benchmark with state saving instructions at appropriate points for ISS, ISSDI and RCG
- Forward execute each instrumented benchmark from the beginning until the end
- Measure forward execution times



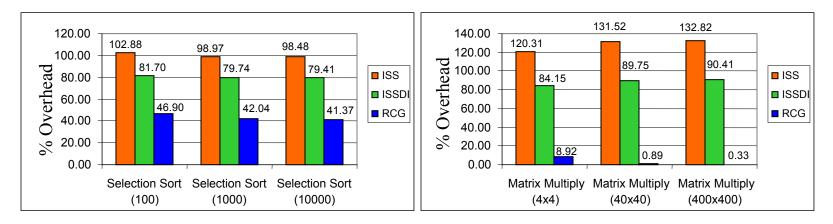
Instrumented Forward Execution Time

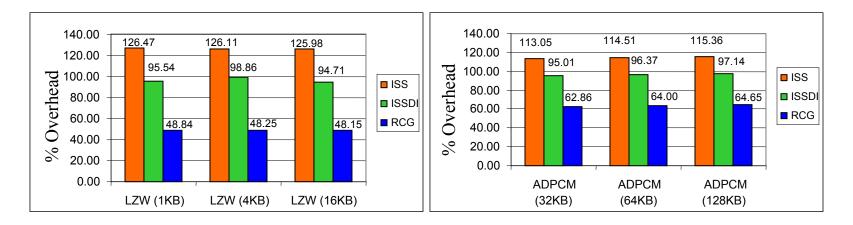
Benchmark	ISS	ISSDI	RCG	ISS/ RCG	ISSDI/ RCG
Selection sort (100 inputs)	42984	38496	31113	1.38X	1.24X
Selection sort (1000 inputs)	3979802	3595213	2841029	1.40X	1.27X
Selection sort (10000 inputs)	394063091	356208073	280677488	1.40X	1.27X
Matrix multiply (4x4)	1432	1197	708	2.02X	1.70X
Matrix multiply (40x40)	1092872	895703	476243	2.29X	1.88X
Matrix multiply (400x400)	1064415269	870539981	458691637	2.32X	1.90X
ADPCM (32KB input data)	805972	737720	616101	1.31X	1.20X
ADPCM (64KB input data)	1611572	1475276	1232110	1.31X	1.20X
ADPCM (128KB input data)	3223166	2950562	2464232	1.31X	1.20X
LZW (1KB input data)	3126206	2699287	2054657	1.52X	1.31X
LZW (4KB input data)	36319691	31942838	23813230	1.52X	1.34X
LZW (16KB input data)	439424024	378614957	288077045	1.53X	1.31X

ISS: Incremental State Saving, ISSDI: Incremental State Saving for Destructive Instructions



Forward Execution Time Overhead





Overhead = <u>instrumented execution time – raw execution time</u> raw execution time



 Reverse execute each benchmark from the end until the beginning (by executing the reverse versions)

• Measure reverse execution times



Reverse Execution Time

Benchmark	ISS	ISSDI	RCG	ISS/ RCG	ISSDI/ RCG
Selection sort (100 inputs)	28724	27137	36719	0.78X	0.74X
Selection sort (1000 inputs)	-	-	3516414	-	-
Selection sort (10000 inputs)	-	-	-	-	-
Matrix multiply (4x4)	880	784	1325	0.66X	0.60X
Matrix multiply (40x40)	660189	578556	1088827	0.61X	0.53X
Matrix multiply (400x400)	-	_	1070219421	-	-
ADPCM (32KB input data)	656702	628958	765036	0.86X	0.82X
ADPCM (64KB input data)	-	1257770	1528807	-	0.82X
ADPCM (128KB input data)	-	_	3057176	-	-
LZW (1KB input data)	-	-	2619106	-	-
LZW (4KB input data)	-	-	30596864	-	-
LZW (16KB input data)	-	-	371045637	-	-



 Forward execute each instrumented benchmark from the beginning until the end

 Measure memory usage for state saving



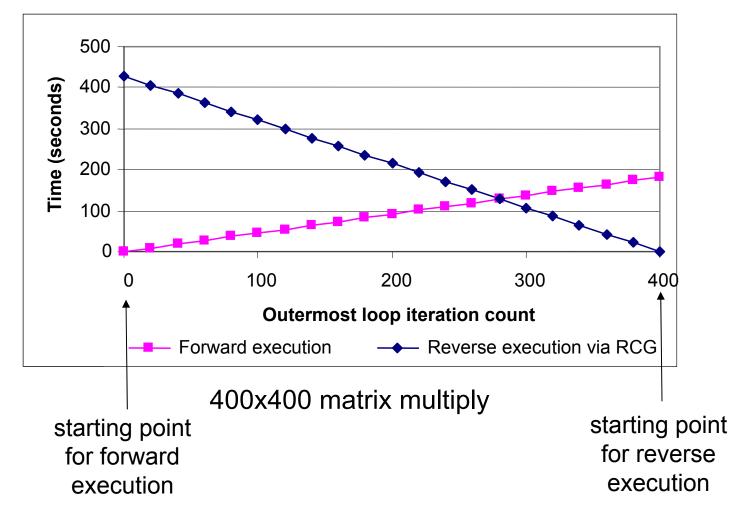
Memory Usage for State Saving

	ISS (KB)	ISSDI (KB)	RCG (KB)	ISS / RCG	ISSDI / RCG
Selection sort (100 inputs)	68.2	46.9	7.5	9X	6.3X
Selection sort (1000 inputs)	6032	4065	151	40X	27X
Selection sort (10000 inputs)	593389	397913	7237	82X	55X
Matrix multiply (4x4)	3.6	2.35	0.17	21X	14X
Matrix multiply (40x40)	2820	1801	12.6	224X	143X
Matrix multiply (400x400)	2756883	1755006	1250	2206X	1404X
ADPCM (32KB input data)	1544	1192	616	2.5X	2X
ADPCM (64KB input data)	3088	2384	1232	2.5X	2X
ADPCM (128KB input data)	6175	4767	2464	2.5X	2X
LZW (1KB input data)	5630	3425	98.4	57X	35X
LZW (4KB input data)	64970	39163	351	185X	112X
LZW (16KB input data)	784336	471140	1331	589X	354X



- Forward execute original 400x400 matrix multiply from the beginning to various intermediate points and measure the execution times
- Reverse execute 400x400 matrix multiply using RCG from the end to various intermediate points and measure reverse execution times

Program Re-execute Approach vs. RCG

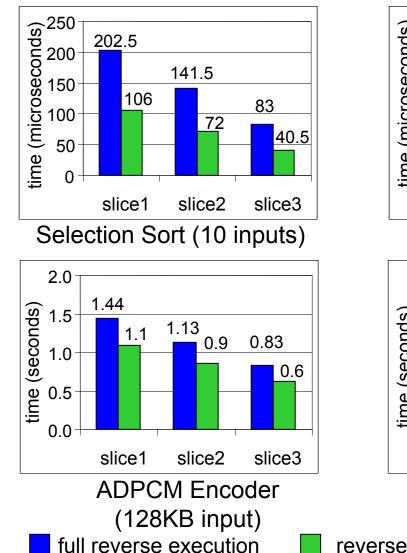


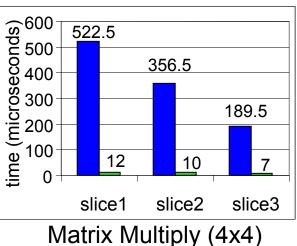
Geora

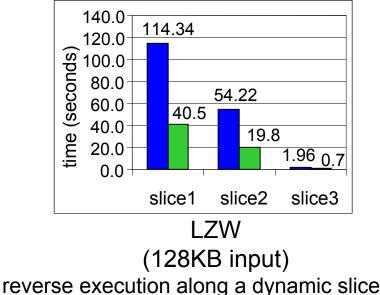


- Extract three slices for each benchmark
- Reverse execute each benchmark fully starting from end of each slice until beginning of each slice
- Reverse execute each benchmark along computed slices only
- Measure the reverse execution times

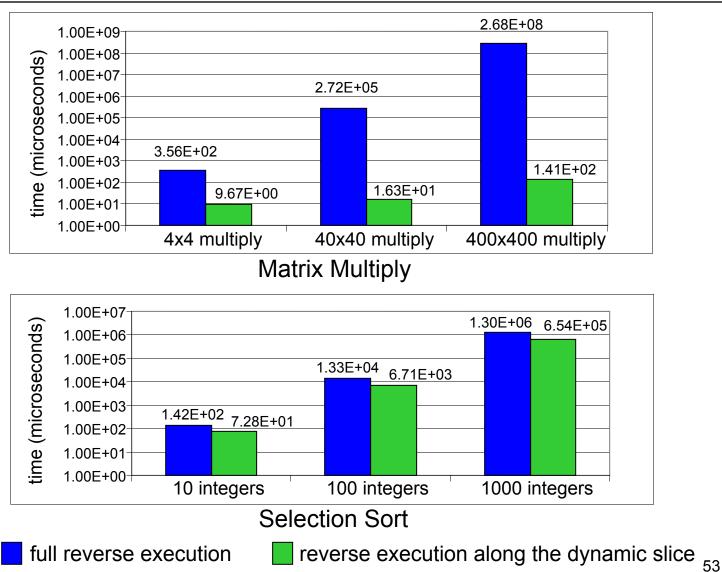
Full-scale Reverse Execution vs. Reverse Execution Along a Slice







Full-scale Reverse Execution vs. **Reverse Execution Along a Slice**

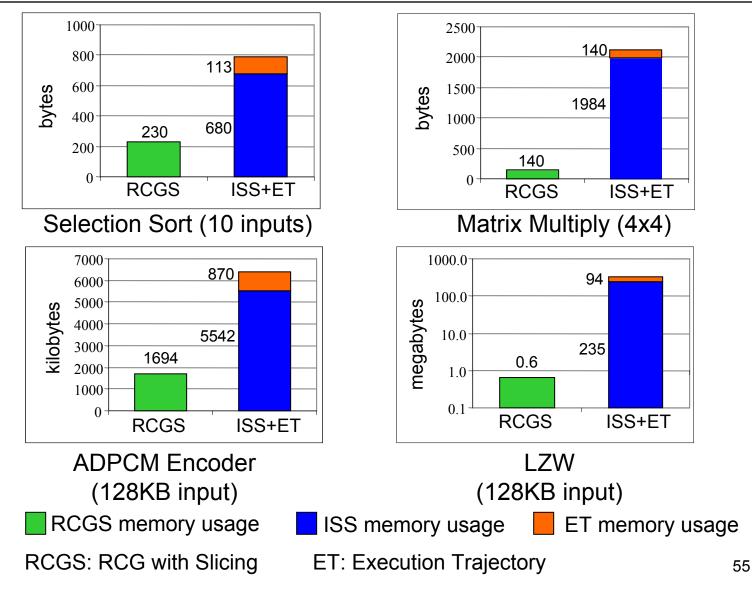




- Extract three slices for each benchmark
- Measure average runtime memory requirement for reverse execution along three slices with RCGS
- Measure average runtime memory requirement for reverse execution along three slices with ISS plus execution trajectory (ET) approach

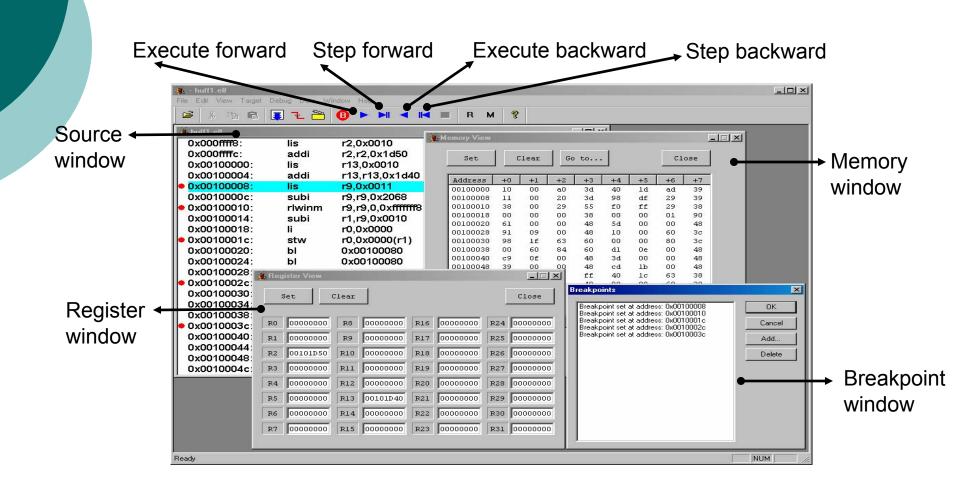


Runtime Memory Requirements





Reverse Debugger





Reverse Debugger

Reverse Debugger Code Specs				
Number of C lines	~7000			
Number of files	19			



Conclusion

- Reduced debugging time with localized reexecutions
- Very low time and memory overheads in forward execution by using reverse code
- Reverse execution up to an assembly instruction level granularity
- Dynamic slicing support to speed up reverse execution without execution trajectory requirement



Publications

- T. Akgul, V. J. Mooney and S. Pande, "A Fast Assembly Level Reverse Execution Method via Dynamic Slicing," accepted for publication in Proceedings of the 26th International Conference on Software Engineering (ICSE'04), May 2004.
- T. Akgul and V. J. Mooney, "Assembly Instruction Level Reverse Execution for Debugging," submitted to *Transactions on Software Engineering and Methodology (TOSEM)* on December 2002, accepted with minor revision.
- T. Akgul and V. J. Mooney, "Instruction-level Reverse Execution for Debugging," *Proceedings of the Workshop on Program Analysis for Software Tools and Engineering (PASTE'02)*, pp. 18-25, November 2002.
- T. Akgul and V. J. Mooney, "Instruction-level Reverse Execution for Debugging," *Technical Report GIT-CC-02-49*, September 2002. http://codesign.ece.gatech.edu/publications/index.htm
- T. Akgul, P. Kuacharoen, V. Mooney and V. Madisetti, "A Debugger RTOS for Embedded Systems," *Proceedings of the 27th EUROMICRO Conference* (EUROMICRO'01), pp. 264-269, September 2001.
- P. Kuacharoen, T. Akgul, V. Mooney and V. Madisetti, "Adaptability, Extensibility, and Flexibility in Real-Time Operating Systems," *Proceedings of the EUROMICRO Symposium on Digital Systems Design* (EUROMICRO'01), pp. 400-405, September 2001.
- T. Akgul, P. Kuacharoen, V. J. Mooney and V. K. Madisetti, "A Debugger Operating System for Embedded Systems," U.S. Patent Application, no. 20030074650, April 17, 2003.
- P. Kuacharoen, T. Akgul, V. J. Mooney and V. K. Madisetti, "A Dynamic Operating System," U.S. Patent Application, no. 20030074487, April 17, 2003 59



Thank you!