"Rules" for identifying the type of feedback

1.) Identify the loop.

This helps you see where the A network is and what is the B network.

2.) Input – series or shunt?

a.) Tests for shunt.

– If one of the two-input terminals on the "input transistor" (the transistor where the input signal is combined with the feedback signal) is on ac ground, the feedback shunt.

Can verify by writing $i_i = i_s - i_f$

– If neither the I or V terminal are on ac ground. Try to write the equation

$$i_i = i_s - i_f$$

b.) Tests for series –

If neither the I or V terminal is on ac ground, then the circuit is series

if $v_i = v_s - v_f$

3.) Output – series-shunt?

If one of the O or V terminals is on AC ground, the output must shunt fb.

If neither the O or V terminals are on AC ground, the feedback is

shunt if the x_{fb} variable $\to 0$ when $R_L \to 0$

series if the x_{fb} variable $\to 0$ when $R_L \to \infty$

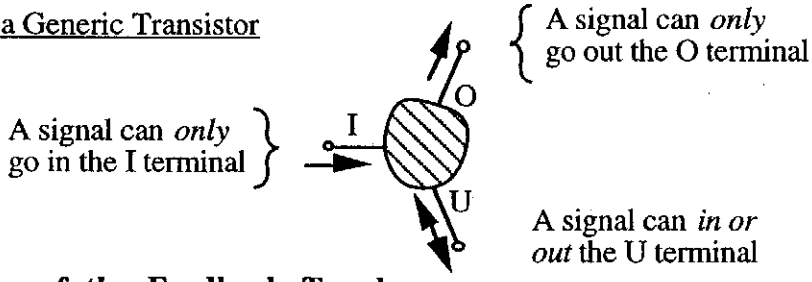
ANALYSIS OF TRANSISTOR FEEDBACK AMPLIFIERS

Steps In Analyzing Transistor Feedback Amplifiers

1. Identify the topology.
2. Determine whether the feedback is positive or negative.
3. Open the loop and calculate A, ß, R_i, and R_o.
4. Use the Table to find A_f, R_{if} and R_{of} or A_F, R_{iF}, and R_{oF}.
5. Use the information in 4.) to find whatever is required (v_{out}/v_{in}, R_{in}, R_{out}, etc.)

Generic Transistor Concept

Properties of a Generic Transistor

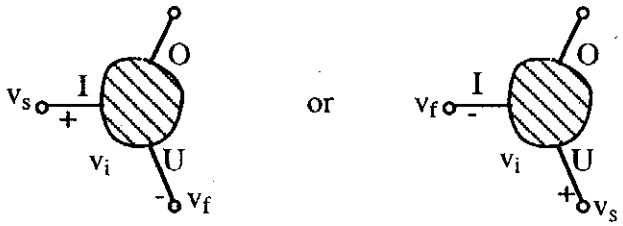


Identification of the Feedback Topology

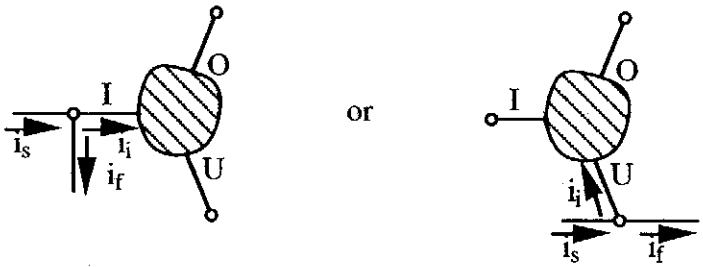
Isolate the input and output transistor(s) and apply the following identification.

Input

Series:

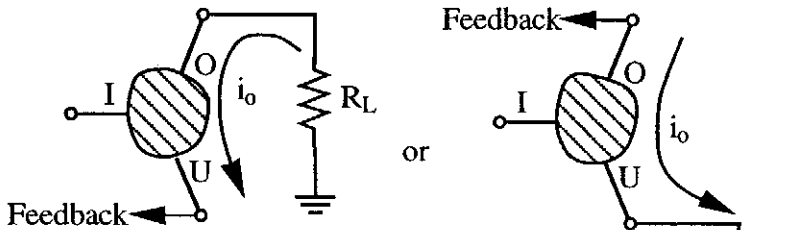


Shunt:

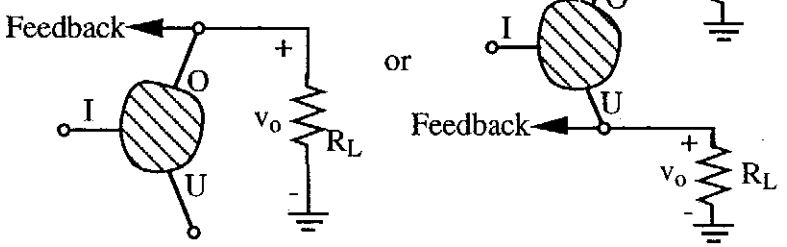


Output

Series:



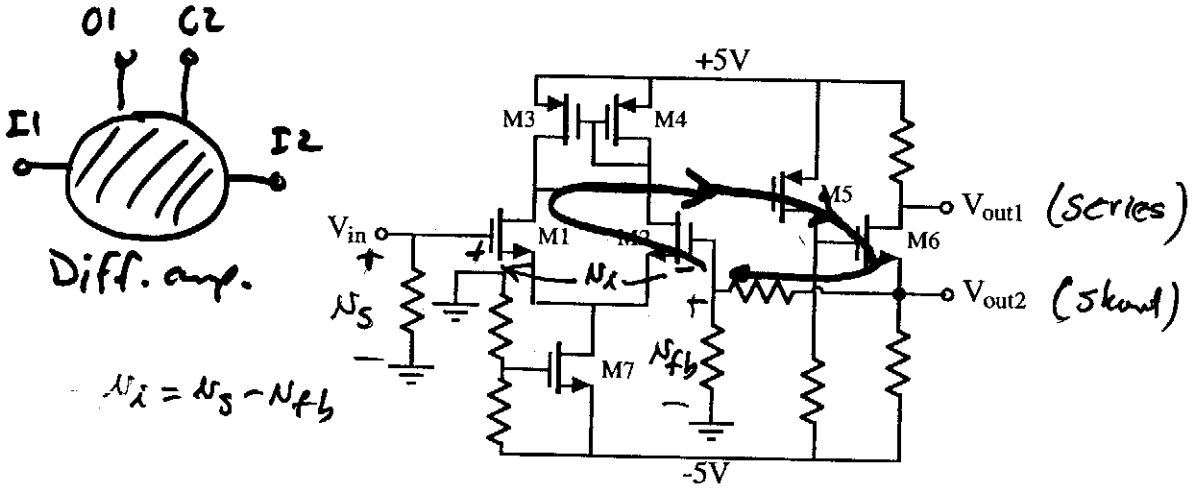
Shunt:



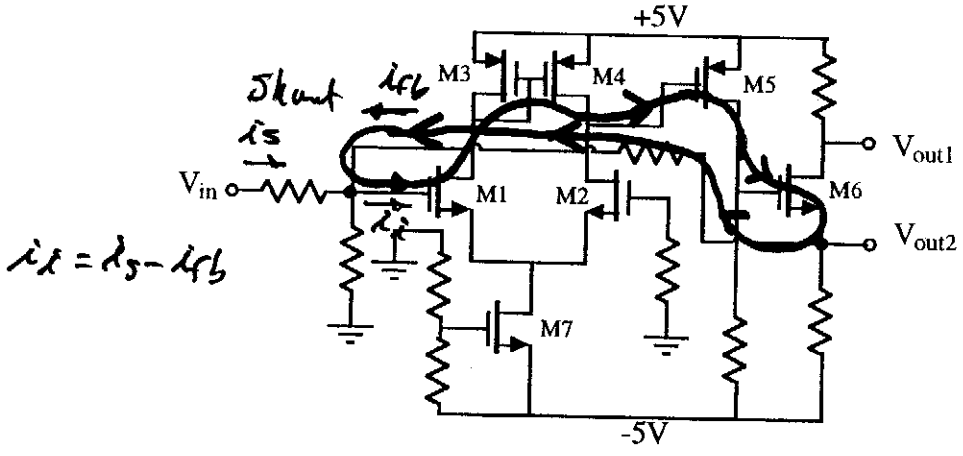
EXAMPLE OF FEEDBACK TOPOLOGY IDENTIFICATION

Use the rules of identifying feedback topologies to identify the four different topologies for the circuits shown below.

Circuits 1 and 2



Circuits 3 and 4



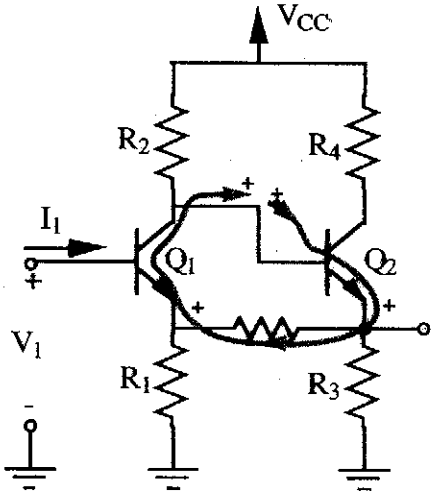
RULES FOR IDENTIFYING POSITIVE AND NEGATIVE FEEDBACK

1. Identify the feedback loop by tracing its path on the diagram. If there are alternate paths, always choose the path with the highest loop gain. (Remember that a signal can go in the "I" or "U" terminal of a transistor and can only come out the "O" or "U" terminal.)

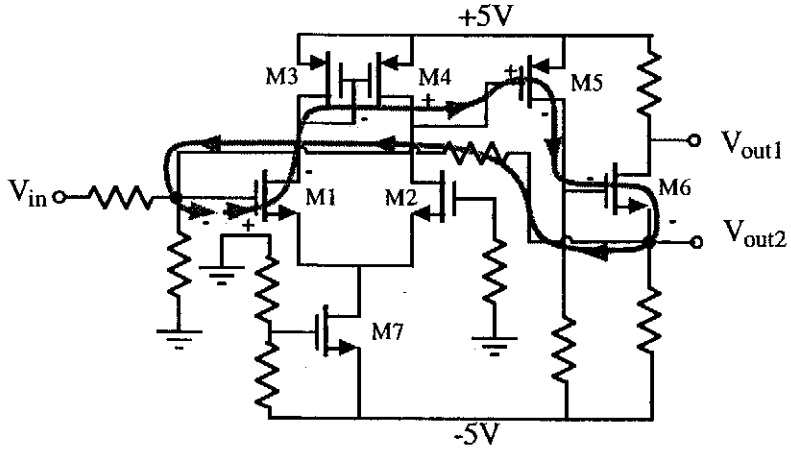
2. At any point on the feedback loop, assume the signal is positive and put a "+" mark at that point. Trace the signal around the loop remembering that the signal only inverts when it goes in a "I" terminal and out the "O" terminal of a transistor. All other paths through a transistor do not invert (i.e., "I" to "U" and "U" to "O").

3. When you have traced the polarity of the signal around the feedback loop back to the point where you placed the "+", the feedback is negative if the signal polarity is "-" and positive if the signal polarity is "+".

Example 1



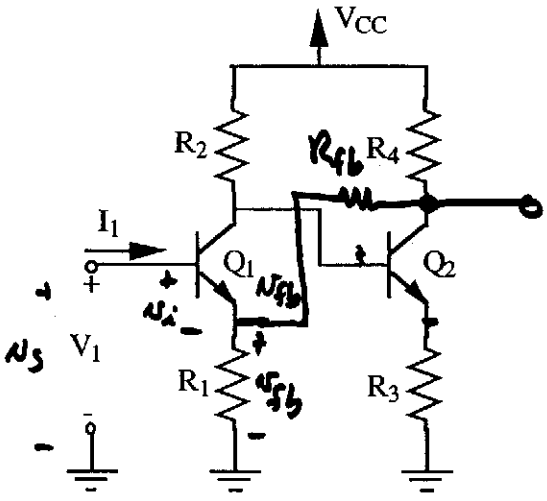
Example 2



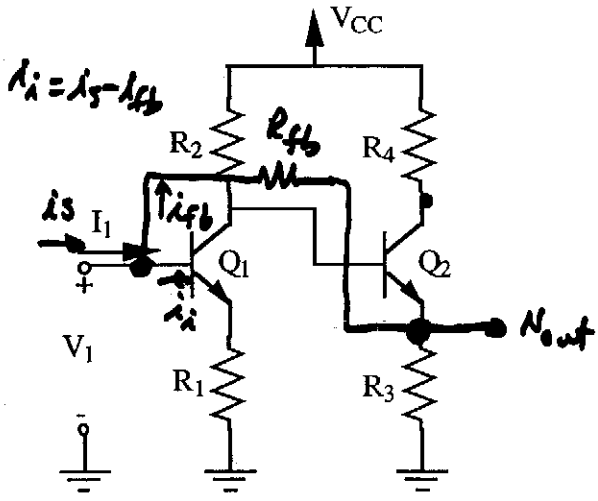
EXAMPLE OF FEEDBACK TOPOLOGY IDENTIFICATION

Use the rules of identifying feedback topologies to create the four different negative feedback topologies using the identical starting structure.

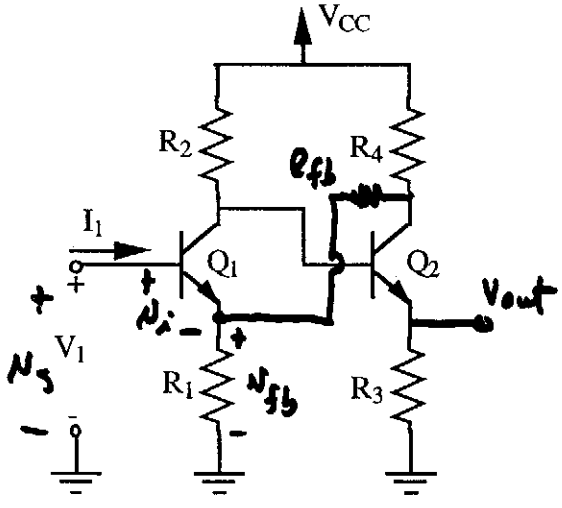
1. Voltage-Voltage (Series-Shunt)



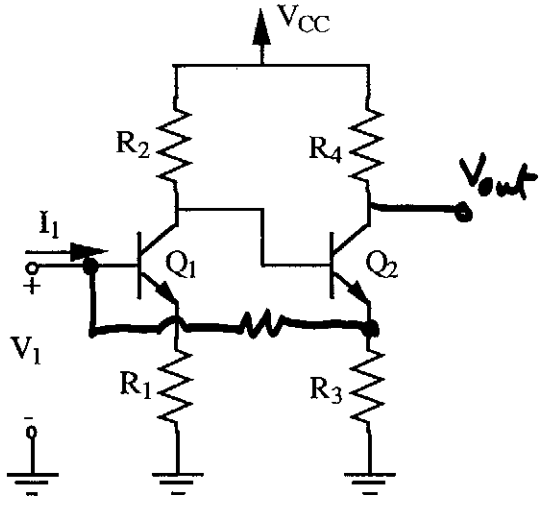
2. Current-Voltage (Shunt-Shunt)



3. Voltage-Current (Series-Series)

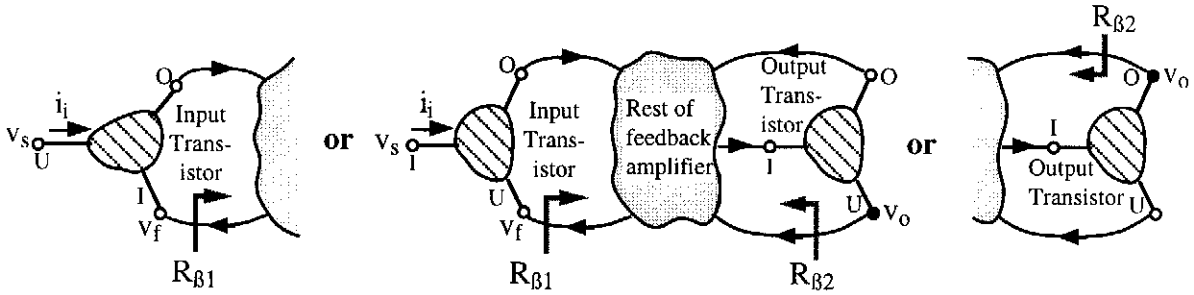


4. Current-Current (Shunt-Series)



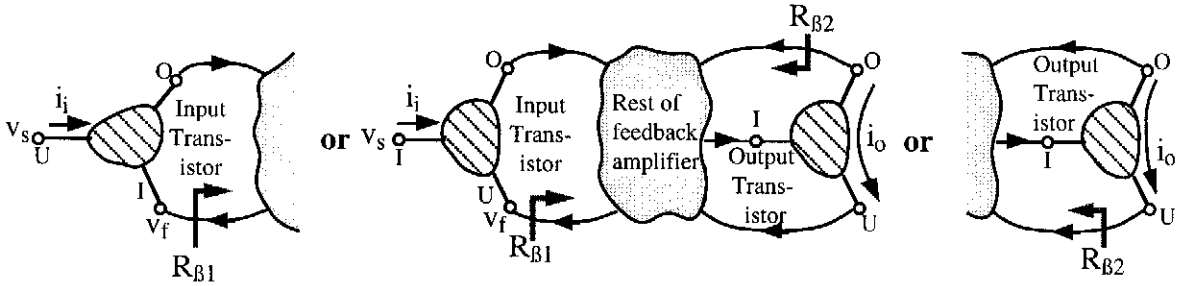
RULES FOR ANALYSIS OF TRANSISTOR FEEDBACK AMPLIFIERS

Series-Shunt



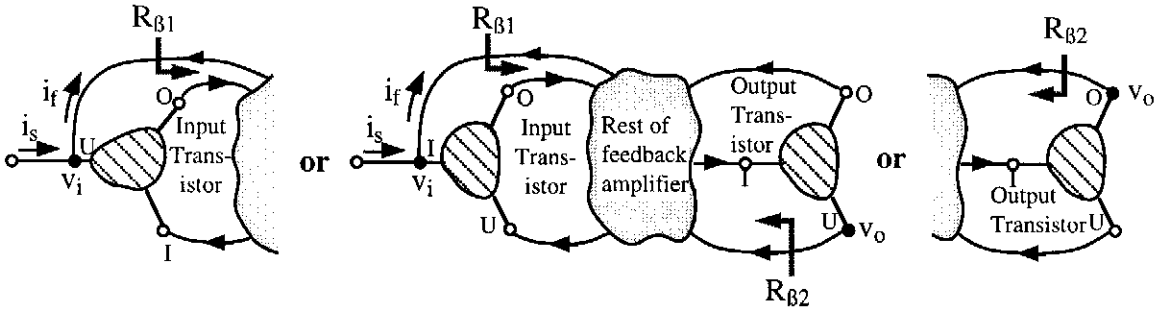
$R_{\beta 1}$ = Resistance seen looking out the I or U terminal of the input transistor with $v_o = 0$.
$R_{\beta 2}$ = Resistance seen looking out the O or U terminal of the output transistor with $i_i = 0$.

Series-Series



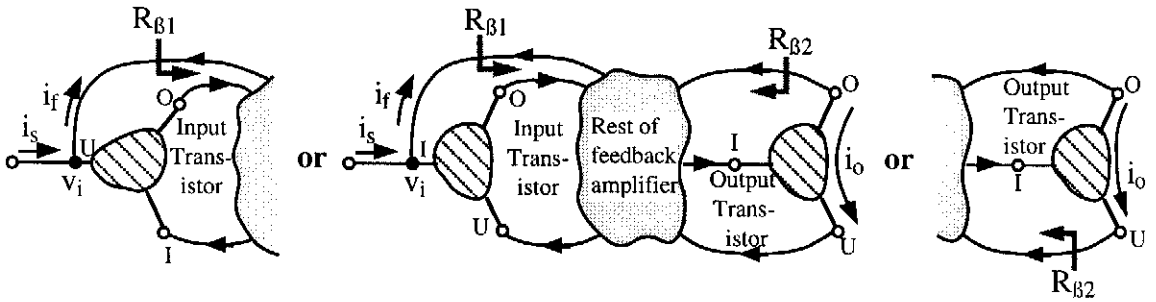
$R_{\beta 1}$ = Resistance seen looking out the I or U terminal of the input transistor with $i_o = 0$.
$R_{\beta 2}$ = Resistance seen looking out the O or U terminal of the output transistor with $i_i = 0$.

Shunt-Shunt



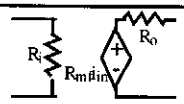
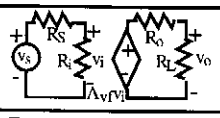
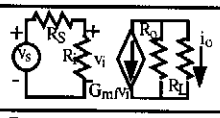
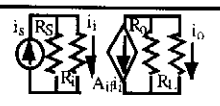
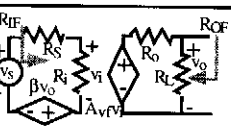
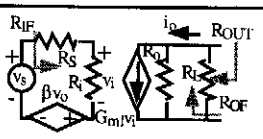
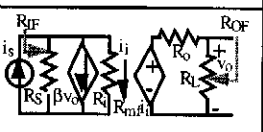
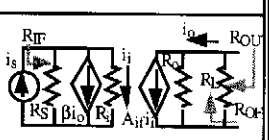
$R_{\beta 1}$ = Resistance seen looking out the I or U terminal of the input transistor with $v_o = 0$.
$R_{\beta 2}$ = Resistance seen looking out the O or U terminal of the output transistor with $v_i = 0$.

Shunt-Series



$R_{\beta 1}$ = Resistance seen looking out the I or U terminal of the input transistor with $i_o = 0$.
$R_{\beta 2}$ = Resistance seen looking out the O or U terminal of the output transistor with $v_i = 0$.

Summary of the Important Relationships of Open-loop and Closed-loop Feedback Amplifiers.

Quantity	Voltage Amplifier	Transconductance Amplifier	Transresistance Amplifier	Current Amplifier
Input-output variable	Voltage-voltage	Voltage-current	Current-voltage	Current-current
Small Signal Model				
Small Signal Amplifier with Source & Load				
Ideal R_S	$R_S = 0$ or $R_S \ll R_i$	$R_S = 0$ or $R_S \ll R_i$	$R_S = \infty$ or $R_S \gg R_i$	$R_S = \infty$ or $R_S \gg R_i$
Ideal R_L	$R_L = \infty$ or $R_L \gg R_o$	$R_L = 0$ or $R_L \ll R_o$	$R_L = \infty$ or $R_L \gg R_o$	$R_L = 0$ or $R_L \ll R_o$
Overall Forward Gain	$A_V = \dfrac{R_i R_L A_{vf}}{(R_S+R_i)(R_L+R_o)}$	$G_M = \dfrac{R_i R_o G_{mf}}{(R_S+Ri)(R_L+R_o)}$	$R_M = \dfrac{R_S R_L R_{mf}}{(R_S+Ri)(R_L+R_o)}$	$A_I = \dfrac{R_S R_o A_{if}}{(R_S+Ri)(R_L+R_o)}$
Feedback Topology	Series-shunt	Series-series	Shunt-shunt	Shunt-series
Ideal ß, finite R_S and R_L Feedback Small Signal Models				
Closed-Loop Gain (Ideal R_S and R_L)	$A_{VF} = \dfrac{A_{vf}}{(1+A_{vf}\beta_v)}$	$G_{mF} = \dfrac{G_{mf}}{(1+G_{mf}\beta_g)}$	$R_{mF} = \dfrac{R_{mf}}{(1+R_{mf}\beta_r)}$	$A_{iF} = \dfrac{A_{if}}{(1+A_{if}\beta_i)}$
Closed-Loop Input Resistance (Ideal R_S and R_L)	$R_{iF} = R_i(1 + A_{vf}\beta_v)$	$R_{iF} = R_i(1 + G_{mf}\beta_g)$	$R_{iF} = \dfrac{R_i}{1 + R_{mf}\beta_r}$	$R_{iF} = \dfrac{R_i}{1 + A_{if}\beta_i}$
Closed-Loop Output Resistance (Ideal R_S and R_L)	$R_{oF} = \dfrac{R_o}{1 + A_{vf}\beta_v}$	$R_{oF} = R_o(1 + R_{mf}\beta_g)$	$R_{oF} = \dfrac{R_o}{1 + R_{mf}\beta_r}$	$R_{oF} = R_o(1 + A_{if}\beta_i)$
Closed-Loop Gain	$A_{VF} = \dfrac{A_V}{(1+A_V\beta_v)}$	$G_{MF} = \dfrac{G_M}{(1+G_M\beta_g)}$	$R_{MF} = \dfrac{R_M}{(1+R_M\beta_r)}$	$A_{IF} = \dfrac{A_I}{(1+A_I\beta_i)}$
Closed-Loop Input Resistance	$R_{IF} = (R_i+R_S)(1+A_V\beta_v)$	$R_{IF} = (R_i+R_S)(1 + G_M\beta_g)$	$R_{IF} = \dfrac{\frac{R_iR_S}{R_i+R_S}}{1 + R_M\beta_r}$	$R_{IF} = \dfrac{\frac{R_iR_S}{R_i+R_S}}{1 + A_I\beta_i}$
Closed-Loop Output Resistance	$R_{OF} = \dfrac{\frac{R_oR_L}{R_o+R_L}}{1 + A_V\beta_v}$	$R_{OF} = (R_o+R_L)(1+G_M\beta_g)$	$R_{OF} = \dfrac{\frac{R_oR_L}{R_o+R_L}}{1 + R_M\beta_r}$	$R_{OF} = (R_o+R_L)(1+A_I\beta_i)$
Output Resistance of Series Output Fb. Ckt	$R_{OUT} = R_{OF}$	$R_{OUT} = \dfrac{R_L}{R_{OF}}(R_{OF}-R_L)$	$R_{OUT} = R_{OF}$	$R_{OUT} = \dfrac{R_L}{R_{OF}}(R_{OF}-R_L)$