Lecture 12

Physical Vapor Deposition: Evaporation and Sputtering

Reading:

Chapter 12

Evaporation

Evaporation and Sputtering (Metalization)

For all devices, there is a need to go from semiconductor to metal. Thus we need a means to deposit metals. Many of these techniques used for metal deposition can be used to deposit other materials as well.

Several methods are currently used for deposition of metal layers.

Physical Vapor Deposition techniques (PVD)

1.) Evaporation
2.) Sputtering
3.) Chemical Vapor Deposition (CVD)
4.) Electrochemical techniques

1.) Evaporation:

Advantages: Highest purity (Good for Schottky contacts) due to low pressures.

Disadvantages: Poor step coverage, forming alloys can be difficult, lower throughput due to low vacuum.

Evaporation is based on the concept that there exists a finite "vapor pressure" above any material. The material either sublimes (direct solid to vapor transition) or evaporates (liquid to vapor transition).

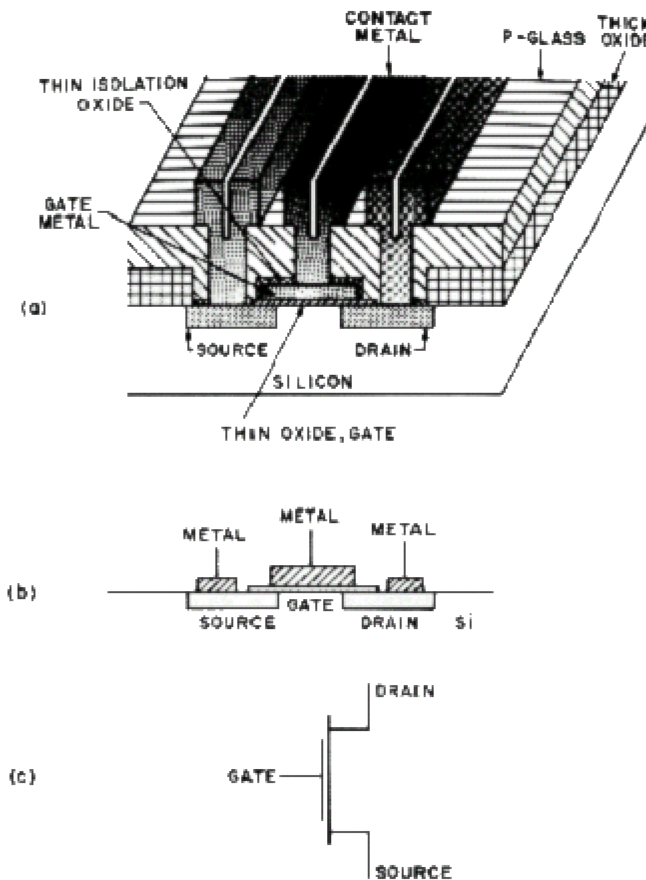


FIGURE 1
A typical MOSFET in (a) cross section, (b) a simple schematic representation, and (c) a designer's symbolic representation.

Evaporator Systems

Two main types of evaporators: E-beam and filament.

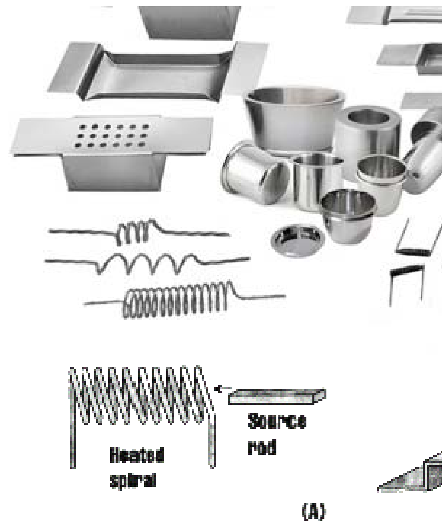
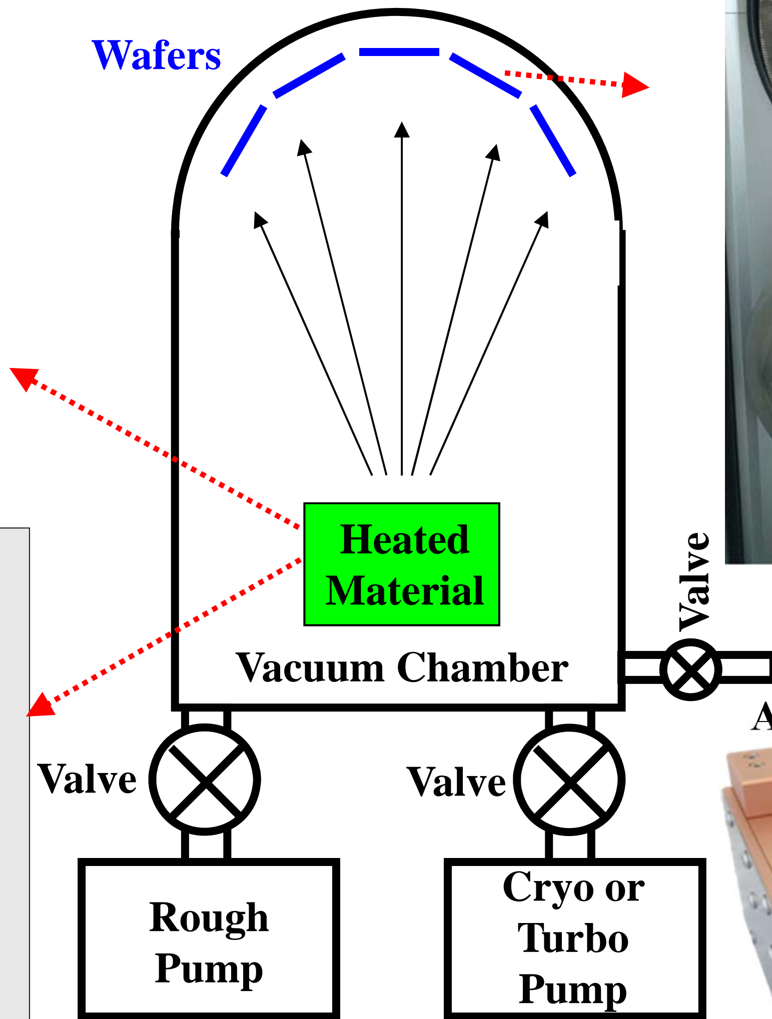
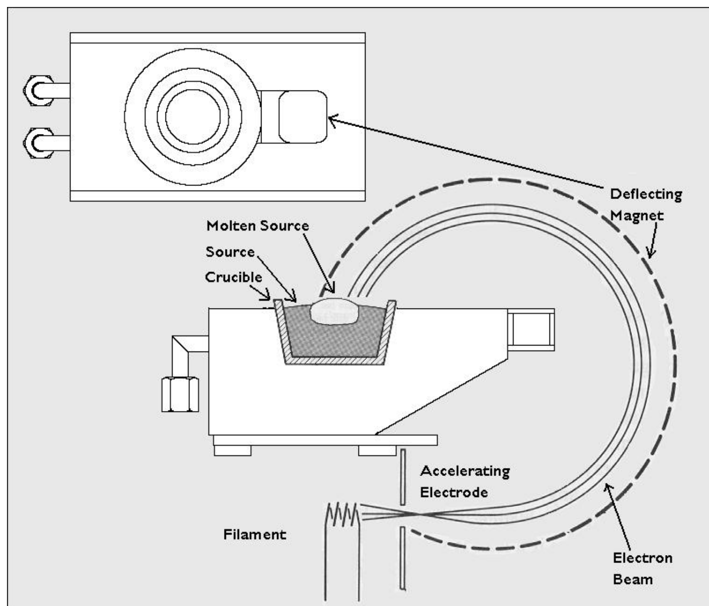


Figure 12-6 Resistive evaporator sources. (a) Simple sources including heating the charge itself and using a coil of refractory metal heater coil and a charge rod. (b) More standard thermal sources including a dimpled boat in a resistive media.





Evaporator Physics

For evaporation, the vapor pressure is,

$$P_{evaporation} = 3x10^{12}\sigma^{3/2}T^{-1/2}e^{\left(\frac{\Delta H}{NkT}\right)} \approx P_o e^{\left(\frac{Ea}{kT}\right)}$$

where σ is the surface tension of the liquid, N is avagadro's number, and ΔH is the enthalpy of evaporation (the energy required to convert from a liquid to gas phase).

We can define the number of molecules crossing a plane per unit time as,

$$J = \sqrt{\frac{P^2}{2\pi kTm}}$$

where P is pressure in Pascals, k is Boltzsmans constant, T is absolute temperature and m is the atomic or molecular mass.

If the liquid is assumed to be at a constant temperature, and the crucible (container holding the liquid) has a constant area opening, the wafer is located on a sphere as defined by figure 12-3, the the deposition rate is,

$$R_d = \sqrt{\frac{m}{2\pi k\rho^2}}\frac{P_{evaporation}}{\sqrt{T}}\frac{Area}{4\pi r^2}$$

where ρ is the mass density (kg/m^2), Area is the area of the wafer, and r is the radius of the sphere defined in figure 12-3.

Virtual Source: Point in free space where the pressure drops enough to result in molecular flow. Closer to the source viscous flow applies.

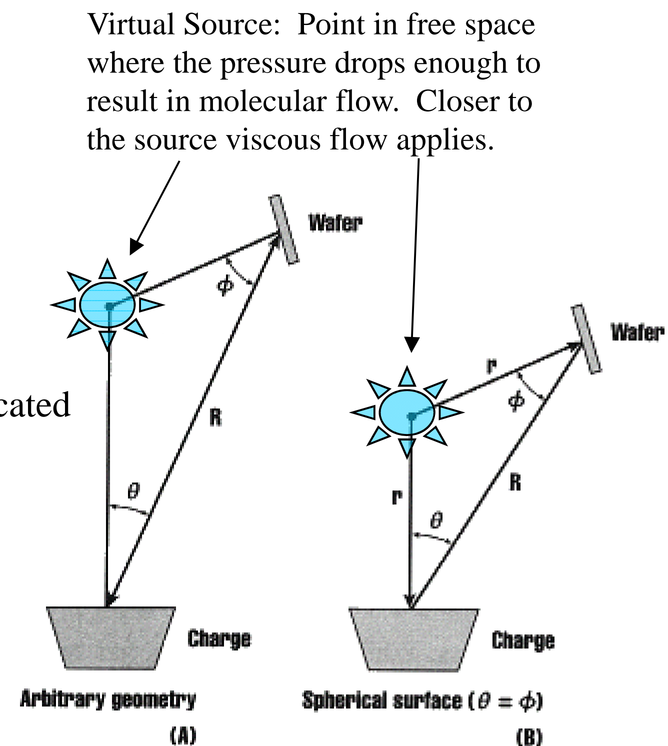


Figure 12-3 The geometry of deposition for a wafer (a) in an arbitrary position and (b) on the surface of a sphere.

Evaporation Step Coverage

The step coverage of evaporated films is poor due to the directional nature of the evaporated material (shadowing) (see figure 12-5). Heating (resulting in surface diffusion) and rotating the substrates (minimizing the shadowing) help with the step coverage problem, but evaporation can not form continuous films for high aspect ratios (AR=step height/step width or diameter) greater than 1.

We need a less directional metallization scheme====> Higher pressures!

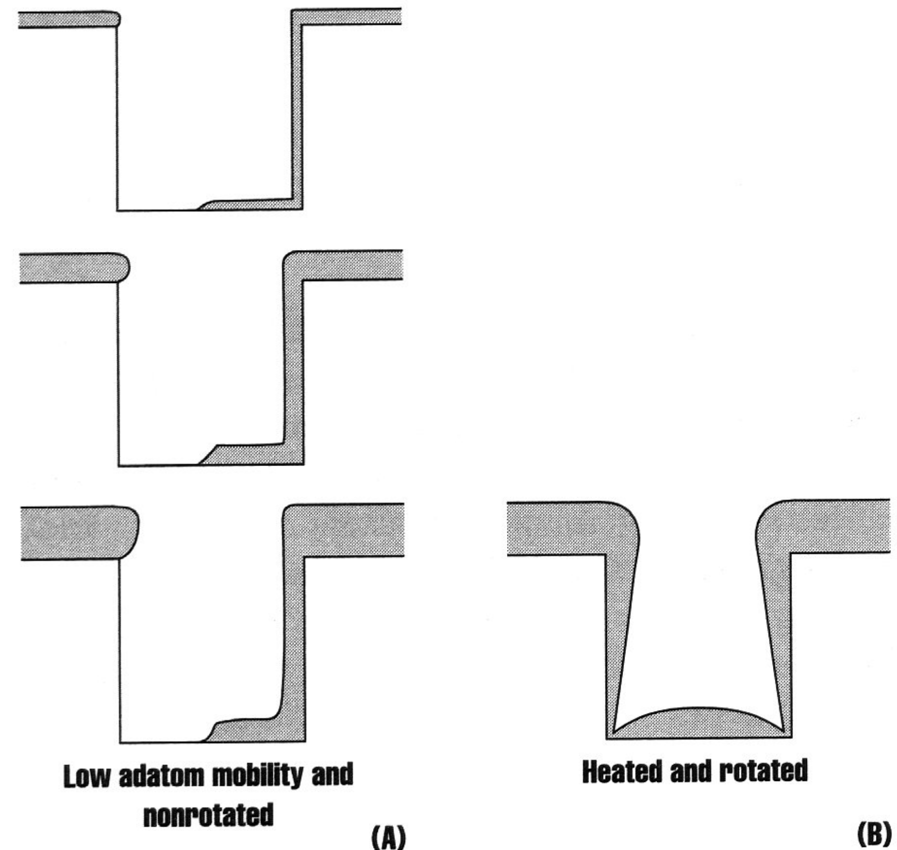


Figure 12-5 (a) Time evolution of the evaporative coating of a feature with aspect ratio of 1.0, with little surface atom mobility (i.e., low substrate temperature) and no rotation. (b) Final profile of deposition on rotated and heated substrates.

Sputtering

2.) Sputtering:

Advantages: Better step coverage, less radiation damage than E-beam evaporation, easier to deposit alloys.

Disadvantages: Some plasma damage including implanted argon. Good for ohmics, not Schottky diodes.

A plasma at higher pressure is used to "knock" metal atoms out of a "target". These energetic atoms deposit on a wafer located near the target. The higher pressure produces better step coverage due to more random angled delivery. The excess energy of the ions also aids in increasing the surface mobility (movement of atoms on the surface).

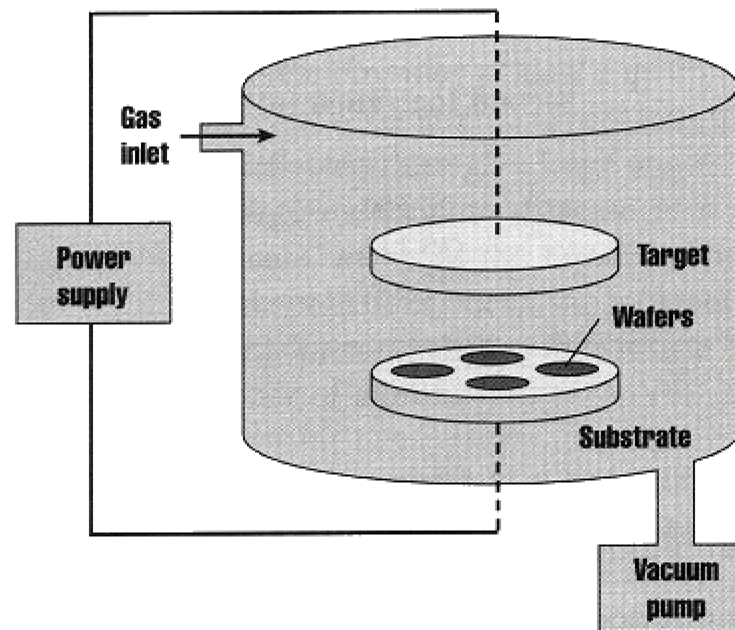


Figure 12-11 Chamber for a simple parallel plate sputtering system.

Sputtering

A threshold energy for the release of an atom from the target exists, below which the atom is not "sputtered".

This threshold energy is,

$$E_{threshold} = \frac{Heat\ of\ Vaporization}{\gamma(1-\gamma)} \quad where \quad \gamma = \frac{4M_1M_2}{(M_1+M_2)^2}$$

The sputter yield (ratio of target atoms expelled to incident atoms impinging on the target) increases with increasing energy (plasma power or DC bias). (See 12-13).

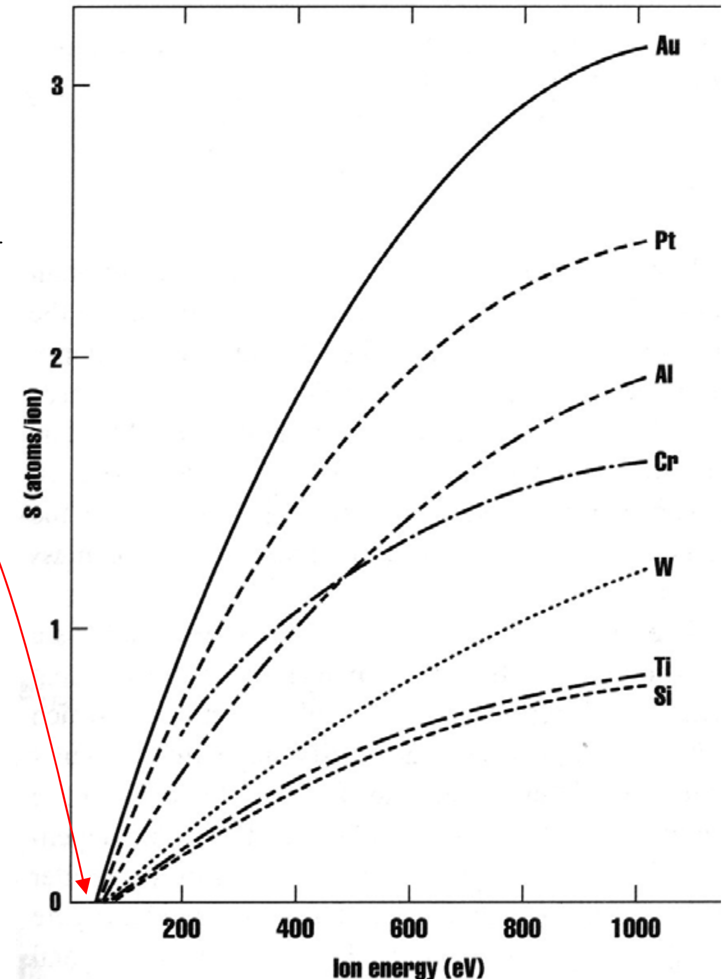


Figure 12-13 Sputter yield as a function of ion energy for normal incidence argon ions for a variety of material: *(after Anderson and Bay, reprinted by permission).*

Sputtering Details

Film Morphology

Deposited films can be: (See 12-20).

1.) Porous and/or Amorphous —> Results from poor surface mobility =low temperature, low ion energy (low RF power/DC bias or higher pressures=less acceleration between collisions).

2.) "T-zone": Small grain polycrystalline, dense, smooth and high reflectance (the sweet spot for most metal processes) Results from higher surface mobility =higher temperature or ion energy

3.) Further increases in surface mobility result in columnar grains that have rough surfaces. These rough surfaces lead to poor coverage in later steps.

4.) Still further increases in surface mobility result in large (non-columnar) grains. These grains can be good for diffusion barriers (less grain boundary diffusion due to fewer grains) but pose problems for lithography due to light scatter off of large grains, and tend to be more rigid leading to more failures in electrical lines.

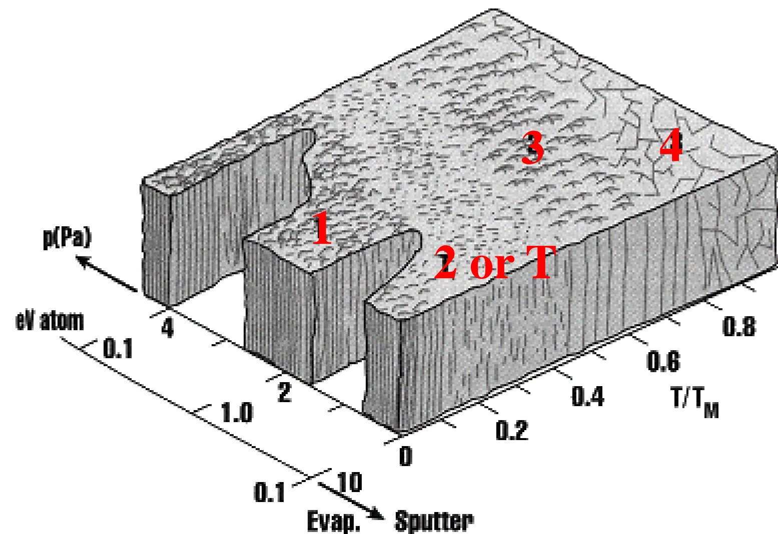


Figure 12-20 The three zone model of film deposition as proposed by Movchan and Demchishin *(after Thornton, reprinted by permission, AIP).*

Sputtering Details

Often, it is needed to sputter alloys instead of pure elemental metals (Al+Si+Cu). Consider the problem of electromigration in Aluminum

Causes:
Electron momentum transfer to the ions in high current density lines.
Solution: Add a small number (typically <3-5%) larger atoms such as copper that “anchor” the aluminum atoms in place or replace the entire metal line with larger atoms such as copper so that each atom is more difficult to move.

When sputtering Aluminum and Copper alloys, the film on the wafer has more copper than the target. Reason: At the target, the argon has achieved high enough energy to sputter the Al and Cu evenly. However, in the gas (lower electric field), the heavier atoms are less effected by light sputter gas. The light Al can gain enough energy to be above it’s evaporation temperature when it hits the wafer. Thus, the Cu sticks, but the Al does not.

The target material must be tailored to the sputter conditions to get the desired film composition!

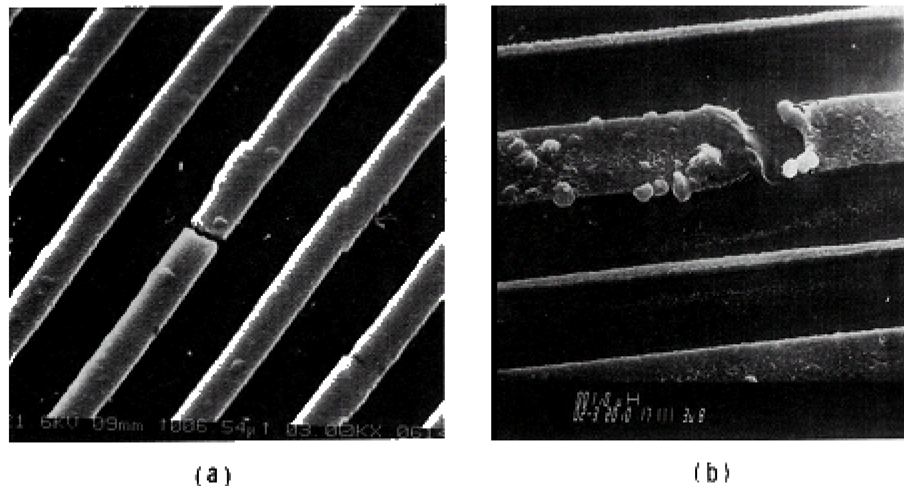


FIGURE 13
SEM micrographs of electromigration failure in aluminum runners. for (a) S-gun magnetron-deposited Al–0.5% Cu alloy and (b) In-source-evaporated Al–0.5% Cu alloy. (*From Vaidya, Fraser, and Sinha, Ref. 38.*)

Sputtering Details

Film stress:
Film stress can result in wafer bowing (problems with lithography), film cracking or peeling. There is 2 kinds of films stress:

1.) Extrinsic Stress (forces acting on the wafer due to sources external to the deposited film)
Example: Thermal induced stress:

$$Stress_{thermal\ mismatch} = \frac{Youngs\ Modulus\ of\ film}{1-(Poissons's\ Ratio\ of\ film)} \int_{T_{room}}^{T_{deposition}} (\alpha_{film} - \alpha_{wafer})dT$$

where α is the thermal expansion coefficient [1/degree].

2.) Intrinsic Stress (forces acting on the wafer due to sources internal to the deposited film)
These can be differences in atomic spacing, variations in grain orientation or size, grain growth during deposition, and even implanted or trapped gaseous impurities such as argon. These depend strongly on the deposition conditions.

Both of these stresses can lead to a bowed wafer with deflection δ defined in figure 12-28.

$$Stress = \frac{\delta E D^2}{t(1-\nu)3R^2}$$

Where E is the films Youngs modulus, ν is the films Poisson ratio, D is the wafer thickness, t is the film thickness, R is the radius of the wafer bow.

Figure 12-28 The change in wafer deflection may be used to measure the stress in a deposited layer. This is typically measured using a reflected laser beam.

Sputtering Details

Self Aligned Process

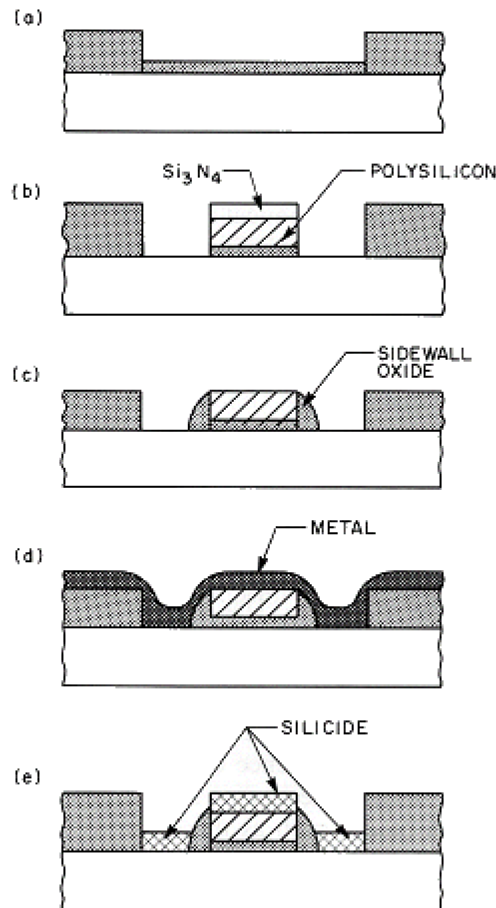
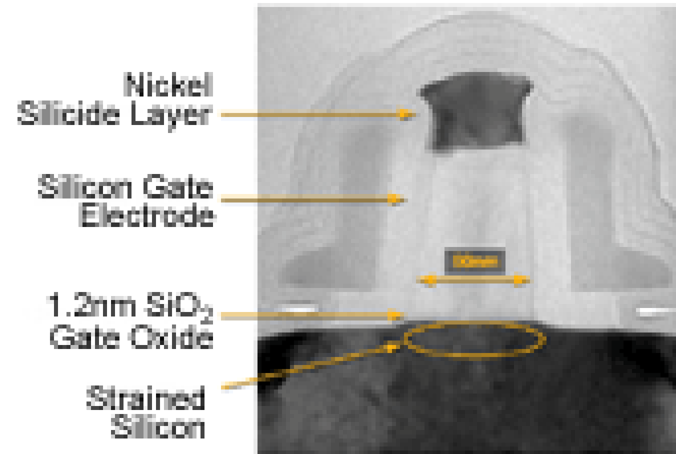


FIGURE 6
Showing process steps for self-aligned gate, source, and drain-silicide formation.

Self aligned Gate Process
See figure Sze 9-6



50nm transistor dimension is ~2000x smaller than diameter of human hair

The transistors implemented in Intel's new chip making process are the smallest ever to be designed into a commercial microprocessor, measuring on 50 nanometers. How small is that? You could fit hundreds of these transistors inside a red blood cell.

Sputtering Details

Multi-Level Metalization

Verbally Discuss Damascene with aid of Added Slides.

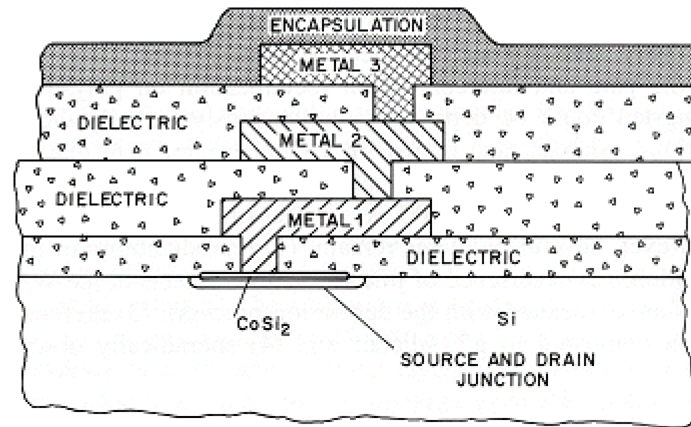
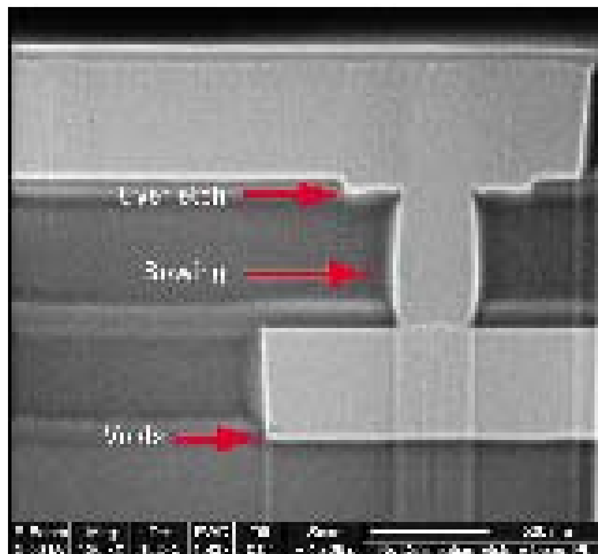
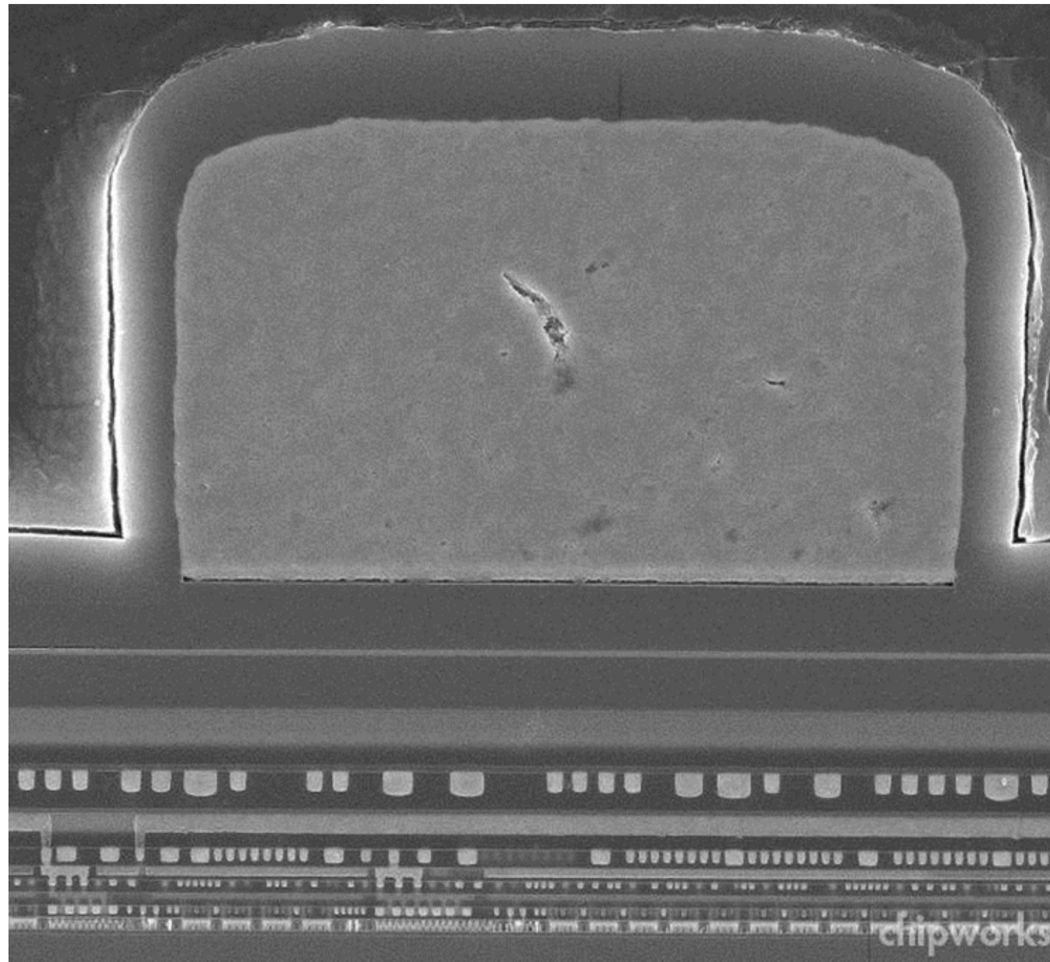


FIGURE 17
A schematic drawing of a multilevel metallization structure.



Multi-level Metallization
See figure Sze 9-17

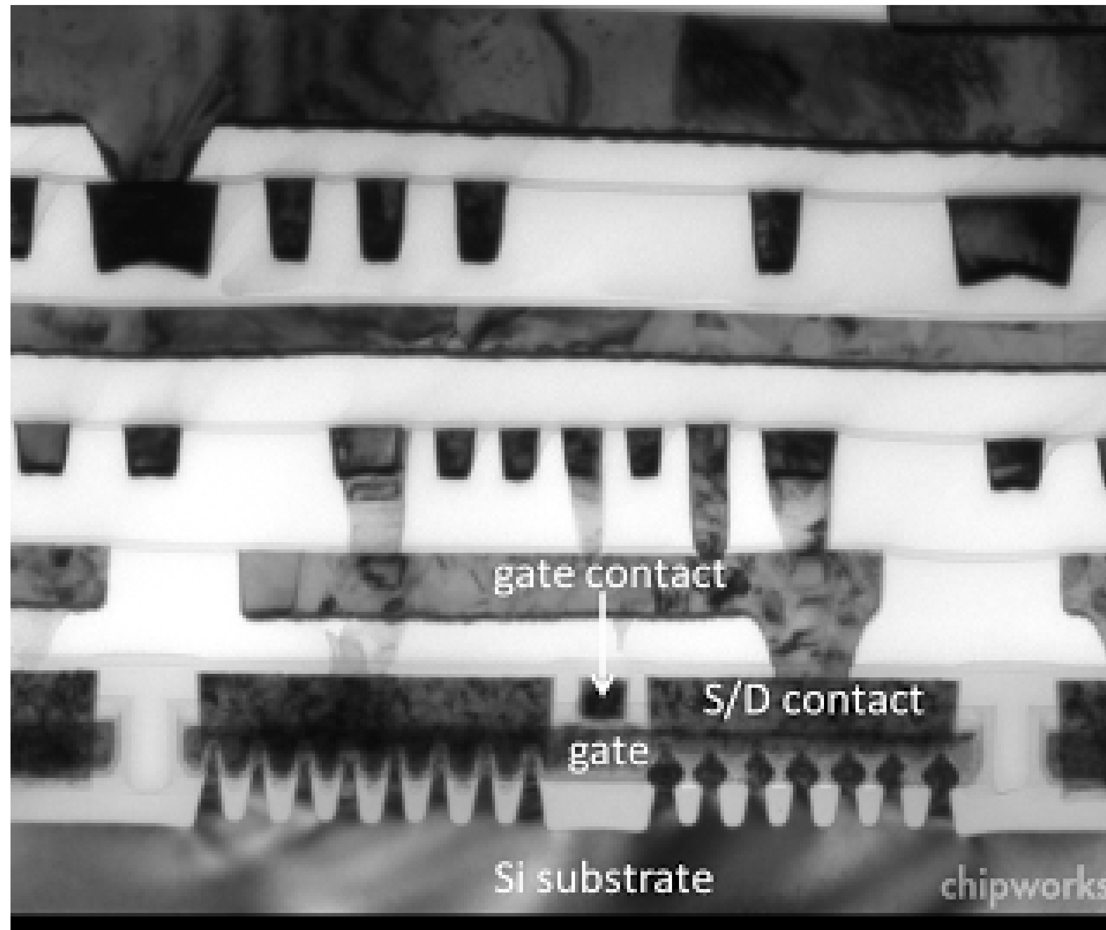


Intel Xeon E3-130V2 General Structure

A closer TEM image (Fig. 4) shows the lower metal stack and a pair of multi-fin NMOS and PMOS transistors. This section is parallel to the gate, across the fins, and we can see the contact trenches and metal levels M1 up to M5.

We have to digress here a little to explain what we're looking at. A typical TEM sample is 80 – 100 nm thick, to be thin enough to be transparent to the electron beam and at the same time have enough physical rigidity so that it does not bend or fall apart.

Here we are trying to image structures in a die with a gate length of less than 30 nm; so if we make a sample parallel to the gate, and if the sample is aligned perfectly along the centre of the gate, then it will contain the gate plus at least part of the source/drain (S/D) silicon and contacts on either side.



TEM Image of Lower Metals and NMOS and PMOS (right) Transistors

That is what we see above – I have labeled the gate and contact stripes, and we have PMOS on the right and NMOS on the left. The tungsten-filled contacts obscure parts of the gate, but we can clearly see that the PMOS S/D fins have epitaxial growth on them, and the fins have an unexpected slope – a little different from Intel's tri-gate schematic shown last year