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EDUCATION

Ph.D., Computer Science and Engineering 2001
University of Michigan, Ann Arbor, MI
Dissertation Title: *Improving Energy and Performance of Data Cache Architectures by Exploiting Memory Reference Characteristics*. (Horace H. Rackham Distinguished Dissertation Award, University of Michigan.)

M.S.E., Computer Science and Engineering 1994
University of Michigan, Ann Arbor, MI

B.S., Electrical Engineering 1990
National Tsinghua University, Hsin-Chu, Taiwan
Valedictorian of the Class 1990

EMPLOYMENT

Georgia Institute of Technology, Atlanta, GA July 2008 - Present
Associate Professor, School of Electrical and Computer Engineering

Georgia Institute of Technology, Atlanta, GA June 2003 - Present
Adjunct Faculty Member, College of Computing

Georgia Institute of Technology, Atlanta, GA August 2002 - June 2008
Assistant Professor, School of Electrical and Computer Engineering

Agere Systems, Atlanta, GA July 2001 - August 2002
Architecture Manager, StarCore Technology Center

Intel Corporation, Santa Clara, CA May 1999 - July 2001
Research Staff Member, Microprocessor Research Labs

The University of Michigan, Ann Arbor, MI January 1999 - August 2000
Research Assistant, Advanced Computer Architecture Lab

Intel Corporation, Folsom, CA October 1995 - April 1999
Senior Processor Architect, Microprocessor Division 6

Divio Corporation, Sunnyvale, CA September 1998 - January 1999
Consultant

The University of Michigan, Ann Arbor, MI May 1993 - August 1995
Research Assistant, Advanced Computer Architecture Lab

The Chinese Infantry School, Kaohsiung, Taiwan December 1990 - May 1992
Instructor Officer, Electronics and Signal Corps

TEACHING

Ph.D. Dissertation Supervision

- Joshua Bruce Fryman, *SoftCache Architecture*, College of Computing, Georgia Institute of Technology, (Co-advised with Umakishore Ramachandran), August 2005. Current position: Senior Staff Engineer at Intel Corporation, Hillsboro, OR.
- Weidong Shi, *Architectural Support for Protecting memory Integrity and Confidentiality*, College of Computing, Georgia Institute of Technology, April 2006. Current position: Assistant Professor, Computer Science Department, University of Houston, Houston, TX.
- Taeweon Suh, *Integration and Evaluation of Cache Coherence Protocols for Multiprocessor SOCs*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2006. Current position: Associate Professor, Computer Science Education Department, Korea University, Seoul, South Korea.
- Kiran Puttaswamy, *Designing High-Performance Microprocessors in 3-D Integration Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Gabriel Loh), December 2007. Current position: Senior Design Engineer at Intel Corporation, Austin, TX.
- Chinnakrishnan Ballapuram, *Semantic-Oriented Low Power Architecture*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Senior Design Engineer at Intel Corporation, Folsom, CA.
- Mrinmoy Ghosh, *Microarchitectural Techniques to Reduce Energy Consumption in the Memory Hierarchy*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2009. Current position: Researcher at ARM Corporate R&D, Austin, TX.
- Dong Hyuk Woo, *Designing Heterogeneous Many-Core Processors to Provide High Performance Under Limited Power Budget*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2010. Current position: Researcher at Intel Labs, Intel Corporation, Santa Clara, CA.

Master's Thesis Supervision

- Prateek Tandon, *High-Performance Advanced Encryption Standard (AES) Security Co-Processor Design*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2003. Current position: Senior Design Engineer at Intel Corporation, Santa Clara, CA.
- Aniket Naik, *Efficient Conditional Synchronization for Transactional Memory Based System*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Milos Prvulovic), August 2006. Current position: Senior Hardware Engineer at Nvidia Corporation, Santa Clara, CA.
- Fayez Mohamood, *DLL-conscious Instruction Fetching for SMT Processors*, School of Electrical and Computer Engineering, Georgia Institute of Technology, August 2006. Current position: Product Manager at BigDoor Media, Inc., Seattle, WA.
- Richard M. Yoo, *Adaptive Transaction Scheduling for Transactional Memory Systems*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Ph.D. student at Stanford University, Stanford, CA.
- Pratik Marolia, *Watermarking FPGA Bitstream for IP Protection*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Design Engineer, Intel Corporation, Hillsboro, OR.
- Vikas Rangaswamy Vasisht, *Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2008. Current position: Design Engineer, Intel Corporation, Austin, TX.
- Manoj Balanageswaran Athreya, *Subverting Linux On-the-fly using Hardware Virtualization Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2010. Current position: Design Engineer, Qualcomm Inc., San Diego, CA.

Current Ph.D. Students

- Dean L. Lewis. Thesis subject: "Design for Pre-bond Testability in 3D Integrated Circuits." (7th year Ph.D. student.)
- Nak Hee Seong. Thesis subject: "A Reliable, Secure Phase-Change Memory as a Main Memory." (5th year Ph.D. student.)
- Sungkap Yeo. Thesis subject: "Achieving High Energy Efficiency for Data Center Computing." (5th year Ph.D. student.)
- Jen-Cheng Huang. Thesis subject: "Virtualized Secure Multi-Core System." (4th year Ph.D. student.)
- Tzu-Wei Lin. Thesis subject: "Implementing Many-Core Processor Using 3D Integration Technology." (3rd year Ph.D. student.)
- Mohammad M. Hossain. Thesis subject: "Optimization for Virtual Machine based Data Center." (3rd year Ph.D. student.)
- Lifeng Nai. Thesis subject: "Unified Multi-Core Architecture for Transactional Memory and Speculative Multithreading." (1st year Ph.D. student.)

COURSES TAUGHT and DEVELOPED

- **ECE2030 Introduction to Computer Systems.** I designed a few creative term projects (in different semesters) to help students to solve real and interesting logic and computer design problems and to understand machine-level operations using MIPS assembly programming. For example, one project asked students to design a decryption algorithm using MIPS assembly languages by reverse-engineering the ciphertext that I provided. Another example is a project to find the perfect number (equivalent to the summation of its own factors) for a given range. Both projects require algorithmic designs at the machine instruction level. Students learn not only how to program at machine level assembly languages, but also brainstorm ideas with respect to how to accelerate their programs for higher efficiency.
- **ECE3055 Computer Architectures and Operating Systems.** I offered this course every other year based on the materials developed by several other faculty including myself.
- **ECE4100/6100 Advanced Computer Architecture.** I renovated the materials and designed new course projects to increase students' understanding on crucial microarchitectural modules in modern microprocessors and familiarize them with the design tools. The projects include an instruction cache enhanced with victim cache (in structural Verilog model), an Alpha 21264-like tournament hybrid branch predictor (in behavioral Verilog model), latest branch predictors (*e.g.*, perceptron predictor, O-GEHL predictor, etc.), and a dynamic instruction scheduler (in behavioral Verilog model), and a MOESI cache coherence protocol (in C/C++). These projects imitate how these crucial microarchitectural modules were designed in a real processor design team and help students drive the algorithm-level concepts learned in class into functional designs at the logic gate level.
- **ECE4893 Multicore and GPU Programming for Video Games.** Dr. Aaron Lanterman and myself designed this new course to respond to the timely demand for computer engineers in the GPU, 3D gaming, and parallel application industries. This class focuses on the hardware architecture design and programming model for the emerging multi-core processors and GPGPUs. Several mini-projects based on widely used API (Microsoft Direct3D), shader language (HLSL/Cg), and development environment (Microsoft XNA) were designed to enrich students' experiences and develop their programming skills on these special purpose processors. The projects were designed to run on the latest Nvidia GeForce graphics cards and Cell Blades in the Cell Center of Competence.
- **ECE7102 RISC Architectures.** This course was completely renovated to focus on latest developments in microarchitecture research. In addition, in-depth design details of commercial high-performance microprocessors such as EPIC from Intel/HP and Pentium 4 from Intel were also incorporated into the course materials. Simplescalar, the most popular architecture simulator adopted in

academia was used in this course. Programming assignments based on SimpleScalar were designed for students to learn how to perform microarchitecture research by using this toolkit.

- **CS8001 Computer Architecture Seminar.** Computer architecture faculty from both ECE and CS co-managed this weekly meeting to discuss the latest research and industry trend in the general area of computer architecture. I was one of the most senior faculty members among them to organize this reading group since 2002. It became a credit course for those who are doing or interested in computer architecture research.
- **CS8803 Language and Compiler for Embedded Systems.** Dr. Santosh Pande of CS and I developed this course for a dual-degree master program offered by Georgia Tech and Korea University. The course targets higher education in embedded software for engineers from Korean industry including Samsung, LG, and Korean Telecom. I developed several course modules and class projects emphasizing on the design of instruction set architecture for embedded system, high performance techniques for exploiting instruction-level parallelism (ILP) in embedded software, code compression techniques, real-time scheduling for embedded systems, and embedded security issues. Two projects developed for this course. The first project is to build a control-flow graph for given VLIW codes and find the ILP for them; the second one is to implement and evaluate the compression efficiency for a few code compression techniques including one similar to the method used by IBM CodePack and one dictionary-based compression algorithm.
- **ECE8833 Polymorphic and Many-Core Computer Architecture.** I developed this special topic course intended to replace the older ECE7102. The content covers classical work in computer architecture as well as the latest, emerging issues and research topics in the field. The students are required to form a two- to three-people's team and propose a research project for their term project.

RESEARCH GRANTS

Research Grants from Federal Agency

- GF1. **National Science Foundation (NSF):** "ITR: Toward Autonomous Computing Platforms: System-Wide Hardware/Software Performance Monitoring and Adaptation." Co-PI with Sally McKee (Cornell), \$814,000 (Lee's allocation: \$407,000.) 10/2003 - 09/2009.
- GF2. **National Science Foundation (NSF):** "ITR: Morphable Software Services: Self-Modifying Programs for Distributed Embedded Systems Organization: National Science Foundation." Co-PI with Karsten Schwan, Tucker Balch, Greg Eisenhauer, Santosh Pande, Calton Pu. (Lee was listed as a senior personnel.) \$1,033,775. (Lee's allocation: \$147,683.) 10/2003 - 05/2007.
- GF3. **US Department of Energy (DoE) Early CAREER PI Award:** "Toward Highly Secure and Autonomic Computing Systems: A Hierarchical Approach." PI, \$299,755. 08/2005 - 08/2009. (Georgia Tech Office of VP of Research supplemented with \$15,000.)
- GF4. **National Science Foundation (NSF):** "CAREER: Introspective Computing - A Multicore Approach to Availability, Reliability, and Security." PI, \$400,000. 06/2007 - 05/2012. (Georgia Tech Office of VP of Research supplemented with \$25,000 and one research assistant for the project period.)
- GF5. **National Science Foundation (NSF):** "CPA: Parallel-On-Demand — A Broad Purpose 3D-Integrated Performance Acceleration Layer for General Purpose Processors." PI, \$255,000. 07/2008 - 8/2012.
- GF6. **National Science Foundation (NSF):** "CCLI-Phase 1 Exploratory: Problem-Based Learning of Multithreaded Programming." PI, \$54,843. 01/2009 - 08/2010.
- GF7. **US Department of Defense (DoD):** "Design, Fabrication, and Testing of 3D-MAPS: A Massively Parallel Processor with 3D Stacked Memory." PI with Sung Kyu Lim and Gabriel Loh. \$941,543. (Lee's allocation: \$313,848.) 05/2009 - 04/2011.
- GF8. **National Science Foundation (NSF):** "II-NEW: GreenIT: Testbeds for Real-time Data Center and Platform Energy and Thermal Management." Co-PI with Karsten Schwan, Yogendra Joshi, Hyesoon Kim, and Saibal Mukhopadhyay. \$410,000 (Lee's allocation \$82,000.) 03/2010 - 02/2011.

- GF9. **National Science Foundation (NSF):** "CSR: A Unified Many-Core Architecture for Enabling Speculative Multithreading and Transactional Memory." PI, \$351,831. 08/2010 - 07/2013.
- GF10. **US Department of Defense (DoD):** "3D-MAPS V2: A Massively Parallel Processor with 3D Stacked Memory." PI with Sung Kyu Lim. \$295,776. (Lee's allocation: \$147,888.) 08/2011 - 09/2012.

Research Grants from Industry and Others

- GI1. **CERCS Industry Research Fund:** "Semantics-Oriented Low-power Architecture." PI, \$40,000. 10/2002 - 12/2003.
- GI2. **Intel Corporation:** "Equipment grant for embedded computing research." Co-PI with Karsten Schwan. \$25,000. 01/2004.
- GI3. **Semiconductor Research Corporation's MARCO Centers GSRC/C2S2:** "High Performance 3D Microarchitecture Design." PI with Sung Kyu Lim and Gabriel Loh. \$210,000 (Lee's allocation: \$70,000.) 07/2005 - 08/2006.
- GI4. **Intel Corporation:** "Curriculum Development Addressing Multi-Core Platform Issues." Co-PI with Ada Gavrilovska, Karsten Schwan, and Matt Wolf. \$78,168 (Lee's allocation: \$16,000.) 01/2006 - 04/2007.
- GI5. **Semiconductor Research Corporation's MARCO Center C2S2:** "High Performance 3D Microarchitecture Design." PI with Sung Kyu Lim and Gabriel Loh. \$450,000 (Lee's allocation: \$150,000.) 08/2006 - 07/2009.
- GI6. **Intel Corporation:** "Parallelizing Applications for Intel Multicore Processors." Co-PI with Ada Gavrilovska. \$50,000 (Lee's allocation: \$25,000.) 01/2007 - 04/2007.
- GI7. **Intel Corporation:** "Collaborative Multi-core Training." Co-PI with Ada Gavrilovska, Karsten Schwan, and Matt Wolf. \$38,500. (Lee's allocation: \$9,625.) 08/2007 - 07/2008.
- GI8. **Intel Corporation:** "Curriculum Development Addressing Multi-Core Platform Issues." Co-PI with Ada Gavrilovska, Karsten Schwan, and Matt Wolf. \$80,000 (Lee's allocation: \$20,000.) 01/2008 - 12/2008.
- GI9. **Intel Corporation:** "Accelerating Medical Image Reconstruction for Multicore Processors." PI, \$25,000. 01/2008 - 12/2008.
- GI10. **Intel Corporation:** "Thread Fairness in the Larrabee Architecture." Co-PI with Hyesoon Kim. \$45,000 (Lee's allocation: \$22,500.) 09/2008 - 08/2009.
- GI11. **Georgia Tech Focused Research Program (FRP):** "GreenIT: IT Technologies for Green Computing." Co-PI with Sudhakar Yalamanchili, Ada Gavrilovska, Yogendra Joshi, Hyesoon Kim, Saibal Mukhopadhyay, Karsten Schwan. \$75,000 (Lee's allocation: \$15,000.) 08/2009 - 04/2010.
- GI12. **Intel Corporation:** "Thread Fairness in the Larrabee Architecture (Phase II)." Co-PI with Hyesoon Kim. \$45,000 (Lee's allocation: \$22,500.) 01/2010 - 08/2012.
- GI13. **Intel Corporation:** "Exploiting Memory Hierarchy for Heterogeneous Multi-Core Systems: A Holistic Approach." PI, \$80,000. 04/2010 - 08/2012.
- GI14. **Intel Corporation:** "Curriculum Development: Intel Atom in Embedded Systems Courses." Co-PI with Ada Gavrilovska, Santosh Pande, Karsten Schwan, Matt Wolf, and Sudhakar Yalamanchili. \$70,000 (Lee's allocation \$11,500.) 01/2011 - 04/2012.
- GI15. **Industrial Technology Research Institute (ITRI), Taiwan:** "Accelerated Computing Using 3-D Integration Technology." PI, \$70,000. 08/2011 - 07/2012.
- GI16. **IBM Corporation:** "Architectural Exploration for Emerging Memory Technologies." PI, \$45,000 (through IBM Faculty Award.)
- GI17. **Samsung Electronics Corporation:** "Test and Repair Methodologies for 3D Stacked DRAM with Through Silicon Vias." PI, \$100,000. 03/2012 - 04/2013.

HONOR AND AWARDS

- Chancellor Mei Yi-Chi Memorial Award, 1989.
- Valedictorian of the Class 1990 of National Tsinghua University, Hsinchu, Taiwan, 1990.
- University of Michigan Research Fellowship, 2003.
- Intel Division Award, 1996.
- Intel Foundation Fellowship, 2000-2001.
- Best Paper Award. *The 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33)*, 2000. (Paper C4.)
- Horace H. Rackham Distinguished Dissertation Award, University of Michigan, 2001.
- Best Paper Award. *The 2004 ACM/IEEE International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES-2004)*, 2004. (Paper C14.)
- Department of Energy Early CAREER Principal Investigators Award, 2005.
- Best Paper Award. *The 2nd Watson Conference on Interaction Between Architecture, Circuits and Compilers (P = AC²)*, Yorktown Heights, New York, September 2005. (Paper C23.)
- ECE Outstanding Junior Faculty Award, Georgia Tech, 2006.
- Best Paper Award nomination. *The 17th IEEE International Conference on Field Programmable Logic and Applications (FPL-07)*, Amsterdam, Netherlands, 2007. (Paper C40.)
- Best Paper Award Finalist. *The 11th Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, MA, 2007. (Paper W8.)
- NSF CAREER Award, 2007.
- Best Paper Award nomination. *The 2009 IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2009)*, San Jose, CA, 2009. (Paper C58.)
- IEEE MICRO Top Picks from the Computer Architecture Conferences of 2010. (Paper J20.)
- IBM Faculty Award, 2011.
- Best Paper Award. *The ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS 2011)*, Polytechnic Institute of NYU, Brooklyn, NY, 2011. (Paper C67.)

SCHOLARLY ACCOMPLISHMENTS

Books and Part of Books

- B1. *Intel Architecture Software Optimization Reference Manual*, Intel Literature Center, order number: 245127-001, August, 1998. (Author of Chapter 6: Optimizing Cache Utilization for Pentium III Processor, pp.6-1 to pp.6-30, and Appendix A: The Mathematics of Prefetch Scheduling Distance, pp.F-1 to pp.F-12.)
- B2. Abderrahim Benquassmi, Eric Fontaine, and Hsien-Hsin S. Lee. "Parallelization of Katsevich CT Image Reconstruction Algorithm on Generic Multi-Core Processors and GPGPU." In *GPU Computing GEMS, Section 10 Medical Imaging, Chapter 31*, Wen-Mei Hwu (editor-in-chief), Morgan Kaufmann Publishers, 2011.
- B3. Sungkap Yeo and Hsien-Hsin S. Lee. "Peeling the Power Onion of Data Centers." A book chapter to appear in *Energy Efficient Thermal Management of Data Centers* by Yogendra Joshi (editor-in-chief), Springer, 2012.

Refereed Journal Publication

- J1. Paul Zagacki, Deep Buch, Emile Hsieh, Daniel Melaku, Vladimir Pentkovski, and Hsien-Hsin Lee, "Architecture of a 3D Software Stack for Peak Pentium III Processor Performance." *Intel Technology Journal*, Volume 3, Issue 2, May, 1999.
- J2. Hsien-Hsin S. Lee, Gary S. Tyson, and Matthew K. Farrens, "Bandwidth Utilization using Eager Writeback." *Journal of Instruction-Level Parallelism*, Vol. 4, 2001.
- J3. Joshua B. Fryman, Chad M. Huneycutt, Hsien-Hsin S. Lee, Kenneth M. Mackenzie and David E. Schimmel, "Energy Efficient Network Memory for Ubiquitous Devices." In *IEEE MICRO special issue on Power Complexity Aware Design*, pp. 60-70, September/October 2003.
- J4. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 1." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.33-41, July/August 2004.
- J5. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 2." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.70-78, September/October 2004.
- J6. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh, "Towards the Issues in Architectural Support for Protection of Software Execution." In *ACM SIGARCH Computer Architecture News*, Vol. 33, Issue 1, pp.6-15, March 2005.
- J7. Mongkol Ekpanyapong, Jacob Minz, Thaisiri Watwai, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol.25, No.7, pp.1289-1300, July, 2006.
- J8. Chenghuai Lu, Tao Zhang, Weidong Shi, and Hsien-Hsin S. Lee, "M-TREE: A High Efficiency Security Architecture for Protecting Integrity and Privacy of Software." In *Journal of Parallel and Distributed Computing, Special Issue on Security in Grid and Distributed Systems*, Vol.66, Issue 9, pp.1116-1128, 2006. (acceptance rate =12.2%, 10/82.)
- J9. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." Invited article. In *Transactions of High Performance Embedded Architectures and Compilers*, Vol.1, pp.95-115, 2007. Springer Verlag.
- J10. Xiaotong Zhuang and Hsien-Hsin S. Lee, "Reducing Cache Pollution via Dynamic Data Prefetch Filtering." In *IEEE Transactions on Computers*, Vol.56, No.1, pp.18-31, January, 2007.
- J11. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, "Multi-Objective Microarchitectural Floorplanning For 2D and 3D ICs." In *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.26, No.1, pp.38-52, 2007.
- J12. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee. "POD: A 3D-integrated Broad-Purpose Acceleration Layer." In *IEEE MICRO special issue on Accelerator Architectures*, pp.28-40, July/August, 2008.
- J13. Fayez Mohamood, Mrinmoy Ghosh, and Hsien-Hsin S. Lee. "DLL-Conscious Instruction Fetch Optimization for SMT Processors." In *Journal of Systems Architecture*, 54, pp.1089-1100, 2008.
- J14. Dong Hyuk Woo and Hsien-Hsin S. Lee. "Extending Amdahl's Law for Energy-Efficient Computing in the Many-Core Era." In *IEEE Computer*, Vol.41, No.12, pp.24-31, December, 2008.
- J15. Dong Hyuk Woo and Hsien-Hsin S. Lee. "PROPHET: Goal-Oriented Provisioning for Highly Tunable Multicore Processors in Cloud Computing." In *ACM SIGOPS Operating Systems Review special issue on the Interaction among the OS, Compilers, and Multicore Processors*, Vol.43, Issue 2, pp.102-103, April, 2009.
- J16. Hsien-Hsin S. Lee and Krishnendu Chakrabarty. "Test Strategies for 3D Integrated Circuits." In *IEEE Design & Test of Computers, Special Issue on 3D IC Design and Test*, vol.26, no.5, pp.26-35, September/October, 2009.

- J17. Jun Yang, Lan Gao, Youtao Zhang, Marek Chrobak, and Hsien-Hsin S. Lee. "A Low-Cost Memory Remapping Scheme for Address Bus Protection" In *Journal of Parallel and Distributed Computing*, vol.70, issue 5, pp.443-457, May 2010.
- J18. Sung Woo Chung, Hsien-Hsin S. Lee, and Woo Hyong Lee. "Architecture/OS Support for Embedded Multi-core Systems." In *The Computer Journal*, vol.53, no.8, pp.1134-1135, 2010.
- J19. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, and Hsien-Hsin S. Lee. "Chameleon: Virtualizing Idle Acceleration Cores of A Heterogeneous Multi-Core Processor for Caching and Prefetching." In *ACM Transactions on Architecture and Code Optimization*, vol.7, no.1, pp.1-35, April, 2010.
- J20. Nak Hee Seong, Dong Hyuk Woo, and Hsien-Hsin S. Lee. "Security Refresh: Prevent Malicious Wear-out and Increase Durability for Phase-Change Memory with Dynamically Randomized Address Mapping." In *IEEE MICRO special issue on Top Picks from the Computer Architecture Conferences of 2010*, pp.119-127, January/February, 2011.
- J21. Ahmad Sharif and Hsien-Hsin S. Lee, "Data Prefetching by Exploiting Global and Local Access Patterns." In *Journal of Instruction-Level Parallelism, Special Issue: The First JILP Data Prefetching Championship (DPC-1)*, Volume 13, 2011. ISSN 1942-9525.
- J22. Xin Zhao, Dean Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Low-Power Clock Tree Design for Pre-Bond Testing of 3D Stacked ICs." In *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.30, No.5, pp.732-745, 2011.
- J23. Sungkap Yeo and Hsien-Hsin S. Lee. "Using Mathematical Modeling in Provisioning a Heterogeneous Cloud Computing Environment." In *IEEE Computer*, Vol. 44, No. 8, pp. 55-62, August, 2011.
- J24. Michael B. Healy, Fayez Mohamood, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Integrated Microarchitectural Floorplanning and Runtime Controller for Inductive Noise Mitigation." In *ACM Transactions on Design Automation of Electronic Systems*, Volume 16, Issue 4, pp.46:1-25, 2011.
- J25. Dong Hyuk Woo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Pragmatic Integration of An SRAM Row Cache in Heterogeneous 3D DRAM Architecture using TSV." To appear in *IEEE Transactions on Very Large Scale Integrated Circuits and Systems*, 2012.

Refereed Conference Publication

- C1. Eric L. Boyd, Waqar Azeem, Hsien-Hsin Lee, Tien-Pao Shih, Shih-Hao Hung, and Edward S. Davidson, "A Hierarchical Approach to Modeling and Improving the Performance of Scientific Applications on the KSR1." In *Proceedings of the 1994 International Conference on Parallel Processing (ICPP-94)*, pp.188-192, St. Charles, Illinois, August, 1994.
- C2. Hsien-Hsin Lee, Youfeng Wu, and Gary Tyson, "Quantifying Instruction-Level Parallelism Limits on an EPIC Architecture." In *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2000)*, pp.21-27, Austin, Texas, April, 2000.
- C3. Hsien-Hsin S. Lee and Gary S. Tyson, "Region-based Caching: an Energy-Delay Efficient Memory Architecture for Embedded Processors." In *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES'00)*, pp.120-127, San Jose, California, November, 2000.
- C4. Hsien-Hsin S. Lee, Gary S. Tyson, and Matthew K. Farrens, "Eager Writeback - a Technique for Improving Bandwidth Utilization." In *Proceedings of the 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33)*, pp.11-21, Monterey, California, December, 2000. **(Best Paper Award of MICRO-33.)**
- C5. Hsien-Hsin S. Lee, Mikhail Smelyanskiy, Chris J. Newburn, and Gary S. Tyson, "Stack Value File: Custom Microarchitecture for the Stack." In *Proceedings of the 7th IEEE International Symposium on High Performance Computer Architecture (HPCA-7)*, pp.5-14, Monterrey, Mexico, January, 2001. (acceptance rate = 23.6%, 26/110)

- C6. Mikhail Smelyanskiy, Scott A. Mahlke, Edward S. Davidson, and Hsien-Hsin S. Lee, "Predicate-aware Scheduling: A Technique for Reducing Resource Constraints." In *Proceedings of the First Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO-2003)*, pp.168-177, Fisherman's Wharf, San Francisco, California, March 2003. (acceptance rate =35.4%)
- C7. Hsien-Hsin S. Lee and Chinnakrishnan S. Ballapuram, "Energy Efficient D-TLB and Data Cache using Semantic-Aware Multilateral Partitioning." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03)*, pp. 306-311, Seoul, Korea, August 2003. (acceptance rate = 24.4%, 54/221)
- C8. Xiaotong Zhuang and Hsien-Hsin S. Lee, "A Hardware Based Cache Pollution Filtering Mechanism for Aggressive Prefetches." In *Proceedings of the International Symposium on Parallel Processing (ICPP-03)*, pp.286-293, Kaohsiung, Taiwan, October 2003. (acceptance rate = 20% in architecture track)
- C9. Yuvraj S. Dhillon, Abdulkadir U. Diril, Abhijit Chatterjee, and Hsien-Hsin S. Lee, "An Algorithm for Achieving Minimum Energy Consumption in CMOS Circuits Using Multiple Supply and Threshold Voltages at the Module Level." In *Digest of Technical Papers of the International Conference on Computer-Aided Design (ICCAD-03)*, pp.693-700, San Jose, California, November 2003. (acceptance rate = 26%, 130/490)
- C10. Taeweon Suh, Douglas M. Blough and Hsien-Hsin S. Lee, "Supporting Cache Coherence in Heterogeneous Multiprocessor Systems." In *Proceedings of the Design Automation and Test in Europe Conference (DATE'04)*, pp.1150-1155, Paris, France, February 2004. (acceptance rate = 23.2%, 181/780)
- C11. Mongkol Ekpanyapong, Jacob R. Minz, Thaisiri Watwai, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design." In *Proceedings of the 41st Design Automation Conference (DAC-2004)*, pp.634 -639, San Diego, California, June 2004. (acceptance rate = 21%, 163/785)
- C12. Mongkol Ekpanyapong, Pinar Korkmaz, and Hsien-Hsin S. Lee, "Choice Predictor for Free." In *Proceedings of the 9th IEEE Asia-Pacific Computer Systems Architecture Conference (ACSAC-2004)*, pp.399 - 413, Beijing, China, September 2004.
- C13. Mrinmoy Ghosh, Weidong Shi, and Hsien-Hsin S. Lee, "CoolPression — A Hybrid Significance Compression Technique for Reducing Energy in Caches." In *Proceedings of the IEEE International System-On-Chip Conference (SOCC-2004)*, pp. 399 - 402, Santa Clara, California, September, 2004.
- C14. Xiaotong Zhuang, Tao Zhang, Hsien-Hsin S. Lee and Santosh Pande, "Hardware Assisted Control Flow Obfuscation for Embedded Processors." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'04)*, pp. 292 - 302, Washington D.C., September 2004. (acceptance rate=25.2%, 31/123) . **(Best Paper Award of CASES 2004.)**
- C15. Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, and Chenghuai Lu, "Architectural Support for High Speed Authentication of Shared Memory in Multiprocessor Systems." In *Proceedings of the International Conference on Parallel Architecture and Compilation Techniques (PACT'04)*, pp. 123 - 134, Antibes Juan-les-Pins, France, September 2004. (acceptance rate = 18.8%, 23/122)
- C16. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu and Tao Zhang, "Attacks and Risk Analysis for Hardware Supported Software Copy Protection Systems." In *Proceedings of the 4th ACM Workshop on Digital Right Management (DRM'2004)*, pp.54-62, Washington D.C., October 2004.
- C17. Mongkol Ekpanyapong, Sung Kyu Lim, Chinnakrishnan Ballapuram, and Hsien-Hsin S. Lee, "Wire-driven Microarchitectural Design Space Exploration," In *Proceedings of the 2005 IEEE International Symposium on Circuits and Systems (ISCAS-05)*, pp.1867-1870, Kobe, Japan, May 2005.
- C18. Martin Schulz, Brian S. White, Sally A. McKee, Hsien-Hsin S. Lee, and Jurgen Jeitner, "Owl: Next Generation System Monitoring." In *Proceedings of the ACM Computing Frontiers 2005*, pp.116-124, Ischia, Italy, May 2005.
- C19. Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu, and Alexandra Boldyreva, "High Efficiency Counter Mode Security Architecture via Prediction and Precomputation." In *Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32)*, pp.14-24, Madison, Wisconsin, June 2005. (acceptance rate = 23.2%, 45/194)

- C20. Weidong Shi, Hsien-Hsin S. Lee, Guofei Gu, Mrinmoy Ghosh, Laura Falk, and Trevor Mudge, "Intrusion Tolerant and Self-recoverable Network Service System Using Security Enhanced Chip Multiprocessor." In *Proceedings of the 2nd IEEE International Conference on Autonomic Computing (ICAC-05)*, pp.263-273, Seattle, WA, June 2005. (acceptance rate of regular papers = 16.7%, 25/150)
- C21. Taeweon Suh, Daehyun Kim, and Hsien-Hsin S. Lee, "Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MP SoCs." In *Proceedings of the 42nd Design Automation Conference (DAC-42)*, pp.553-558, Anaheim, California, June 2005. (acceptance rate=20%)
- C22. Chinnakrishnan S. Ballapuram, Hsien-Hsin S. Lee, and Milos Prvulovic, "Synonymous Address Compaction for Energy Reduction in Data TLB." In *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED-05)*, pp.357-362, San Diego, California, August 2005. (acceptance rate=22%, 53/233)
- C23. Fayez Mohamood, Mrinmoy Ghosh and Hsien-Hsin S. Lee, "DLL-Conscious Instruction Fetch Optimization for SMT Processors." In *Proceedings of the 2nd Watson Conference on Interaction Between Architecture, Circuits and Compilers (P = AC²)*, pp.143-152, Yorktown Heights, New York, September 2005. . **(Best Paper Award of P = AC².)**
- C24. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." In *Proceedings of the 2005 International Conference on High Performance Embedded Architectures and Compilers (HiPEAC 2005)*, pp.153 - 168, Barcelona, Spain, November 2005. (acceptance rate=20.2%, 17/84)
- C25. Weidong Shi, Joshua B. Fryman, Guofei Gu, Hsien-Hsin S. Lee, Youtao Zhang, and Jun Yang, "InfoShield: A Security Architecture for Protecting Information Usage in Memory." In *Proceedings of the 12th International Conference on High Performance Computer Architectures (HPCA-12)*, pp.225-234, Austin, Texas, February 2006. (acceptance rate=14%)
- C26. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, "Microarchitectural Floorplanning Using Performance and Temperature Tradeoff." In *Proceedings of the Design, Automation and Test in Europe (DATE-06)*, pp.1288-1293, Munich, Germany, March 2006. (acceptance rate = 17%)
- C27. Mrinmoy Ghosh, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee, "Efficient System-on-Chip Energy Management with a Segmented Bloom Filter." In *Proceedings of the Architecture of Computing Systems (ARCS'05)*, pp.283-297, Frankfurt, Germany, March 2006. (acceptance rate = 21%)
- C28. Weidong Shi, Hsien-Hsin S. Lee, Laura Falk, and Mrinmoy Ghosh, "An Integrated Framework for Dependable and Revivable Architecture Using Multicore Processors." In *Proceedings of the 33rd International Symposium on Computer Architecture (ISCA-33)*, pp.102-113, Boston, MA, June 2006. (acceptance rate = 13%, 31/231)
- C29. Lan Gao, Jun Yang, Marek Chrobak, Youtao Zhang, San Nguyen, and Hsien-Hsin S. Lee, "A Low-cost Memory Remapping Scheme for Address Bus Protection." In *Proceedings of the 15th International Conference on Parallel Architecture and Compilation Techniques (PACT'06)*, pp.74-83, Seattle, WA, September 2006. (acceptance rate = 25.6%, 30/117)
- C30. Weidong Shi, Hsien-Hsin S. Lee, Richard M. Yoo, and Alexandra Boldyreva, "A Digital Rights Enabled Graphics Processing System." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware*, pp.17-26, Vienna, Austria, September 2006. (acceptance rate = 31.1%, 14/45)
- C31. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "DRAMdecay: Using Decay Counters to Reduce Energy Consumption in DRAMs." In *Proceedings of the 3rd Watson Conference on Interaction between Architecture, Circuits and Compilers (PAC²)*, Yorktown Heights, NY, October, 2006.
- C32. Chinnakrishnan S. Ballapuram, Kiran Puttaswamy, Gabriel H. Loh and Hsien-Hsin S. Lee, "Entropy-based Low Power Data TLB Design." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.304-311, Seoul, Korea, October, 2006. (Short paper acceptance rate = 39.8%, 41/103)

- C33. Dong Hyuk Woo, Mrinmoy Ghosh, Emre Ozer, Stuart Biles and Hsien-Hsin S. Lee, "Reducing Energy of Virtual Cache Synonym Lookup using Blooming Filters." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.179-189, Seoul, Korea, October, 2006. (Regular paper acceptance rate = 24.3%, 25/103)
- C34. Richard M. Yoo, Han Lee, Kingsum Chow, and Hsien-Hsin S. Lee, "Constructing a Non-Linear Model with Neural Networks For Workload Characterization." In *Proceedings of the 2006 IEEE International Symposium on Workload Characterization (IISWC-06)*, pp.150-159, San Jose, California, October, 2006.
- C35. Weidong Shi, and Hsien-Hsin S. Lee, "Authentication Control Point and its Implications for Secure Processor Design." In *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp.103-112, Orlando, Florida, December, 2006. (acceptance rate = 24.1%, 42/174)
- C36. Fayez Mohamood, Michael Healy, Sung Kyu Lim, and Hsien-Hsin S. Lee, "A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design." In *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp. 3-14, Orlando, Florida, December, 2006. (acceptance rate = 24.1%, 42/174)
- C37. Fayez Mohamood, Michael Healy, Sung Kyu Lim, and Hsien-Hsin S. Lee, "Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling." In *Proceedings of the 12th Asia and South Pacific Design Automation Conference (ASP-DAC'07)*, pp.786-791, Yokohama, Japan, January, 2007. (acceptance rate = 32.1%, 131/408)
- C38. Taeweon Suh, Hsien-Hsin S. Lee, Shih-Lien Lu, and John Shen, "Coherence Traffic Considered Harmful - An FPGA Approach to Quantifying Coherence Traffic Efficiency on Multiprocessor Systems," In *International Symposium on Field-Programmable Gate Arrays (FPGA 2007)*, Monterey, California, February 2007. (poster paper.)
- C39. Weidong Shi and Hsien-Hsin S. Lee, "Accelerating Memory Decryption and Authentication with Frequent Value Prediction." In *Proceedings of the ACM International Conference on Computing Frontiers (CF'07)*, pp.35-46, Ischia, Italy, May, 2007.
- C40. Taeweon Suh, Shih-Lien L. Lu, and Hsien-Hsin S. Lee, "An FPGA Approach to Quantifying Coherence Traffic Efficiency on Multiprocessor Systems" In *Proceedings of the 17th IEEE International Conference on Field Programmable Logic and Applications (FPL 2007)*, pp. 47-53, Amsterdam, The Netherlands, August, 2007. (acceptance rate = 21%) (**Nominated for the Best Paper Award.**)
- C41. Richard M. Yoo, Hsien-Hsin S. Lee, Han Lee, and Kingsum Chow, "Hierarchical Means: Single Number Benchmarking with Workload Cluster Analysis." In *Proceedings of the 2007 IEEE International (IISWC-2007)*, pp.204-213, Boston, MA, September, 2007.
- C42. Dean L. Lewis, and Hsien-Hsin S. Lee, "A Scan-Island Based Design Enabling Pre-bond Testability in Die-Stacking Microprocessors." In *Proceedings of the International Test Conference (ITC 2007)*, pp. 1-8, Santa Clara, CA, October, 2007.
- C43. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Virtual Exclusion: An Architectural Approach to Reducing Leakage Energy in Caches for Multiprocessor Systems." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.
- C44. Eric Fontaine and Hsien-Hsin S. Lee, "Optimizing Katsevich Image Reconstruction Algorithm on Multicore Processors." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.
- C45. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Smart Refresh: An Enhanced Memory Controller Design for Reducing Energy in Conventional and 3D Die-Stacked DRAMs." In *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO-40)*, pp.134-145, Chicago, IL, December, 2007. (acceptance rate = 35/166 = 21%)
- C46. Michael Healy, Fayez Mohamood, Hsien-Hsin S. Lee and Sung Kyu Lim, "A Unified Methodology for Power Supply Noise Reduction in Modern Microarchitecture Design." In *Proceedings of the 13th IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC'08)*, pp.611-616, Seoul, Korea, 2008.

- C47. Chinnakrishnan S. Ballapuram, Ahmad Sharif, and Hsien-Hsin S. Lee, "Exploiting Access Semantics and Program Behavior to Reduce Snoop Power in Chip Multiprocessors." In *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII)*, pp.60-69, Seattle, WA, 2008. (acceptance rate = 31/127, 24.4%)
- C48. Richard M. Yoo, Yang Ni, Adam Welc, Bratin Saha, Ali-Reza Adl-Tabatabai, and Hsien-Hsin S. Lee, "Kicking the Tires of Software Transactional Memory: Why the Going Gets Tough." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp.265-274, Munich, Germany, 2008.
- C49. Richard M. Yoo and Hsien-Hsin S. Lee, "Adaptive Transaction Scheduling for Transactional Memory Systems." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp. 169-178, Munich, Germany, 2008.
- C50. Chinnakrishnan S. Ballapuram and Hsien-Hsin S. Lee, "Improving TLB Energy for Java Applications on JVM." In *Proceedings of the International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII)*, pp.218-223, Samos, Greece, 2008.
- C51. Ahmad Sharif and Hsien-Hsin S. Lee. "Total Recall: A Debugging Framework for GPUs." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware (GH-08)*, pp.13-20, Sarajevo, Bosnia-Herzegovina, June, 2008.
- C52. Vikas R. Vasisht and Hsien-Hsin S. Lee. "SHARK: Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits." In *Proceedings of the 41st ACM/IEEE International Symposium on Microarchitecture (MICRO-41)*, pp.106-116, Lake Como, Italy, November, 2008. (Acceptance rate = 19%, 40/210.)
- C53. Michael Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, and Sung Kyu Lim. "Thermal optimization in Multigranularity Multi-Core Floorplanning." In *Proceedings of the 14th IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC'09)*, pp.43-48, Yokohama, Japan, January, 2009.
- C54. Dean L. Lewis, Sudhakar Yalamanchili, and Hsien-Hsin S. Lee. "High Performance Non-blocking Switch Design in 3D Die-Stacking Technology." In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09)*, pp.25-30, Tampa, FL, May, 2009.
- C55. Dean L. Lewis and Hsien-Hsin S. Lee. "Testing Circuit-Partitioned 3D IC Designs." In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09)*, pp.139-144, Tampa, FL, May, 2009.
- C56. Mrinmoy Ghosh, Simon Ford, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. "Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED-09)*, pp.165-170, San Francisco, CA, August, 2009. **(Selected as one of seven papers of ISLPED highlight for publicity and press.)**
- C57. Dean L. Lewis and Hsien-Hsin S. Lee. "Architectural Evaluation of 3D Stacked RRAM Caches" In *Proceedings of the IEEE International 3D Systems Integration Conference (3DIC-09)*, pp.1-4. San Francisco, CA, September, 2009.
- C58. Xin Zhao, Dean L. Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Pre-bond Testable Low-Power Clock Tree Design for 3D Stacked ICs" In *Proceedings of the 2009 International Conference on Computer-Aided Design (ICCAD-09)*, pp.184-190, San Francisco, CA, November, 2009. **(Nominated for the Best Paper Award.)**
- C59. Dong Hyuk Woo, Nak Hee Seong, Dean L. Lewis, and Hsien-Hsin S. Lee. "An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth." In *Proceedings of the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA-16)*, pp.429-440, Bangalore, India, January, 2010. (Acceptance rate = 18%)

- C60. Dong Hyuk Woo and Hsien-Hsin S. Lee. "COMPASS: A Programmable Data Prefetcher Using Idle GPU Shaders." In *Proceedings of the 16th IEEE International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XV)*, pp.297-309, Pittsburgh, PA, March, 2010. (Acceptance rate = 17.7%, 32/181)
- C61. Nak Hee Seong, Dong Hyuk Woo, and Hsien-Hsin S. Lee. "Security Refresh: Prevent Malicious Wear-out and Increase Durability for Phase-Change Memory with Dynamically Randomized Address Mapping." In *Proceedings of the 37th IEEE International Symposium on Computer Architecture (ISCA-37)*, pp.383-394, Saint-Malo, France, June, 2010. (Acceptance rate = 18%, 44/245)
- C62. Michael B. Healy, Krit Athikulwongse, Rohan Goel, Mohammad M. Hossain, Dae Hyun Kim, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Moongon Jung, Brian Ouellette, Mohit Pathak, Hemant Sane, Guan hao Shen, Dong Hyuk Woo, Xin Zhao, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory." In *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, California, September, 2010.
- C63. Nak Hee Seong, Dong Hyuk Woo, Vijayalakshmi Srinivasan, Jude A. Rivers, and Hsien-Hsin S. Lee. "SAFER: Stuck-At-Fault Error Recovery for Memories." In *Proceedings of the 43rd ACM/IEEE International Symposium on Microarchitecture (MICRO-43)*, pp.115-124, Atlanta, Georgia, December, 2010. (Acceptance rate = 18%, 45/248)
- C64. Dong Hyuk Woo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Heterogeneous Die Stacking of SRAM Row Cache and 3-D DRAM: An Empirical Design Evaluation." In *Proceedings of the 54th IEEE International Midwest Symposium on Circuits and Systems*, pp.1 - 4, Seoul, Korea, August, 2011. (An invited paper.)
- C65. Mrinmoy Ghosh, Ripal Nathuji, Min Lee, Karsten Schwan, and Hsien-Hsin S. Lee. "Symbiotic Scheduling for Shared Caches in Multi-Core Systems Using Memory Footprint Signature." In *Proceedings of the 40th IEEE International Conference on Parallel Processing (ICPP-2011)*, Taipei, Taiwan, pp.11 - 20, September, 2011. (Acceptance rate = 22%, 81/363)
- C66. Dean L. Lewis, Shreepad Panth, Xin Zhao, Sung Kyu Lim, and Hsien-Hsin S. Lee. "Designing 3D Test Wrappers for Pre-bond and Post-bond Test of 3D Embedded Cores." In *Proceedings of the XXIX IEEE International Conference on Computer Design (ICCD-11)*, pp.90 - 95, University of Massachusetts, Amherst, USA, October, 2011.
- C67. Jen-Cheng Huang, Matteo Monchiero, Yoshio Turner, and Hsien-Hsin S. Lee. "Ally: OS-Transparent Packet Inspection Using Sequestered Cores." In *Proceedings of the ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS-11)*, pp. 1 - 11, Brooklyn, NY, October, 2011. (Acceptance rate = 32%, 20/62) (**Best Paper Award of ANCS-11.**)
- C68. Dae Hyun Kim, Krit Athikulwongse, Michael B. Healy, Mohammad M. Hossain, Moongon Jung, Ilya Khorosh, Gokul Kumar, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Shreepad Panth, Mohit Pathak, Minzhen Ren, Guan hao Shen, Taigon Song, Dong Hyuk Woo, Xin Zhao, Joungho Kim, Ho Choi, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim. "3D-MAPS: 3D Massively Parallel Processor with Stacked Memory." To appear in *Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2012.
- C69. Xiaodong Wang, Dilip Vasudevan, and Hsien-Hsin S. Lee. "Global Built-In Self-Repair for 3-D Memories with Redundancy Sharing and Parallel Testing." To appear in *IEEE International 3D System Integration Conference (3DIC-11)*, Osaka, Japan, 2012.

Refereed Workshop Publication

- W1. Hsien-Hsin S. Lee, Joshua B. Fryman, A. Utku Diril, and Yuvraj S. Dhillon, "The Elusive Metric for Low-Power Architecture Research." In *Workshop on Complexity-Effective Design (WCED-03) held in conjunction with the 30th ACM/IEEE International Symposium on Computer Architecture (ISCA-30)*, San Diego, California, June 2003. (acceptance rate=25%)

- W2. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh, "Toward the Issues in Architectural Support for Protection of Software Execution." In *Workshop on Architectural Support for Security and Anti-Virus (WASSA) in conjunction with the 11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XI)*, pp.1-9, Boston, Massachusetts, October 2004.
- W3. Martin Schulz, Brian White, Sally A. McKee, and Hsien-Hsin Lee, "A Vision for Next Generation System Monitoring." In *Workshop on Hardware Performance Monitor Design and Functionality in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, CA, 2005.
- W4. Christopher R. Clark, Ripal Nathuji, and Hsien-Hsin S. Lee, "Using an FPGA as a Prototyping Platform for Multi-core Processor Applications," In *Workshop on Architectural Research using FPGA Platforms (WARFP-2005) in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, CA, 2005.
- W5. Taeweon Suh, Hsien-Hsin S. Lee, Sally A. McKee, and Martin Schulz, "Evaluating System-wide Monitoring Capsule Design Using Xilinx Virtex-II Pro FPGA," In *Workshop on Architecture Research using FPGA Platforms (WARFP-2005) in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, CA, 2005.
- W6. Taeweon Suh, Hsien-Hsin S. Lee. Shih-Lien Lu, and John Shen, "Initial Observations of Hardware/Software Co-Simulation using FPGA in Architecture Research," In *Workshop on Architecture Research using FPGA Platforms (WARFP-2006) in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-12)*, Austin, Texas, 2006.
- W7. Dong Hyuk Woo and Hsien-Hsin S. Lee, "Analyzing Performance Vulnerability due to Resource Denial-of-Service Attack on Chip Multiprocessors." In *Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMPMSI) in conjunction with the 13th International Symposium on High-Performance Computer Architecture (HPCA-13)*, Phoenix, Arizona, February, 2007.
- W8. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee, "POD: A Parallel On-Die Architecture." In *Proceedings of the 11th Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, Massachusetts, September, 2007. (**Award Session**)
- W9. Eric Fontaine and Hsien-Hsin S. Lee. "Bicephaly: Maximizing Bandwidth by Duplexing Power and Data. In *Workshop on Wild and Crazy Ideas (WACI-VI) in conjunction with the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII)*, Seattle, WA, 2008.
- W10. Hrishikesh Amur, Ripal Nathuji, Mrinmoy Ghosh, Karsten Schwan, and Hsien-Hsin S. Lee. "IdlePower: Application-Aware Management of Processor Idle States." In *Workshop on Managed Many-Core Systems (MMCS) co-located with ACM/IEEE International Symposium on High Performance Distributed Computing (HPDC)*, Boston, MA, June, 2008.
- W11. Richard M. Yoo and Hsien-Hsin S. Lee. "Helper Transactions: Enabling Thread-Level Speculation via A Transactional Memory System." In *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA) in Conjunction with ACM/IEEE International Symposium on Computer Architecture (ISCA-35)*, Beijing, China, June 2008.
- W12. Ahmad Sharif and Hsien-Hsin S. Lee. "Data Prefetching Mechanism by Exploiting Global and Local Access Patterns" In *The First Journal of Instruction-Level Parallelism Data Prefetching Championship (DPC-1) in conjunction with the 15th IEEE International Symposium on High Performance Computer Architecture (HPCA-15)*, Raleigh, North Carolina, February, 2009.
- W13. Dean L. Lewis and Hsien-Hsin S. Lee. "Test Strategies for 3D Die Stacked Integrated Circuits." In *Workshop on 3D Integration ? Technology, Architecture, Design, Automation, and Test in conjunction with Design Automation and Test in Europe (DATE-09)*, Nice, France, April, 2009.

- W14. Dean Lewis, Michael Healy, Mohammad Hossain, Tzu-Wei Lin, Mohit Pathak, Hemant Sane, Sung Kyu Lim, Gabriel Loh, and Hsien-Hsin S. Lee. "Design and test of 3D-MAPS, a 3D Die-Stack Many-Core Processor." In *the First IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (poster)*, Austin, Texas, November, 2010.

Invited Talks

- T1. "Region-based Caching," given at the Department of Electrical and Computer Engineering, North Carolina State University (Host: Prof. Tom Conte), April 9, 2001.
- T2. "Region-based Caching," given at the Department of Computer Science, Johns Hopkins University (Hosts: Prof. Jonathan Shapiro and Prof. Gerald Masson), April 13, 2001.
- T3. "Region-based Caching," given at the Department of Computer Science, University of Illinois at Urbana-Champaign (Host: Prof. Sarita Adve), May 2, 2001.
- T4. "Region-based Caching," given at IBM T.J. Watson Research Center (Host: Dr. Pradip Bose), May 6, 2002.
- T5. "Region-based Caching," given at the School of Electrical and Computer Engineering, Georgia Institute of Technology, (Host: Prof. Doug Blough), May 30, 2002.
- T6. "Predicate-Aware Scheduling: A Technique for Reducing Resource Constraints," given at the Department of Electrical and Computer Engineering, North Carolina State University (Host: Prof. Tom Conte), April 21, 2003.
- T7. "High-frequency Inductive Noise Aware Processor Design," at the Intel Architecture Design and CAD Symposium, Intel Corporation (Host: Dr. Jeff Parkhurst), Santa Clara, California, August 23, 2006.
- T8. "Introspective Multi-core Architecture for Secure, Revivable Services," the Intel Pittsburgh Labs and Carnegie Mellon University (Host: Dr. Shimin Chen and Prof. Todd Mowry), Pittsburgh, Pennsylvania, September 22, 2006.
- T9. "Career Path Series: Which path will you follow," at the University of Michigan, Ann Arbor, Michigan, (Host: Associate Dean of Engineering: Prof. Stella Pang,) Jan 18, 2007.
- T10. "Secure Processing On-Chip," at the *Army Research Office Planning Workshop on Embedded System and Network Security* (Host: Prof. Peng Ning and Dr. Cliff Wang), Raleigh, North Carolina, February 22, 2007.
- T11. "High Performance 3D Microarchitecture Design," at IBM Austin Research Labs (Host: Dr. Kevin Nowka), Austin, TX, July 10, 2007.
- T12. "The Chronicles of Microprocessor Architectures — the Transistors, Heat and Challenges," at the National Chang Hua University of Education (Host: Prof. Tsung-Lin Cheng), Chang-Hua, Taiwan, December 13, 2007.
- T13. "The Chronicles of Microprocessor Architectures — the Transistors, Heat and Challenges," at the National University of Tainan (Host: Prof. Been-Chian Chien), Tainan, Taiwan, December 19, 2007.
- T14. "POD: A Heterogeneous Many-Core Platform Using a 3D-Integrated Acceleration Layer," at the National Chiao-Tung University (Host: Profs. Wei-Chung Hsu and Chung-Ping Chung), Hsin-Chu, Taiwan, December 20, 2007.
- T15. "3D-IC Microarchitecture," at the Fukuoka Institute of System LSI Design Industry and Kyushu University (Host: Prof. Koji Inoue), Fukuoka, Japan, June 12, 2008.
- T16. "3D Integration," at the SoC Technology Center, Industrial Technology Research Institute (ITRI), (Host: Prof. Cheng-wen Wu), Hsin-chu, Taiwan, January 22, 2009.
- T17. "Is 3D really a viable next step?" an invited panelist in the *Workshop on 3D Integration and Interconnect-Centric Architectures in conjunction with the 15th International Symposium on High Performance Computer Architecture (HPCA-15)*. Session Chair: Erun Kursun (IBM Research).
- T18. "3D Integration," at the Department of Computer Science and Information Engineering, National University of Kaohsiung, (Host: Prof. Tang-Kai Yin), Kaohsiung, Taiwan, May 21, 2009.

- T19. "3D Integration," at the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, (Host: Prof. Jiang Xu), Hong Kong, May 29, 2009.
- T20. "3D Integration," at the Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, June 2, 2009.
- T21. "3D Integration," at the Department of Industrial Systems Engineering, Asian Institute of Technology, (Host: Profs. Manukid Parnichkun and Mongkol Ekpanyapong), Bangkok, Thailand, June 11, 2009.
- T22. "3D Integration," at the Department of Computer Science and Information Engineering, National Central University, (Host: Prof. Jehn-Ruey Jiang), Chung-Li, Taiwan, June 17, 2009.
- T23. "3D Integration," at the Department of Electrical Engineering, National Cheng-Kung University, (Host: Prof. Chu-Sing Yang), Tainan, Taiwan, June 18, 2009.
- T24. "3D Integration," at the Institute of Information Science, Academia Sinica, (Host: Director Pen-Chung Yew), Taipei, Taiwan, October 22, 2009.
- T25. "3D Integration: the Challenge and Opportunities in Many-core Architecture and Physical Design," at *the 4th IMPACT 2009 & International 3D IC Conference* (Host: Semiconductor Industry Promotion Office, IDB, Ministry of Economic Affairs, Taiwan), Taipei, Taiwan, October 23, 2009.
- T26. "How Do We Scale the Bandwidth Wall," an invited panelist at *the 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI) in conjunction with the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA-16)*. Moderator: Partha Kundu (Intel).
- T27. "Design Space of Phase-Change Memory," at *the Intel Memory Hierarchy Workshop*, Intel Corporation, (Host: Dr. Shih-Lien Lu), Hillsboro, Portland, OR, January 22, 2010.
- T28. "3D Integration," Departmental Colloquium speaker at the Computer & Information Science & Engineering Department, (Host: Dr. Jih-Kwon Peir) University of Florida, Gainesville, FL, March 5, 2010.
- T29. "So Little Bandwidth, So Many Memories," an invited panelist at *the Workshop on Architecting Memory Technologies (WAMT) in conjunction with the 15th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XV)*. Organizer: Shih-Lien Lu (Intel), Pittsburgh, PA, March 14, 2010.
- T30. "3D Integration," a Graduate Seminars speaker at the Electrical & Computer Engineering Department, (Host: Prof. Jun Yang), University of Pittsburgh, Pittsburgh, PA, March 17, 2010.
- T31. "Peeling the Power Onion," an invited panelist at *the 6th Workshop on High Performance, Power-Aware Computing in conjunction with the 24th Annual International Parallel & Distributed Processing Symposium (IPDPS)*. Organizer: Karsten Schwan (Georgia Tech), Atlanta, GA, April 19, 2010.
- T32. "3D Integration," Distinguished Lecture, at the Computer Science Education Department, Korea University, (Host: Prof. Taeweon Suh), Seoul, South Korea, June 1, 2010.
- T33. "Putting Phase Change Memory into Practice for Main Memory," at the Computer Science Departmental Seminar, Korea University, Seoul, South Korea, June 11, 2010.
- T34. "Design, Implementation, and Test for a 3D-IC Many-Core Processor," at *the 10th International Forum on Embedded MPSoC and Multicore*, Gifu city, Gifu, Japan, July 2, 2010.
- T35. "3D Integration," at the College of EECS, National Taiwan University, (Host: Prof. Andy Wu), Taipei, Taiwan, July 14, 2010.
- T36. "Putting Phase Change Memory into Practice for Main Memory," at the Information and Communications Research Laboratories, Industrial Technology Research Institute (ITRI), (Host: Dr. Yuan-Hua Chu), Hsinchu, Taiwan, July 16, 2010.
- T37. "3D Integration," at the Taiwan Semiconductor Manufacturing Corporation (TSMC), (Host: Ken Lin), Hsinchu, Taiwan, July 23, 2010.
- T38. "More than Moore: Can 3D-SICs Continue the Fad and How?" at *the Embedded Software Consortium* (General Chair: Prof. Jenq-Kuen Lee), Hsinchu, Taiwan, October 15, 2010.

- T39. "Design, Implementation, and Test for a 3D-IC Many-Core Processor," at *the IMAPCT 2010 International 3D IC Conference* (Host: Semiconductor Industry Promotion Office, IDB, Ministry of Economic Affairs, Taiwan), Taipei, Taiwan, October 21, 2010.
- T40. "Architecture, Design, and Implementation for a 3D-IC Many-Core Processor," at the IBM Thomas J. Watson Research Center (Hosts: Dr. Valentina Salapura and Dr. Viji Srinivasan), Yorktown Heights, NY, November 4, 2010.
- T41. "Architecture, Design, and Implementation for a 3D-IC Many-Core Processor," an invited talk at National Tsinghua University, (Host: Prof. Young-Long Steve Lin), Hsin-Chu, Taiwan, December 27, 2010.
- T42. "Architecture, Design, and Implementation for a 3D-IC Many-Core Processor," at the Taiwan Semiconductor Manufacturing Company (TSMC), (Host: Dr. Chih-Hang Tung), Hsin-Chu, Taiwan, December 30, 2010.
- T43. "Processor Architecture Design and Implementation Using 3D Integration Technology," at the Electronics Engineering Department, National Chiao-Tung University, (Host: Prof. Ching-Te Kent Chuang), Hsin-Chu, Taiwan, March 1, 2011.
- T44. "Putting Phase-Change Memory (PCM) into Practice for Memory Hierarchy," at the Electrical Engineering Department, National Cheng-Kung University, (Host: Prof. Chung-Ho Chen), Taiwan, Taiwan, March 4, 2011.
- T45. "Making Storage-Class Memory Practical in Future Memory Hierarchy," an invited talk for Hot Topics on Design and Test of 3D and Emerging Memories, *the 29th IEEE VLSI Test Symposium*, Data Point, CA, May 4, 2011.
- T46. "Toward the Design of Robust and Self-Healing Memories," at *the 11th International Forum on Embedded MPSoC and Multicore*, Beaune, France, July 4, 2011.
- T47. "Heterogeneous Die Stacking of SRAM Row Cache and 3-D DRAM: An Empirical Design Evaluation," an invited paper at *the 54th IEEE International Midwest Symposium on Circuits and Systems*, Seoul, Korea, August, 9, 2011.
- T48. "Toward the Design of Robust and Self-Healing Memories," at Korea University (Host: Prof. Sung Woo Chung), Seoul, Korea, August 9, 2011.
- T49. "Toward the Design of Robust and Self-Healing Memories," at the Department of the Electrical Engineering, National Taiwan University (Hosts: Prof. Chien-Mo Li and Dr. Yen-Kuang Chen of Intel-NTU), Taipei, Taiwan, October 5, 2011.
- T50. "Design and Implementation of a Many-Core Processor Using 3-D Integration Technology," at Rambus Inc. (Host: Dr. Trung Diep), Sunnyvale, CA, Nov 16, 2011.

Invention Disclosure

- P1. Hsien-Hsin Lee, Vladimir Pentkovski, and Hsien-Cheng Hsieh, "Pipelined processing of short data streams using data prefetching." US patent number 6,223,276, issued April 24, 2001.
- P2. Vladimir Pentkovski, Hsien-Cheng Hsieh, Hsien-Hsin Lee, and Maiyuran Subramaniam, "Efficient utilization of write-combining." US patent number 6,356,270, issued March 12, 2002.
- P3. Vladimir Pentkovski, Deep Buch, Michael Dwyer, Hsien-Hsin Lee, and Hsien-Cheng Hsieh, "Processing normalized meshes using mesh pool window," US patent number 6,369,813, issued April 9, 2002.
- P4. Salvador Palanca, Niranjan Cooray, Angad Narang, Vladimir Pentkovski, Steve Tsai, Subramaniam Maiyuran, Jagannath Keshava, Hsien-Hsin Lee, Steve Spangler, Suresh Kuttuva, and Praveen Mosur, "Method and apparatus for Prefetching data into cache," US patent number 6,643,745, November 4, 2003.

UNIVERSITY SERVICE

Regular Departmental Service

- ECE Graduate Committee Member, 2003 - 2004.
- ECE Seminar Committee Member, 2004 - 2005.
- ECE Student-Faculty Committee Member, 2005 - 2006.
- ECE Undergraduate Committee Member, 2006 - 2007.
- ECE Graduate Student Recruiting Chair for Computer Engineering Program, 2007 - 2009.
- ECE Undergraduate Committee Member, 2009 - 2010.
- ECE Faculty Recruiting Committee Member, 2010 - Present.

Appointed Service

- Search Committee Member for the *Rhesa "Ray" S. Farmer, Jr. Distinguished Chair in Embedded Computer Systems*, 2006.
- Chair of the Computer Engineering Curriculum Subcommittee, October 2009 - 2011.
- Search Committee Member for ECE School Chair, 2011 - Present.

PROFESSIONAL SERVICE

Editorial Boards

- Associate Editor, *International Journal of Embedded Systems*, 2004 - Present.
- Associate Editor, *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, 2009 - Present.
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2010 - Present.
- Guest co-Editor, *The Computer Journal, Special Issue on Architecture/OS Support for Embedded Multi-Core Systems*, 2010.
- Associate Editor, *Journal of Information Science and Engineering (JISE)*, Academia Sinica, 2011 - Present.
- Guest co-Editor, *Active and Passive Electronic Components, special issue on Design Automation and Test of 3D-SIC*, 2011.

Book Reviewed

- Alan B. Marcovitz, *Introduction to Logic Design*, Second Edition. McGraw Hill. 2005, 2006.
- Umakishore Ramachandran and William D. Leahy, Jr. *Computer Systems: An Integrated Approach to Architecture and Operating Systems*, First Edition, Addison-Wesley, 2007.
- Daniel Page. *A Practical Introduction to Computer Architecture*, Cambridge University, 2006.
- Jean-Loup Baer. *Microprocessor Architecture*. Cambridge Press, 2009.

Conference/Workshop Organizers

- Workshop Co-Chair, *The Workshop on Introspective Architectures (WISA '06)*, Austin, TX, 2006.
- Workshop and Tutorial Chair, *The 39th IEEE/ACM International Symposium on Microarchitecture (MICRO-39)*, Orlando, FL, 2006.
- Special Sessions Chair, *IFIP International Conference on Very Large Scale Integration (VLSI-SoC)*, Atlanta, GA, 2007.

- Program Co-chair, *Workshop of Computer Architecture, SoC, and Embedded Systems, The 2008 International Computer Symposium*, Tamkang University, Damsui, Taipei County, Taiwan, 2008.
- Audio/Video Co-chair, *Embedded System Week (ESWEEK)*, Atlanta, GA, 2008.
- Track chair of VLSI Circuits and Architecture, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Tampa, FL, 2009
- Registration Chair, *the 42nd International Symposium on Microarchitecture (MICRO-42)*, New York City, 2009.
- Tutorial and Workshop Chair, *the 43rd International Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, 2010.
- Workshop Co-Organizer, *Invited Workshop on Technology-Architecture Interaction: Emerging Technologies and their Impact on Computer Architecture, in conjunction with MICRO-43*, Atlanta, GA, 2010.
- General Chair, *the IEEE International Symposium on Workload Characterization (IISWC 2010)*, Atlanta, GA, 2010.
- Steering Committee, *the IEEE International Symposium on Workload Characterization (IISWC 2011)*, Austin, TX, 2011.
- Student Travel Grant/Award Chair, *the 39th ACM/IEEE International Symposium on Computer Architecture (ISCA-39)*, Portland, OR, 2012.

Technical Program Committee

- Program Committee Member, *the ACM/IEEE International Conference on Compilers, Architectures, Synthesis for Embedded Systems (CASES-2004)*, Washington D.C., 2004.
- Program Committee Member, *International Conference on Embedded and Ubiquitous Computing (EUC-04)*, Aizu, Japan, August, 2004.
- Program Committee Member, *Workshop on Compilers and Tools for Constrained Embedded Systems (CTCES 2004)*, Washington D.C., 2004.
- Program Committee Member, *International Conference on Embedded Software and Systems (ICESS'04)*, Hangzhou, China, 2004.
- Program Committee Member, *International Workshop on Parallel & Distributed Embedded Systems (PDES-05)*, Fukuoka Institute of Technology, Japan, 2005.
- Program Committee Member, *IEEE International System-On-Chip Conference (SOCC-05)*, Washington D.C., 2005.
- Program Committee Member, *ACM/IEEE International Conference on Compilers, Architectures, Synthesis for Embedded Systems (CASES-2005)*, San Francisco, CA, 2005.
- Program Committee Member, *IEEE International Conference on Computer Design (ICCD-2005)*, San Jose, CA 2005.
- Program Committee Member, *Workshop on Compilers and Tools for Constrained Embedded Systems (CTCES 2005)*, San Francisco, 2005.
- Program Committee Member, *International Conference on Embedded Software and Systems (ICESS'05)*, Xian, P.R.China 2005.
- Program Committee Member, *Workshop on Interaction between Operating System and Computer Architecture (IOSCA-05)*, Austin, TX, 2005.
- Program Committee Member, *The 12th International Conference on Parallel and Distributed Systems (ICPADS-06)*, Minneapolis, MN, 2006.
- Program Committee Member, *2006 IFIP International Conference on Embedded and Ubiquitous Computing (EUC'06)*, Seoul, Korea, 2006.

- Program Committee Member, *IEEE International System-On-Chip Conference (SOCC-06)*, Austin, Texas, 2006.
- Program Committee Member, *The 33rd ACM/IEEE International Symposium on Computer Architecture (ISCA-33)*, Boston, MA, 2006.
- Program Committee Member, *Workshop on Interaction between Operating System and Computer Architecture (WIOSCA-06)*, Boston, MA, 2006.
- Program Committee Member, *ACM/IEEE International Conference on Compilers, Architectures, Synthesis for Embedded Systems (CASES-2006)*, Seoul, Korea, 2006.
- Program Committee Member, *IEEE International Conference on Computer Design (ICCD-2006)*, San Jose, CA 2006.
- Program Committee Member, *The 13th IEEE International Conference on High Performance Computer Architecture (HPCA-13)*, Phoenix, Arizona, 2007.
- Program Committee Member, *The ACM International Conference on Computing Frontiers (CF-07)*, Ischia, Italy, 2007.
- Program Committee Member, *The 13th International Conference on Parallel and Distributed Systems (ICPADS'07)*, Hsinchu, Taiwan, 2007.
- Program Committee Member, *2007 International Workshop on Embedded Software Optimization (ESO-2007)*, Taipei, Taiwan, 2007.
- Program Committee Member, *Workshop on Interaction between Operating System and Computer Architecture (WIOSCA-07)*, San Diego, CA, 2007.
- Program Committee Member, *ACM/IEEE International Conference on Compilers, Architectures, Synthesis for Embedded Systems (CASES-2007)*, Salzburg, Austria, 2007.
- Program Committee Member, *IEEE International Conference on Computer Design (ICCD-2007)*, Lake Tahoe, CA 2007.
- Program Committee Member, *IEEE International System-On-Chip Conference (SOCC-07)*, Hsinchu, Taiwan, 2007.
- Program Committee Member, *IFIP International Conference on Very Large Scale Integration (VLSI-SoC)*, Atlanta, GA, 2007.
- Program Committee Member, *The ACM International Conference on Computing Frontiers (CF-08)*, Ischia, Italy, 2008.
- Program Committee Member, *The 12th Annual Workshop on Interaction between Compilers and Computer Architecture (INTERACT-12)*, Salt Lake City, Utah, 2008
- Program Committee Member, *The 35th ACM/IEEE International Symposium on Computer Architecture (ISCA-35)*, Beijing, China, 2008.
- Program Committee Member, *IEEE International System-On-Chip Conference (SOCC-08)*, Newport Beach, CA, 2008.
- Program Committee Member, *ACM/IEEE International Conference on Compilers, Architectures, Synthesis for Embedded Systems (CASES-2008)*, Atlanta, GA, 2008.
- Program Committee Member, *IEEE International Conference on Computer Design (ICCD-2008)*, Squaw Creek, Lake Tahoe, CA, 2008.
- Program Committee Member, *The 12th Annual Workshop on Interaction between Compilers and Computer Architecture (INTERACT-13)*, Raleigh, NC, 2009.
- Program Committee Member, *IEEE International System-On-Chip Conference (SOCC-09)*, Belfast, Northern Ireland, 2009.
- Program Committee Member, *The 23rd International Conference on Supercomputing (ICS'09)*, IBM T. J. Watson Research Center, Metro New York City Area, 2009.

- Program Committee Member, *Workshop on 3D Integration and Interconnect-Centric Architectures, held in conjunction with International Symposium on High Performance Computer Architecture*, Raleigh, North Carolina, 2009.
- Program Committee Member, *IEEE International System-On-Chip Conference (SOCC-09)*, Montgomery Village, MD, 2009.
- External Review Committee Member. *The 36th ACM/IEEE International Symposium on Computer Architecture (ISCA-36)*, Austin, Texas, 2009.
- Program Committee Member, *The 2009 International Symposium on Workload Characterization (IISWC 2009)*, Austin, Texas, 2009.
- Program Committee Member, *2009 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA 2009), in conjunction with the 36th International Symposium on Computer Architecture (ISCA-36)*, Austin, Texas, 2009.
- Program Committee Member, *IEEE International Conference on Computer Design (ICCD-2009)*, Squaw Creek, Lake Tahoe, CA, 2009.
- Program Committee Member, *Workshop on Biomedicine in Computing: Systems, Architectures, and Circuits (BiC) in conjunction with the 36th International Symposium on Computer Architecture (ISCA-36)*, Austin, Texas, 2009.
- Poster Committee Member, *IEEE Parallel Architecture and Compilation Techniques (PACT-18)*, Raleigh, North Carolina, 2009.
- Program Committee Member, *IFIP International Conference on Very Large Scale Integration (VLSI-SoC)*, Florianopolis, Brazil, 2009.
- Program Committee Member, *2009 Cross Strait Information Technology Conference (CSIT)*, Chung-Li, National Central University, Taiwan, 2009.
- Program Committee Member, *The 23rd International Conference on VLSI Design*, Bangalore, India, 2010.
- Program Committee Member, *IEEE MICRO Top Picks*, 2010.
- Program Committee Member, *The IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Lixouri Kefalonia, Greece, 2010.
- Program Committee Member, *The 14th Annual Workshop on Interaction between Compilers and Computer Architecture (INTERACT-14)*, Pittsburgh, PA, 2010
- Program Committee Member, *Workshop of Computer Architecture, SOC and Embedded Systems, International Computer Symposium*, Tainan, Taiwan, 2010.
- Program Committee Member, *The 43rd International Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, 2010.
- Program Committee Member, *Workshop on Microarchitectural Support for Virtualization, Data Center Computing, and Clouds (MASVDC) in conjunction with MICRO-43*, Atlanta, GA, 2010.
- Program Committee Member, *IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (3D-TEST) in conjunction with International Test Conference (ITC) / Test Week 2010*, Austin, Texas, 2010.
- Program Committee Member, *The 26th ACM Symposium on Applied Computing, Track on Green/Power-Aware Design and Optimization*, Taichung, Taiwan, 2011.
- Program Committee Member, *ACM Annual Symposium on Parallelism in Algorithms and Architectures (SPAA)*, San Diego, 2011.
- Program Committee Member, *The 3rd Asia Symposium on Quality Electronic Design (ASQED 2011)*, Kuala Lumpur, Malaysia, 2011.

- Program Committee Member, *The Workshop on Emerging Supercomputing Technologies (WEST)*, in conjunction with the *25th International Conference on Supercomputing (ICS-2011)*, Tucson, Arizona, 2011.
- Program Committee Member, *IEEE International Conference on Computer Design (ICCD-2011)*, University of Massachusetts, Amherst, MA, 2011.
- Program Committee Member, *IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (3D-TEST) in conjunction with International Test Conference (ITC)*, Anaheim, CA, 2011.
- Program Committee Member, *The 17th Asia and South Pacific Design Automation Conference (ASP-DAC 2012)*, Sydney, Australia, 2012.
- Program Committee Member, *The ACM International Conference on Computing Frontiers (CF-2012)*, Cagliari, Italy, 2012.
- Program Committee Member, *The 39th ACM/IEEE International Symposium on Computer Architecture (ISCA-39)*, Portland, OR, 2012.
- Program Committee Member, *The 26th International Conference on Supercomputing (ICS)*, San Servolo Island, Venice, Italy, 2012.