

Curriculum Vitae

Sung Kyu Lim

Associate Professor

School of Electrical and Computer Engineering

Georgia Institute of Technology

September 9, 2009

I. Earned Degrees

1. BS: University of California at Los Angeles, Computer Science Department (1994)
2. MS: University of California at Los Angeles, Computer Science Department (1997)
3. PhD: University of California at Los Angeles, Computer Science Department (2000)

II. Employment

1. Research Assistant, UCLA VLSI CAD Lab (September 1995 – June 2000)
2. Post Doctoral Scholar, UCLA VLSI CAD Lab (September 2000 – June 2001)
3. Senior Engineer, Aplus Design Technologies, Inc. (June 2000 – June 2001)
4. Visiting Scholar, School of Electrical Engineering and Computer Science, Seoul National University (June 2001 – August 2001)
5. Assistant Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (August 2001 – June 2007)
6. Associate Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (July 2007 – current)
7. Instructor, Department of Computer Science, Korea University (May 2007 – August 2007, May 2008 – August 2008, May 2009 – August 2009)
8. Instructor, Department of Electrical Engineering, Korean Advanced Institute of Science and Technology (June 2007 – July 2007)

III. Teaching

III.A. Individual Student Guidance

III.A.1. Graduated PhD Students

1. Mongkol Ekpanyapong: passed preliminary exam in October 2001, proposal exam in April 2005, and defense in November 2005. Thesis: “Microarchitecture-Aware Physical Planning for Deep Submicron Technology”. Currently an Assistant Professor at the Asian Institute of Technology, Thailand.

2. Jacob Minz: passed preliminary exam in October 2002, proposal exam in October 2005, and defense in July 2006. Thesis: “Physical Design Automation for System-on-Packages (SOP) and 3D-ICs”. Currently with Synopsys Corporation.
3. Ismail Faik Baskaya: passed preliminary exam in November 2003, proposal exam in December 2006, and defense in July 2009. Thesis: “Physical Synthesis for Field Programmable Analog Array”. Currently an Assistant Professor at Bogazici University, Turkey.

III.A.2. PhD Students

1. Michael Healy: passed preliminary exam in November 2004. Thesis: “Microarchitectural Design Space Exploration”
2. Mohit Pathak: passed preliminary exam in November 2005. Thesis: “Embedded Passive Placement and Routing for RF Designs”
3. Dae Hyun Kim: passed preliminary exam in March 2006. Thesis: “Bus Routing for 2D/3D Microarchitectural Designs”
4. Xin Zhao: passed preliminary exam in March 2007. Thesis: “Variation-tolerant Designs for 3D Integrated Circuits”
5. Young Joon Lee: passed preliminary exam in November 2007. Thesis: “Design Space Exploration for Package-aware 3D Stacked IC”
6. Krit Athikulwongse: passed preliminary exam in November 2001. Thesis: “Low Power Clock Tree Designs for 3D Integrated Circuits”
7. Chang Liu
8. Moongon Jung

III.A.3. Graduated MS Thesis Students

1. Pun Hang Shiu: graduated in December 2003. Thesis: Floorplanning for 3D System-On-Package.
2. Jean Nguyen: graduated in June 2004. Thesis: Partitioning for Quantum Cell Automata-based Circuits.
3. Ramprasad Ravichandran: graduated in June 2005. Thesis: Placement for Quantum Cell Automata-based Circuits.
4. Eric Wong: graduated in August 2006. Thesis: Physical Design for 3D Stacked ICs.
5. Ye Tao: graduated in August 2008. Thesis: Power Supply Noise-aware Floorplanning.

III.B. Other Teaching Activities

III.B.1. New Graduate Course Development

Physical Design Automation of VLSI Systems: This course was offered in Summer 2002, Fall 2003, and Spring 2005 as a special topics course and became a permanent graduate course (ECE6133) in the School of Electrical and Computer Engineering.

- Description: The objective of physical design automation is to transform a structural representation of a VLSI system into a layout representation so that the resulting layout satisfies topological, geometric, timing, and power-consumption constraints of the design. This course focuses on various design automation problems in the physical design process of VLSI circuits, including: logic partitioning, floorplanning, global routing, detailed routing, compaction, and performance-driven layout. In addition, the discussion of a number of important optimization techniques, such as network flow, Steiner tree, scheduling, simulated annealing, generic algorithm, and linear/convex programming are included.

- Motivation: A significant portion of today’s VLSI chips is designed with automatic layout generation tools. This is the first course ever offered at the Georgia Institute of Technology that teaches VLSI layout automation.

IV. Scholarly Accomplishments

IV.A. Published Books and Parts of Books

1. Sung Kyu Lim and Mike Niemier, “Partitioning and Placement for Buildable QCA Circuits,” in *Nano, Quantum and Molecular Computing: Implications to High Level Design and Validation*, edited by Sandeep Shukla and Iris Bahar, Springer, pp 295-316, June 2004. ISBN: 1-4020-8067-0
2. Sung Kyu Lim, “Practical Problems in VLSI Physical Design Automation,” Springer, July 2008. ISBN: 978-1-4020-6626-9.
3. Sung Kyu Lim, “Efficient On-Chip Power, Clock, Thermal, and Signal Delivery for 3D Multi-core Systems,” in *Three Dimensional System Integration: IC Stacking Process and Design*, edited by Antonis Papanikolaou, Dimitrios Soudris and Riko Radojcic, Springer, June 2009.

IV.B. Refereed Publications

IV.B.1. Refereed Journal Publications

1. Jason Cong and Sung Kyu Lim, “Edge Separability based Circuit Clustering With Application to Multi-level Circuit Partitioning,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 3, pp. 346–357, 2004.
2. Jason Cong and Sung Kyu Lim, “Retiming-based Timing Analysis With An Application to Mincut-based Global Placement,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 12, pp. 1684-1692, 2004.
3. Ramprasad Ravichandran, Sung Kyu Lim, and Michael Niemier, “Automatic Cell Placement for Quantum-dot Cellular Automata,” *Integration, the VLSI Journal*, Vol. 38, No. 3, pp. 541-548, 2005.
4. Sung Kyu Lim, Ramprasad Ravichandran, and Mike Niemier, “Partitioning and Placement for Buildable QCA Circuits,” *ACM Journal on Emerging Technologies in Computing Systems*, Vol. 1, No. 1, pp. 50–72, 2005.
5. Sung Kyu Lim, “Physical Design for 3D System-On-Package: Challenges and Opportunities,” *IEEE Design & Test of Computers*, Vol. 22, No. 6, pp. 532–539, 2005.
6. Peter Sassone and Sung Kyu Lim, “Traffic: A Novel Geometric Algorithm For Fast Wire-Optimized Floorplanning,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 6, pp. 1075–1086, 2006.
7. Mongkol Ekpanyapong, Jacob Minz, Thaisiri Watwai, Hsien-Hsin S. Lee, and Sung Kyu Lim, “Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 7, pp. 1289–1300, 2006.
8. Eric Wong, Jacob Minz, and Sung Kyu Lim, “Thermal and Power Integrity-aware Module Placement For 3D System-On-Package,” *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 14, No. 5, pp. 553–557, 2006.
9. Faik Baskaya, Sasank Reddy, Sung Kyu Lim, and David Anderson, “Placement for Large-Scale Floating-Gate Field-Programable Analog Arrays,” *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 14, No. 8, pp. 906–910, 2006.

10. Jacob Minz, Eric Wong, Mohit Pathak, and Sung Kyu Lim, “Placement and Routing for 3D System-On-Package Designs,” *IEEE Transactions on Components and Packaging Technologies*, Vol. 29, No. 3, pp. 644–657, 2006.
11. Jacob Minz and Sung Kyu Lim, “Block-level 3D Global Routing With an Application to 3D Packaging,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, pp. 2248–2257, 2006.
12. Wook-Jin Chung, Brian Smith, and Sung Kyu Lim, “Node Duplication and Routing Algorithms for Quantum-dot Cellular Automata Circuit,” *IEE Proceedings on Circuits, Devices & Systems*, Vol. 153, No. 5, pp. 497–505, 2006.
13. Mongkol Ekpanyapong, Michael Healy, and Sung Kyu Lim, “Profile-Driven Instruction Mapping for Dataflow Architectures,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 12, pp. 3017–3025, 2006.
14. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, “Multi-Objective Microarchitectural Floorplanning For 2D And 3D Stacked ICs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 1, pp. 38–52, 2007.
15. Jacob Minz, Somaskanda Thyagaraja, and Sung Kyu Lim, “Optical Routing for 3D System-On-Package,” *IEEE Transactions on Components and Packaging Technologies*, Vol. 30, No. 4, pp. 805–812, 2007.
16. Eric Wong, Jacob Minz, and Sung Kyu Lim, “Decoupling Capacitor Planning and Sizing for Noise and Leakage Reduction,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 11, pp. 2023–2034, 2007.
17. Faik Baskaya, David V. Anderson, and Sung Kyu Lim, “Net Sensitivity Based Optimization of Large-scale Field Programmable Analog Array (FPAA) Placement and Routing,” *IEEE Transactions on Circuits and Systems II*, Vol. 56, No. 7, pp. 565–569, 2009.
18. Mohit Pathak and Sung Kyu Lim, “Performance and Thermal-aware Steiner Routing for 3D Stacked ICs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 28, No. 9, pp. 1373–1386, 2009.
19. Yoon Jo Kim, Yogendra K. Joshi, Andrei G. Fedorov, Young-Joon Lee, and Sung Kyu Lim, “Thermal Characterization of Interlayer Microfluidic Cooling of Three-Dimensional IC with Non-Uniform Heat Flux,” *ASME Journal of Heat Transfer*, 2009.

IV.B.2. Refereed Conference Publications

1. Jason Cong, Peter Li, Sung Kyu Lim, Toshiyuki Shibuya, and Dongmin Xu, “Large Scale Circuit Partitioning With Loose/Stable Net Removal and Signal Flow Based Clustering,” *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 441–446, 1997.
2. Jason Cong and Sung Kyu Lim, “Multiway Partitioning With Pairwise Movement,” *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 512–516, 1998.
3. Maogang Wang, Sung Kyu Lim, Jason Cong, and Majid Sarrafzadeh, “Multi-way Partitioning Using Bi-partition Heuristics,” *Proceedings of the IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 667–672, 2000.
4. Jason Cong and Sung Kyu Lim, “Performance Driven Multiway Partitioning,” *Proceedings of the IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 441–446, 2000.
5. Jason Cong and Sung Kyu Lim, “Edge Separability-based Circuit Clustering With Application to Circuit Partitioning,” *Proceedings of the IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 429–434, 2000.

6. Jason Cong, Sung Kyu Lim, and C. Wu, “Performance Driven Multi-level and Multiway Partitioning With Retiming,” *Proceedings of the ACM Design Automation Conference*, pp. 274–279, 2000.
7. Jason Cong and Sung Kyu Lim, “Physical Planning with Retiming,” *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 2–7, 2000.
8. Peter Sassone and Sung Kyu Lim, “A Novel Geometric Algorithm for Fast Wire-Optimized Floorplanning,” *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 74–80, 2003.
9. Jacob Minz and Sung Kyu Lim, “Layer Assignment for System on Packages,” *ACM/IEEE Asia and South Pacific Design Automation Conference*, pp. 31–37, 2004.
10. Mongkol Ekpanyapong and Sung Kyu Lim, “Performance-driven Global Placement via Adaptive Network Characterization,” *ACM/IEEE Asia and South Pacific Design Automation Conference*, pp. 137–142, 2004.
11. Jacob Minz, Mohit Pathak, and Sung Kyu Lim, “Net and Pin Distribution for 3D Package Global Routing,” *Design, Automation and Test in Europe*, pp. 1410–1411, 2004.
12. Ramprasad Ravichandran, Jacob Minz, Mohit Pathak, Siddharth Easwar, and Sung Kyu Lim, “Physical Layout Automation for System-On-Packages,” *IEEE Electronic Components and Technology Conference*, pp. 41–48, 2004.
13. Mongkol Ekpanyapong, Karthik Balakrishnan, Vidit Nanda, and Sung Kyu Lim, “Simultaneous Delay and Power Optimization for Multi-level Partitioning and Floorplanning with Retiming,” *IEEE International Symposium on Circuits and Systems*, pp. 57–60, 2004.
14. Pun Hang Shiu, Ramprasad Ravichandran, Siddharth Easwar, and Sung Kyu Lim, “Multi-layer Floorplanning for Reliable System-on-Package,” *IEEE International Symposium on Circuits and Systems*, pp. 69–72, 2004.
15. Ramprasad Ravichandran, Nihal Ladiwala, Jean Nguyen, Mike Niemier, and Sung Kyu Lim, “Automatic Cell Placement for Quantum-dot Cellular Automata,” *ACM Great Lake Symposium on VLSI*, pp. 332–337, 2004.
16. Mongkol Ekpanyapong, Jacob Minz, Thaisiri Watwai, Hsien-Hsin S. Lee, and Sung Kyu Lim, “Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design,” *ACM Design Automation Conference*, pp. 634–639, 2004.
17. Jacob Minz, Sung Kyu Lim, Jinwoo Choi, and Madhavan Swaminathan, “Module Placement for Power Supply Noise and Wire Congestion Avoidance in 3D Packaging,” *IEEE Electrical Performance of Electronic Packaging*, pp. 123–126, 2004.
18. Jacob Minz and Sung Kyu Lim, “A Global Router for System-On-Package Targeting Layer and Crosstalk Minimization,” *IEEE Electrical Performance of Electronic Packaging*, pp. 99–102, 2004.
19. Karthik Balakrishnan, Vidit Nanda, Siddharth Easwar, and Sung Kyu Lim, “Wire Congestion And Thermal Aware 3D Global Placement,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 1131–1134, 2005.
20. Ramprasad Ravichandran, Mike Niemier, and Sung Kyu Lim, “Partitioning and Placement for Buildable QCA Circuits,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 424–427, 2005.
21. Mongkol Ekpanyapong, Michael Healy, and Sung Kyu Lim, “Placement for Configurable Dataflow Architecture,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 1127–1130, 2005.
22. Jacob Minz, Eric Wong, and Sung Kyu Lim, “Thermal and Crosstalk-Aware Physical Design For 3D System-On-Package,” *IEEE Electronic Components and Technology Conference*, pp. 824–831, 2005.

23. Faik Baskaya, Sasank Reddy, Sung Kyu Lim, Tyson Hall, and David V. Anderson, “Mapping Algorithm for Large-scale Field Programmable Analog Array,” *ACM International Symposium on Physical Design*, pp. 152–158, 2005.
24. Mongkol Ekpanyapong, Sung Kyu Lim, Chinnakrishnan Ballapuram, and Hsien-Hsin S. Lee, “Wire-driven Microarchitectural Design Space Exploration,” *IEEE International Symposium on Circuits and Systems*, pp. 1867–1870, 2005.
25. Brian Smith and Sung Kyu Lim, “QCA Channel Routing with Wire Crossing Minimization,” *ACM Great Lake Symposium on VLSI*, pp. 217–220, 2005.
26. Jacob Minz, Sung Kyu Lim, and Cheng-Kok Koh, “3D Module Placement for Congestion and Power Noise Reduction,” *ACM Great Lake Symposium on VLSI*, pp. 458–461, 2005.
27. Wook Jin Chung, Brian Smith, and Sung Kyu Lim, “QCA Physical Design With Crossing Minimization,” *IEEE Conference on Nanotechnology*, pp. 262–265, 2005.
28. Michael Healy, Mongkol Ekpanyapong, and Sung Kyu Lim, “MILP-based Placement and Routing for Dataflow Architecture,” *International Conference on Field Programmable Logic and Applications*, pp. 71–76, 2005.
29. Faik Baskaya, Sasank Reddy, Sung Kyu Lim, and David Anderson, “Hierarchical Placement for Large-scale FPAA,” *International Conference on Field Programmable Logic and Applications*, pp. 421–426, 2005.
30. Jacob Minz, Eric Wong, and Sung Kyu Lim, “Reliability-aware Floorplanning for 3D Circuits,” *IEEE International SOC Conference*, pp. 81–82, 2005.
31. Eric Wong, Jacob Minz, and Sung Kyu Lim, “Power Noise-aware 3D Floorplanning for System-On-Package,” *IEEE Electrical Performance of Electronic Packaging*, pp. 259–262, 2005.
32. Mongkol Ekpanyapong, Thaisiri Watwai, and Sung Kyu Lim, “Statistical Bellman-Ford Algorithm With An Application to Statistical Retiming,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 959–964, 2006.
33. Eric Wong and Sung Kyu Lim, “3D Floorplanning with Thermal Vias,” *Design, Automation and Test in Europe*, pp. 878–883, 2006.
34. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, “Microarchitectural Floorplanning Under Performance and Temperature Tradeoff,” *Design, Automation and Test in Europe*, pp. 1288–1293, 2006.
35. Jacob Minz, Somaskanda Thyagaraja, and Sung Kyu Lim, “Optical Routing for 3D System-On-Package,” *Design, Automation and Test in Europe*, pp. 337–338, 2006.
36. Mongkol Ekpanyapong and Sung Kyu Lim, “Integrated Retiming and Simultaneous Vdd/Vth Scaling for Total Power Minimization,” *ACM International Symposium on Physical Design*, pp. 142–148, 2006.
Nominated for Best Paper Award
37. Eric Wong, Jacob Minz, and Sung Kyu Lim, “White Space Management for Thermal Via and Decoupling Capacitor Insertion Targeting 3D System-On-Package,” *IEEE Electronic Components and Technology Conference*, pp. 1795–1801, 2006.
38. Eric Wong, Jacob Minz, and Sung Kyu Lim, “Decoupling Capacitor Planning and Sizing for Noise and Leakage Reduction,” *IEEE International Conference on Computer-Aided Design*, pp. 395–400, 2006.
39. Fayez Mohamood, Michael Healy, Hsien-Hsin Lee, and Sung Kyu Lim, “A Floorplan Aware Dynamic Inductive Noise Controller for Reliable 2D and 3D Microprocessors,” *IEEE/ACM International Symposium on Microarchitecture*, pp. 3–14, 2006.

40. Mongkol Ekpanyapong, Xin Zhao, and Sung Kyu Lim, “An Efficient Computation of Statistically Critical Sequential Paths Under Retiming,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 547–552, 2007.
41. Fayez Mohamood, Michael Healy, Hsien-Hsin Lee, and Sung Kyu Lim, “Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 786–791, 2007.
42. Faik Baskaya, Brian Gestner, Chris Twigg, Sung Kyu Lim, David V. Anderson, and Paul Hasler, “Rapid Prototyping of Large-scale Analog Circuits with Field Programmable Analog Array,” *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 319–320, 2007.
43. Mohit Pathak and Sung Kyu Lim, “Thermal-aware Steiner Routing for 3D Stacked ICs,” *IEEE International Conference on Computer-Aided Design*, pp. 205–211, 2007.
44. Mohit Pathak, Souvik Mukherjee, Madhavan Swaminathan, Ege Engin, and Sung Kyu Lim, “Placement and Routing of RF Embedded Passive Designs In LCP Substrate,” *IEEE International Conference on Computer Design*, 2007.
45. Eric Wong and Sung Kyu Lim, “Whitespace Redistribution For Thermal Via Insertion In 3D Stacked ICs,” *IEEE International Conference on Computer Design*, 2007.
46. Mohit Pathak, Satya Vadlamudi, Josh Beavers, and Sung Kyu Lim, “Automatic Layout Generation of RF Embedded Passive Designs,” *IEEE Electrical Performance of Electronic Packaging*, pp. 115–118, 2007.
47. Jacob Minz, Xin Zhao, and Sung Kyu Lim, “Buffered Clock Tree Synthesis for 3D ICs Under Thermal Variations,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 504–509, 2008.
48. Dae Hyun Kim and Sung Kyu Lim, “Bus-Aware Microarchitectural Floorplanning,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 204–208, 2008.
49. Michael Healy, Fayez Mohamood, Hsien-Hsin S. Lee, and Sung Kyu Lim, “A Unified Methodology for Power Supply Noise Reduction in Modern Microarchitecture Design,” *IEEE/ACM Asia South Pacific Design Automation Conference*, pp. 611–616, 2008.
50. Dae Hyun Kim and Sung Kyu Lim, “Global Bus Route Optimization with Application to Microarchitectural Design Exploration,” *IEEE International Conference on Computer Design*, pp. 658–663, 2008.
51. Young Joon Lee and Sung Kyu Lim, “Co-Optimization of Signal, Power, and Thermal Distribution Networks for 3D ICs,” *IEEE Symposium on Electrical Design of Advanced Packaging and Systems*, pp. 163–166, 2008.
52. Michael Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, and Sung Kyu Lim, “Thermal Optimization in Multi-Granularity Multi-Core Floorplanning,” *IEEE/ACM Asia South Pacific Design Automation Conference*, 2009.
53. Ye Tao and Sung Kyu Lim, “Decoupling Capacitor Planning With Analytical Delay Model on RLC Power Grid”, *Design, Automation and Test in Europe*, 2009.
54. Young-Joon Lee, Yoon-Jo Kim, Gang Huang, Muhannad Bakir, Yogendra Joshi, Andrei Fedorov, and Sung Kyu Lim, “Co-Design of Signal, Power, and Thermal Distribution Networks for 3D ICs”, *Design, Automation and Test in Europe*, 2009.
55. Michael Healy and Sung Kyu Lim, “A Study of Stacking Limit and Scaling in 3D ICs: an Interconnect Perspective”, *IEEE Electronic Components and Technology Conference*, 2009.
56. Young-Joon Lee and Sung Kyu Lim, “Routing Optimization of Multi-modal Interconnects In 3D ICs”, *IEEE Electronic Components and Technology Conference*, 2009.

57. Young-Joon Lee, Mike Healy, and Sung Kyu Lim, “Co-design of Reliable Signal and Power Interconnects in 3D Stacked ICs,” *IEEE International Interconnect Technology Conference*, 2009.
58. Dae Hyun Kim, Saibal Mukhopadhyay, and Sung Kyu Lim, “TSV-aware Interconnect Length and Power Prediction for 3D Stacked ICs,” *IEEE International Interconnect Technology Conference*, 2009.
59. Yoon Jo Kim, Yogendra K. Joshi, Andrei G. Fedorov, Young-Joon Lee, and Sung Kyu Lim, “Thermal Characterization of Interlayer Microfluidic Cooling of Three-Dimensional IC with Non-Uniform Heat Flux,” *ASME Conference on Nanochannels, Microchannels and Minichannels*, 2009.
60. Dae Hyun Kim, Saibal Mukhopadhyay, and Sung Kyu Lim, “Through-Silicon-Via Aware Interconnect Prediction and Optimization for 3D Stacked ICs,” *ACM/IEEE International Workshop on System Level Interconnect Prediction*, 2009.
61. Jeremy Tolbert, Xin Zhao, Saibal Mukhopadhyay, and Sung Kyu Lim, “Slew-Aware Clock Tree Design For Reliable Subthreshold Circuits,” *IEEE International Symposium on Low Power Electronics and Design*, 2009.
62. Faik Baskaya, David V. Anderson, Paul Hasler, and Sung Kyu Lim, “A Generic Reconfigurable Array Specification and Programming Environment (GRASPER),” *IEEE European Conference on Circuit Theory & Design*, 2009.
63. Young-Joon Lee, Rohan Goel, and Sung Kyu Lim, “Multi-functional Interconnect Co-optimization for Fast and Reliable 3D Stacked ICs,” *IEEE International Conference on Computer-Aided Design*, 2009.
64. Dae Hyun Kim, Krit Athikulwongse, and Sung Kyu Lim, “A Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout,” *IEEE International Conference on Computer-Aided Design*, 2009.
65. Xin Zhao, Dean Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim, “Pre-bond Testable Low-Power Clock Tree Design for 3D Stacked ICs,” *IEEE International Conference on Computer-Aided Design*, 2009.

IV.D. Presentations

IV.D.1. Invited Seminar Presentations in the US

1. “Physical Design Automation for Emerging Technologies,” Xilinx Corporation, San Jose. Invited by Dr. Amit Singh, November 10, 2003.
2. “Physical Design Automation for Fast and Reliable 3D Circuits,” Princeton University, New Jersey. Invited by Prof. Sharad Malik at EE department, May 3, 2006.
3. “Physical Design Automation for Fast and Reliable 3D Circuits,” Intel Corporation, Santa Clara. Invited by Dr. Jeff Parkhurst, August 23, 2006.
4. “Physical Design Automation for Fast and Reliable 3D Circuits,” University of Texas, Austin. Invited by Prof. David Pan at ECE department, March 29, 2007.
5. “Thermal/Power-Aware Physical Design for 3D ICs,” Georgia Institute of Technology, Atlanta. Invited by Prof. Paul Kohl at the Interconnect Focus Center, May 7, 2007.
6. “High Performance 3D Microarchitecture Design,” IBM T. J. Watson Research Center, Yorktown Heights. Invited by Dr. Joel Silberman, Oct 3, 2007.
7. “Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs,” Georgia Institute of Technology, Atlanta. Invited by Prof. Paul Kohl at the Interconnect Focus Center (IFC), August 28, 2008.
8. “Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs,” Workshop on Integrated CAD Tools for Next Generation Thermal Management Methodologies and Devices: Status and Needs, Interconnect Focus Center (IFC), Atlanta. Invited by Prof. Paul Kohl. November 17, 2008.

IV.D.2. Invited Seminar Presentations in Korean Universities

1. “Performance Driven Circuit Partitioning,” Seoul National University (SNU), Seoul. Invited by Prof. Kiyong Choi at EE department, July 3, 2001.
2. “Multi-level Optimization Techniques for the Physical Design Automation of VLSI Systems,” Korean Advanced Institute of Science and Technology (KAIST), Taejeon. Invited by Prof. Incheol Park at EE department, July 9, 2001.
3. “Performance Driven Circuit Partitioning,” Yonsei University, Seoul. Invited by Prof. Moonkey Lee at EE department, July 16, 2001.
4. “Performance Driven Circuit Clustering for VLSI Systems,” Hongik University, Seoul. Invited by Prof. Hayoon Song at CS department, July 18, 2001.
5. “Thermal/Power-Aware Physical Design for 3D ICs,” Sungkyunkwan University (SKKU), Suwon. Invited by Prof. Jun Dong Cho at School of ICE, June 14, 2007.
6. “Physical Design for 3D Integration at the Chip and Package Level,” Yonsei University, Seoul. Invited by Prof. Sang Hyun Park at CS department, July 4, 2007.
7. “Physical Design for 3D Integration at the Chip and Package Level,” Kumoh National Institute of Technology, Gumi. Invited by Prof. Young Hak Kim at EE department, July 9, 2007.
8. “Physical Design for 3D Integration at the Chip and Package Level,” Hongik University, Seoul. Invited by Prof. Hayoon Song at CS department, July 11, 2007.
9. “Physical Design for 3D Integration at the Chip and Package Level,” Seoul National University (SNU), Seoul. Invited by Prof. Ki Young Choi at EE department, July 16, 2007.
10. “Physical Design for 3D Integration at the Chip and Package Level,” Yeungjin College, Daegu. Invited by Prof. Jae Hong Park at EE department, July 23, 2007.
11. “Physical Design for 3D Integration at the Chip and Package Level,” Korean Advanced Institute of Science and Technology (KAIST), Daejeon. Invited by Prof. In Cheol Park at EE department, July 24, 2007.
12. “Physical Design for 3D Integration at the Chip and Package Level,” Inha Technical College, Incheon. Invited by Prof. Dong Sik Kim at EE department, July 30, 2007.
13. “Power and Thermal-aware Architecture, Circuits, and Interconnect Techniques,” Sungkyunkwan University (SKKU), Suwon. Invited by Prof. Dong Ryeol Shin at School of ICE, May 28, 2008.
14. “Power and Thermal-aware Architecture, Circuits, and Interconnect Techniques,” Korean Advanced Institute of Science and Technology (KAIST), Daejeon. Invited by Prof. Hyun Wook Park at EE department, June 10, 2008.
15. “3D Integrated Circuits: Challenges and Opportunities,” Yonsei University, Seoul. Invited by Prof. Sung Bong Yang at CS department, June 10, 2008.
16. “Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory,” Korean Advanced Institute of Science and Technology (KAIST), Daejeon. Invited by Prof. Joungho Kim at EE Department, July 7, 2009.
17. “Fundamentals of VLSI Physical Design with Application to 3D IC Design Automation,” 2-Day Workshop, Seoul National University (SNU), Seoul. Invited by Prof. Ki Young Choi at EE Department, July 9–10, 2009.
18. “Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory,” Sungkyunkwan University (SKKU), Suwon. Invited by Prof. Jun Dong Cho at School of ICE, July 14, 2009.

19. “Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory,” Kumoh National Institute of Technology, Gumi. Invited by Prof. Tae Young Choi at EE department, July 16, 2007.
20. “Fundamentals and Recent Trend of Through-Silicon-Via (TSV) Based 3D Circuit Design,” 2-Day Workshop, Korea University (KU), Seoul. Invited by Prof. Hyuk Yoo at CS Department, July 21–22, 2009.

IV.D.3. Invited Seminar Presentations in Korean Industries

1. “Multi-level Optimization Techniques for the Physical Design Automation of VLSI Systems,” Samsung Semiconductor, Kiheung. Invited by Dr. Kyu Myoung Choi at CAE Team, July 19, 2001.
2. “Physical Design for 3D Integration at the Chip and Package Level,” LG Mobile Handset R&D Center, Seoul. Invited by Dr. Soo Youl Yang, July 6, 2007.
3. “Physical Design for 3D Integration at the Chip and Package Level,” Samsung Semiconductor, Kiheung. Invited by Dr. Kyu Myoung Choi at System LSI Team, July 11, 2007.
4. “3D Integrated Circuits: Challenges and Opportunities,” Hynix Semiconductor Inc., Icheon. Invited by Dr. Jun Ho Lee at Memory R&D Division, January 24, 2008.
5. “Power and Thermal-aware Architecture, Circuits, and Interconnect Techniques,” Samsung Semiconductor, Kiheung. Invited by Dr. Jin Suk Kong at System LSI Team, June 3, 2008.
6. “Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs,” Electronics and Telecommunications Research Institute (ETRI), Kwangju, Invited by Dr. Hyun Suh Kang, December 11, 2008.

V. Service

V.A. Professional Contributions

V.A.1. Professional Membership

1. Institute of Electrical and Electronics Engineers (IEEE), member (1995–2005), senior member (2005–present)
2. Association for Computing Machinery (ACM), member (1995–present)
3. Advisory Board Member, ACM Special Interest Group on Design Automation (SIGDA) (2003–2007)
4. Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (2007–present)
5. Guest Editorship
 - ACM Transactions on Design Automation of Electronic Systems, “Special Issue on Demonstrable Software Systems and Hardware Platforms” (2006)
 - International Journal of Computational Science and Engineering, “Special Issue on Computational Methods and Techniques for Nanoscale Technology Computer Aided Design” (2007)
6. Publication Chair (2005) and Tutorials Chair (2006), International Conference on Compilers, Architectures and Synthesis of Embedded Systems
7. CAD Track Chair, IEEE International Symposium on Circuits and Systems (2004–2006)
8. Publication Chair, IFIP International Conference on VLSI (2007)
9. Co-chair, Workshop on Accelerating Time-to-Market through Compiler-driven Optimization of Embedded Platforms (2004)

10. Technical Program Committee Member

- IEEE International Conference on Computer-Aided Design (2009)
- IEEE International Symposium on Circuits and Systems (2002, 2003)
- ACM Great Lakes Symposium on VLSI (2004, 2005, 2006, 2007)
- IEEE International Conference on Computer Design (2003, 2005, 2006, 2007)
- ACM/IEEE Asia South Pacific Design Automation Conference (2005, 2008, 2009)
- ACM International Symposium on Physical Design (2006, 2007)
- IFIP International Conference on VLSI (2004, 2007)
- International Conference on Parallel Processing (2005)

V.B. Campus Contributions

1. Graduate Curriculum Committee, School of Electrical and Computer Engineering (2002 – 2004)
2. Faculty Honors Committee, School of Electrical and Computer Engineering (2004 – 2007)
3. Undergraduate Curriculum Committee, School of Electrical and Computer Engineering (2007 – present)
4. Affiliated Faculty, Center for Research in Embedded Systems and Technology (CREST) (2002 – present)
5. Affiliated Faculty, Center for Experimental Research in Computer Systems (CERCS) (2002 – present)
6. Affiliated Faculty, Packaging Research Center (PRC) (2002 – present)
7. Faculty advisor, Korean Graduate Student Association (2001 – present)
8. Faculty advisor, Korean Undergraduate Student Association (2001 – present)

VI. Grants and Contracts

VI.A. As Principal and Co-principal Investigator

1. Performance vs Power Optimization in Physical Design Automation
 - Role: PI
 - Organization: Georgia Yamacraw
 - Contract Period: August 16, 2001 – August 15, 2004
 - Amount Awarded: \$270,000
2. Noise Immune On/Off Chip 3-D Routing for High Speed System-On-Package Substrate
 - Role: PI
 - Organization: National Science Foundation
 - Contract Period: August 15, 2002 – August 14, 2004
 - Amount Awarded: \$100,000
3. Chip/Package Co-design of Physical Layout for Fast and Reliable System-On-Packages
 - Role: PI
 - Organization: Association for Computing Machinery
 - Contract Period: June 15, 2003 – June 14, 2004
 - Amount Awarded: \$24,000

4. Placement and Routing for Polymorphic Computing Architecture
 - Role: PI
 - Organization: Defense Advanced Research Projects Agency (sub-contract)
 - Contract Period: May 15, 2003 – May 14, 2004
 - Amount Awarded: \$45,000
5. NER: Automatic Placement Algorithms for Quantum Cell Automata
 - Role: PI (co-PI: Mike Niemier), my share = 70%.
 - Organization: National Science Foundation
 - Contract Period: August 1, 2004 – July 31, 2005
 - Amount Awarded: \$129,734
6. Bringing Low Power Reconfigurable Analog Signal Processing to Embedded Systems
 - Role: PI (co-PIs: David Anderson, Paul Hasler), my share = 100%.
 - Organization: National Science Foundation
 - Contract Period: September 1, 2004 – August 31, 2007
 - Amount Awarded: \$240,000
7. High-Performance 3D Microarchitecture Design
 - Role: co-PI (PI: Gabriel H. Loh, co-PI: Hsien-Hsin S. Lee and Sung Kyu Lim), my share = 33%.
 - Organization: Gigascale Systems Research Center, Semiconductor Research Corporation
 - Contract Period: June 1, 2005 – August 31, 2006
 - Amount Awarded: \$210,000
8. Equipment Grant
 - Organization: Intel Corporation
 - Date Awarded: September 7, 2005
 - Amount Awarded: \$75,000
9. CAREER: Physical Design Automation for Fast and Reliable 3D Circuits
 - Role: PI
 - Organization: National Science Foundation
 - Contract Period: June 15, 2006 – June 14, 2011
 - Amount Awarded: \$400,000
10. High-Performance 3D Microarchitecture Design
 - Role: co-PI (PI: Gabriel H. Loh, co-PI: Hsien-Hsin S. Lee and Sung Kyu Lim), my share = 33%.
 - Organization: Center for Circuit & System Solutions, Semiconductor Research Corporation
 - Contract Period: September 1, 2006 – August 31, 2009
 - Amount Awarded: \$450,000
11. Mixed Signal Design Tool for System-On-Package
 - Role: PI
 - Organization: Packaging Research Center
 - Contract Period: January 8, 2007 – January 7, 2009

- Amount Awarded: \$100,000
12. Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs
 - Role: PI
 - Organization: Interconnect Focus Center, Semiconductor Research Corporation
 - Contract Period: September 1, 2007 – August 31, 2009
 - Amount Awarded: \$250,000
 13. Design, Fabrication, and Testing of 3D-MAPS: A Massively Parallel Processor with 3D Stacked Memory
 - Role: PI (co-PIs: Hsien-Hsin S. Lee and Gabriel H. Loh), my share = 33%.
 - Organization: National Security Agency
 - Contract Period: February 1, 2009 – January 31, 2011
 - Amount Awarded: \$941,248
 14. 3D Integration of Sub-Threshold Multi-core Co-processor for Ultra Lower Power Computing
 - Role: PI (co-PI: Saibal Mukhopadhyay), my share = 50%.
 - Organization: National Science Foundation
 - Contract Period: August 15, 2009 – August 14, 2012
 - Amount Awarded: \$450,000

VII. Honors and Awards

1. Design Automation Conference Graduate Scholarship (\$24,000), 2003.
2. NSF Faculty Early Career Development (CAREER) Award (\$400,000), 2006.
3. Outstanding Junior Faculty Member Award, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2007.
4. Hesburgh Award Teaching Fellows, Center for the Enhancement for Teaching and Learning (CETL), Georgia Institute of Technology, 2008. (Institute-level Teaching Award for tenured faculty)
5. Distinguished Service Award, ACM Special Interest Group on Design Automation (SIGDA), 2008.
6. Marquis Who's Who in America, 2007, 2008, 2009, 2010.

VIII. Teaching Evaluation

VIII.A. Undergraduate Courses

Term/Year	Course Number/Name	# of students	# of responses	teaching score
Fall 2001	ECE3060: VLSI and Advanced Digital Design	43	36	3.8
Spring 2002	ECE2030: Introduction to Computer Engineering	49	42	4.1
Spring 2003	ECE3060: VLSI and Advanced Digital Design	51	45	4.7
Spring 2004	ECE3060: VLSI and Advanced Digital Design	32	30	4.8
Summer 2004	ECE2030: Introduction to Computer Engineering	27	24	4.8
Fall 2004	ECE3060: VLSI and Advanced Digital Design	32	27	4.7
Summer 2005	ECE2030: Introduction to Computer Engineering	21	18	4.8
Fall 2005	ECE2030: Introduction to Computer Engineering	39	32	4.9
Spring 2006	ECE2030: Introduction to Computer Engineering	39	33	4.9
Spring 2006	ECE3060: VLSI and Advanced Digital Design	29	23	4.8
Summer 2006	ECE2030: Introduction to Computer Engineering	53	41	4.6
Fall 2006	ECE3060: VLSI and Advanced Digital Design	24	14	5.0
Spring 2007	ECE2030: Introduction to Computer Engineering	52	33	4.9
Fall 2007	ECE3060: VLSI and Advanced Digital Design	22	12	4.8
Spring 2008	ECE2030: Introduction to Computer Engineering	52	33	4.9
Fall 2008	ECE3060: VLSI and Advanced Digital Design	37	31	4.9
Spring 2009	ECE2030: Introduction to Computer Engineering	44	21	4.7
Totals (Students/Responses) and Averages (Means)		646	495	4.71

VIII.B. Graduate Courses

Term/Year	Course Number/Name	# of students	# of responses	teaching score
Summer 2002	ECE8823a: Physical Design Automation of VLSI Sys.	20	17	4.7
Fall 2003	ECE8823a: Physical Design Automation of VLSI Sys.	7	7	4.8
Spring 2005	ECE8823a: Physical Design Automation of VLSI Sys.	5	5	4.3
Spring 2007	ECE6133: Physical Design Automation of VLSI Sys.	21	15	5.0
Summer 2007	CS8803: Advanced Digital Design for Embedded HW	17	16	4.8
Spring 2008	ECE6133: Physical Design Automation of VLSI Sys.	21	16	5.0
Summer 2008	CS8803: Advanced Digital Design for Embedded HW	25	16	4.9
Spring 2009	ECE6133: Physical Design Automation of VLSI Sys.	26	18	4.8
Summer 2009	CS8803: Advanced Digital Design for Embedded HW	28	6	5.0
Totals (Students/Responses) and Averages (Means)		170	116	4.81