Georgia Institute of Technology
School of Electrical and Computer Engineering
ECE 4435 Op Amp Design Laboratory Fall 2003

Design Project 1

A Balanced Input Signal Stage with Pre-Emphasis for a DBX Noise Reduction Encoder

Introduction

Professional DBX noise reduction units have an input stage that consists of a balanced-input, variable-gain amplifier followed by a pre-emphasis stage that shapes the frequency response of the signal according to the DBX standard. The input stage converts a balanced input signal into an un-balanced or single-ended signal. The gain of this stage is variable to allow adjustment to accommodate input signals of different levels. The pre-emphasis circuit boosts the signal from the balanced amplifier by 9.5 dB in the frequency range between 400 Hz and 1200 Hz to conform to the DBX record pre-emphasis standard. The object of this design project is to design an input stage for a DBX noise reduction encode unit.

Circuit Specifications

1. The circuit will have one balanced input and one single-ended output.
2. At 1 kHz, the magnitude of the voltage gain from a balanced input signal to an unbalanced output signal will be variable from -6 dB to $+18$ dB.
3. The circuit must be capable of driving a 600 Ω load at its output to a level of $+6$ dBm with a sine-wave input signal in the frequency range of 20 Hz to 20 kHz with an overload margin before clipping of $+6$ dB. (0 dBm corresponds to 1 mW into 600 Ω.)
4. The lower -3 dB or half-power cutoff frequency from either input to the output must be 20 Hz. The upper -3 dB or half-power cutoff frequency must be 20 kHz.
5. The DC offset voltage at either output must have a magnitude less than 10 mV.
6. The voltage gain transfer function from balanced input to unbalanced output will have a zero at 400 Hz and a pole at 1200 Hz.
7. The common-mode rejection ratio of the balanced input stage must be greater than 50 dB.
8. The power supply rejection ratio from either power supply rail to either output must be at least 60 dB.
9. The output impedance to ground must be 100 Ω.
10. The input impedance to ground at each input must be 10 kΩ.
11. A test frequency of 1 kHz is specified for the preceding four steps. Error tolerances of $\pm 5\%$ are acceptable for each specification.

Design Considerations

An important criterion of your design will be the correlation you can achieve between your experimental laboratory results, SPICE computer simulations, and your theoretical calculations. In your preliminary design, you can consider all operational amplifiers to be ideal. Your final design

circuit should be capable of being "tweaked" to compensate for non-ideal characteristics occurring in op amps and other components. Keep in mind that you should be designing a circuit which can be mass produced and widely utilized. Therefore, it should be easily adjusted with off-the-shelf components.

Comparisons should be made among the response of ideal sum and difference amplifiers, the theoretical circuit response as predicted by SPICE, and the experimental circuit response. In the lab, it will be relatively easy to measure the frequency response characteristics with the equipment available. Comparison of theoretical, experimental, and SPICE characteristics will be essential in evaluating the quality of your design.

Power supplies of $+15\,\mathrm{V}$ and $-15\,\mathrm{V}$ are available for your design.

References

Some useful references for the design can be found in Chapters 1, 2, and 5 of the text. You are encouraged to use utilize the library for further references.

Design Evaluation Criteria

1. Design approach, philosophy, and clarity of explanation. Follow suggestions given in the "Op Amp Design Lab Procedures and Instructions" sheet on the class web page.

2. Achievement of design specifications.

3. Documentation of design performance.

4. Design simplicity and economics. Evaluate the cost of your design according to the instructions on the "Op Amp Design Lab Procedures and Instructions" sheet.

5. Assume that your design is to be used in an application requiring large quantity production using off-the-shelf components.

6. Other Components: If you are considering using some special device or component, determine the cost and availability of a tested and guaranteed unit from a reliable vendor. With this information, your laboratory GTA will determine the equivalent cost units.

Design Schedule

1. Submit for approval a preliminary "paper design" to your lab GTA for his review in class on 09/01/03. This paper design should show as a minimum a block diagram of the proposed design with a possible complete circuit diagram with all component values chosen for each block in the diagram. Also, provide design equations and explain the thought processes behind your preliminary design. This preliminary design does not have to be the final design you realize for this experiment, but it should help you begin to solidify the underlying concepts and specifications. Remember, the more information that you can provide for your lab GTA, the more direction he can give you and the more time he can save you in the laboratory. Your "paper design" should be complete enough so that you can assemble and test at least one block during your laboratory period for the week of 09/01/03 without having to do any design work in the lab.

2. Utilize the SPICE computer program to theoretically verify your circuit design. Use the 741 op amp model (and subcircuit) that will be posted on the class web page. Obtain SPICE gain versus frequency plots and transient response plots for the output voltage. Present this SPICE verification of your design to your lab GTA for his certification at your regular lab period during the week of 09/08/03.

3. Complete the laboratory evaluation of your design with a witness verification of proper design performance and submit your complete report to your lab GTA during lab on the week of 09/22/03.

ECE 4435 Design Project Evaluation Criteria

Prelab Submitted on 09/01/03	5 points
Laboratory Attendance	10 points
Explanation of Design Approach & Insight Into Design	10 points
Block Diagram of Circuit	
Derivation of Gain for Each Stage	
Derivation of Pre-Emphasis Network	
Zero and Pole Frequencies	
Derivation of Half-Power Frequencies	
Input Impedance Considerations	
Output Impedance Considerations	
Rejection Ratios	
Results & Presentation of SPICE Simulations	5 points
"Signed Off" in Lab during the second lab period	
Simulation of Final Overall Circuit	
Presentation	
Economics & Cost Analysis	5 points
Justify Design Choices	
Total Component Cost	
Presentation of Experimental Results	5 points
Complete Documentation of Results Verified in Lab	
Comparison of Theoretical, SPICE, and Experimental	
Results (In Tabular Form with % Errors)	
Explanation of Results	
Explanation of Measurement Techniques	
Experimental Results Obtained	5 points
Gains	
Half-Power Frequencies	
Frequency Response of Pre-Emphasis Network	
Input & Output Impedances	
Overload Margin	
Output Offsets	
Signal Rejection Ratios	
Power Supply Rejection Ratio	
Conclusions	5 points
Sources of Error	
Proposed Improvements to Circuit	
General Comments on Whether Specifications are Reasonable	
General Comments on Whether Measuring Techniques are Reasonable	

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Evaluation Sheet for Design Project 1

A Balanced Input Signal Stage with Pre-Emphasis for a DBX Noise Reduction Encoder

Name:_____

_____ 05 Verification of Preliminary Design

_____ 10 Laboratory Attendance

_____ 05 Explanation of Design Approach

_____ 05 Demonstration of Insight into the Design

_____ 05 Results and Presentation of SPICE Simulations

_____ 05 Economics and Cost Analysis

_____ 05 Presentation of Experimental Results

_____ 05 Experimental Results Obtained

_____ 05 Conclusions

_____ 50 Total

Verification of Experimental Results

Parameter	Specification	Result	Witness
Gain at 1 kHz	-6 dB to $+18$ dB		
Frequency Response	20 Hz to 20 kHz		
Zero Frequency	400 Hz		
Pole Frequency	1200 Hz		
Input Resistances	10 kΩ		
Output Resistance	100 Ω		
Output Level	$+6$ dBm		
Overload Margin	$+6$ dB		
Output DC Offset	< 10 mV		
CMRR	> 50 dB		
PSRR	> 60 dB		

Witnessed by: _____ Date: _____