

An Audio Compressor/Peak Limiter Circuit

The object of this experiment is to use the voltage-controlled amplifier designed in the last lab to realize an audio compressor/peak limiter circuit. Such a circuit detects when the output signal increases above a preset limit and reduces the gain of the circuit to cause the output level to not increase as the input level increases. These circuits are commonly used in broadcasting and recording to prevent overload of transmitters and recorders. They are also used for special effects in audio signal processing of voice and music signals.

The difference between a limiter and a compressor is primarily in the attack and release times of the circuits. A limiter reduces gain quickly when an overload occurs and then lets the gain go back to its original value quickly when the overload goes away. For example, if someone drops a microphone in a PA system, the audio pulse generated could blow the loudspeakers. A limiter can prevent this. A compressor changes gain slowly compared to a limiter. These circuits are used to maintain a more constant output level without decreasing gain on transient peaks. Combinations of compressor and limiters are commonly used in broadcasting to cause the transmitter to be modulated at 100% to increase the loudness of their signal at the receiver.

The basic circuit for the design project is described in

<http://users.ece.gatech.edu/~mleach/papers/limiter.pdf>

This circuit uses a p-channel JFET. Your design project is to realize this circuit using an n-channel JFET. The circuit is shown in Figure 1. This circuit differs from that in the reference paper in that the JFET is an n-channel device, the diodes are reversed, and the polarity of two power supply voltages is reversed.

The first part of this lab is to realize the detector part of the circuit in Figure 1 consisting of op amps A_2 and A_3 . The circuit is not to be connected to the VCA until it is operational. The first step is to assemble the precision rectifier circuit consisting of A_2 , A_3 , D_1 , D_2 , and resistors R_4 , R_5 , R_6 , R_7 , and R_9 . Omit D_3 , R_8 , and the circuit to the left of A_3 . The left node of resistor R_9 should connect to the output of A_3 . The specifications are:

- The input resistance is to be $10\text{ k}\Omega$. This is equal to $R_4 || R_7$. It is suggested that you choose $R_4 = R_7$.
- The output voltage from A_3 is to be a negative going full-wave rectified signal with a gain of unity. That is, the voltage output of A_3 is to be $-|v_{IR}|$, where v_{IR} is the voltage applied to the right node of resistors R_4 and R_7 .
- Apply power to the circuit. When it is operational and you have documented its performance, add resistor R_8 to the circuit. Calculate its value so that it causes the output voltage of A_3 to be offset by 1 V positive with no input signal. The output voltage of A_3 should now be $1 - |v_{IR}|$.

The next step is to assemble the current mirror circuit consisting of Q_1 through Q_3 . Do not connect the base input to Q_1 to the output of A_3 until the circuit is operational. The steps are as follows:

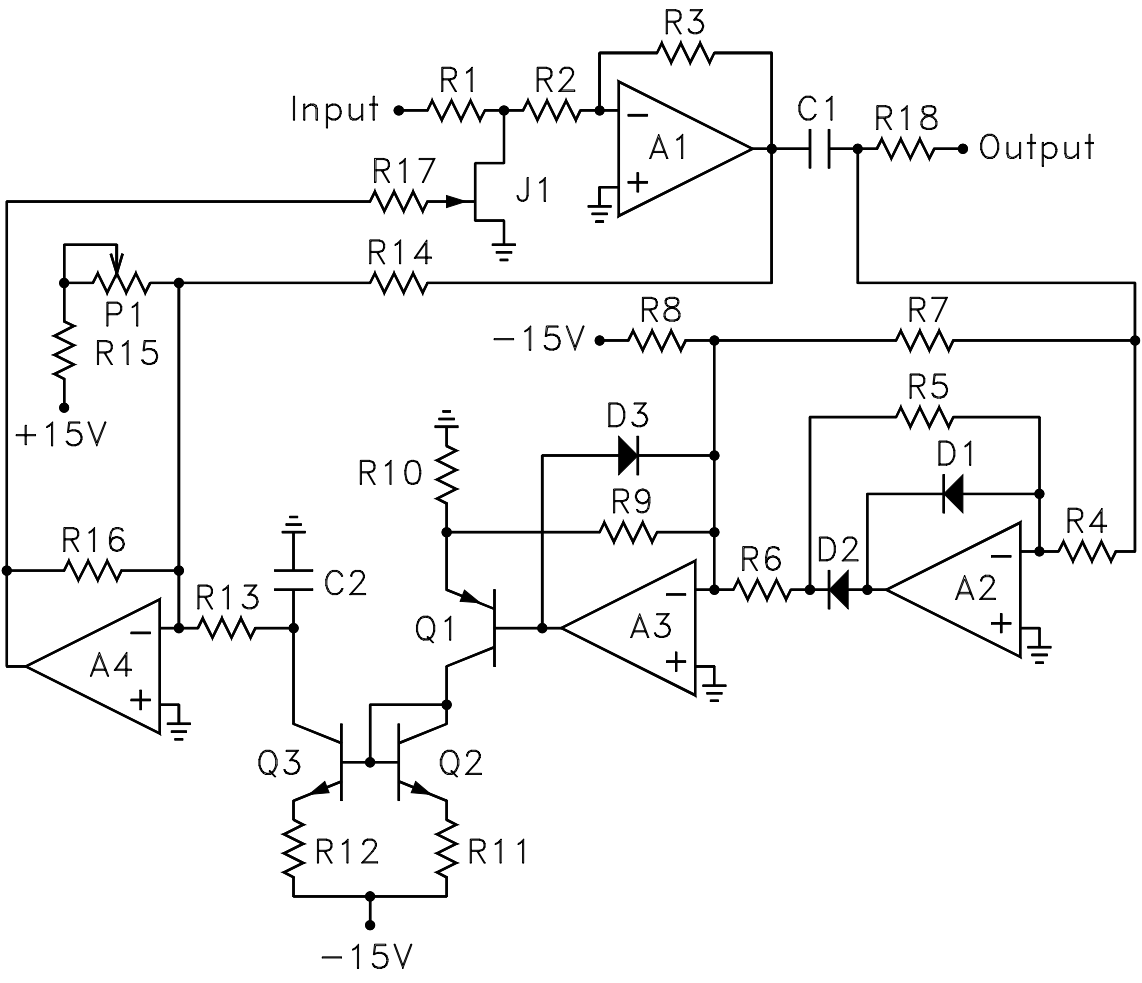


Figure 1: Basic circuit diagram of the compressor/limiter.

- With $R_{10} = 1\text{ k}\Omega$ and $R_{11} = R_{12} = 100\ \Omega$, assemble the circuit consisting of Q_1 through Q_3 . Do not apply power yet.
- Put a diode from the base of Q_1 to ground. The diode arrow should point from base to ground. This diode is the same as D_3 in the circuit, except its cathode should be connected to ground.
- Omitting R_{13} and C_2 , connect the collector of Q_3 to ground through a $1\text{ k}\Omega$ resistor.
- Connect the function generator in series with a $10\text{ k}\Omega$ resistor to the base of Q_1 .
- Connect channel A of the oscilloscope to the emitter of Q_1 and channel B to the collector of Q_3 .
- Apply power to the circuit and adjust the function generator to a suitable level at 1 kHz to produce a negative going signal at the emitter of Q_1 . If the current mirror is working correctly, you should observe the same voltage at the collector of Q_3 . Because the current mirror is not perfect, the voltages may not be exactly the same. But they should be approximately the same.

When the current mirror circuit is operational, the next step is to connect it to the output of the precision rectifier. The steps are as follows:

- Connect the output of A_3 to the base of Q_1 and reconnect D_3 and R_9 as shown Figure 1.
- Power up the circuit.
- Apply a sine wave to the input of the precision rectifier, i.e. to the right nodes of resistors R_4 and R_7 .
- Observe the waveform at the collector of Q_3 . You should see a negative going voltage each time the signal voltage at the input of the precision rectifier exceeds a peak voltage of 1 V (positive or negative).

The circuit will be completed next week by connecting the control circuit to the JFET.