**An Audio Compressor/Peak Limiter Circuit - Part III**

The object of this experiment is to connect the detector circuit assembled last week to the VCA assembled two weeks ago to form a compressor/limiter. The circuit is specified to have an attack time of $\tau_a = 1\,\text{ms}$ and a release time of $\tau_r = 1\,\text{s}$. The design equations for incorporating these specifications into the design are given in

http://users.ece.gatech.edu/~mleach/papers/limiter.pdf

In addition, the threshold of gain reduction is to be 1 V. That is, the circuit is to reduce gain for any signal that causes the output voltage to have a peak value greater than 1 V.

- The first step is to add $P_1$ and $R_{15}$ to the detector circuit designed last week. Calculate the value of these so that $P_1$ can be adjusted to produce a dc offset voltage at the output of $A_4$ over the range $V_{TO} \pm 1\,\text{V}$, where $V_{TO}$ is the threshold voltage for your JFET. The $\pm 1\,\text{V}$ is not an absolute number. The object is to be able to be able to easily adjust $P_1$ so that the dc offset is slightly more positive than $V_{TO}$. The design equation is

$$V_{lim} = V^+ \frac{R_{16}}{R_{15}}$$

  where $V_{lim} = 1\,\text{V}$ is the limit threshold voltage.

- With $C_2 = 10\,\mu\text{F}$, calculate the value of $R_{13}$ for the release time constant $\tau_r = 1\,\text{s}$. The design equation is

$$\tau_r = R_{13} C_2$$

  Use the closest 5% value resistor and use $R_{16} = R_{13}$.

- Using the value of $R_9$ from last week, use the equation

$$R_9 \| R_{10} = \frac{2 R_{13} I_{DSS} R_1 \| R_2}{V_{TO}^2 \left(\tau_r / \tau_a - 1\right)}$$

  to calculate the required value of $R_{10}$.

- With the output of $A_4$ not connected to the JFET, power up the circuit with $v_I = 0$. Adjust $P_1$ so that the dc output of $A_4$ is approximately $V_{TO}$.

- Connect the output of $A_4$ to the JFET gate through $R_{17}$. Apply an input voltage of 0.5 V peak to the circuit. Measure $v_O$ and adjust $P_1$ so that the circuit gain is reduced just slightly from the gain when the JFET is pinched off (or equivalently when the JFET is an open circuit). Increase the input voltage and observe the gain of the circuit automatically reducing so as to maintain a peak output voltage of 1 V as $v_I$ increases to a maximum value of 10 V peak.

- Once the circuit is operational, measure the peak value of $v_O$ versus the peak value of $v_I$ for $0 \le |v_I| \le 10\,\text{V}$ at a frequency of $f = 1\,\text{kHz}$. Plot the graph of $v_{Opeak}$ versus $v_{Ipeak}$ in your report. You should make the measurements at a sufficient number of points to obtain a smooth curve.

The object of this part of the experiment is to make the circuit operational. After your circuit is operational, do not disassemble it. It will be further evaluated next week, and an audio source will be made available so that you can see how it operates with an audio signal.