

Chapter 8

Noise in JFETs

The circuit symbols for the junction FET or JFET are shown in Fig. 8.1. There are two types of devices, the n-channel and the p-channel. Each device has gate (G), drain (D), and source (S) terminals. The drain and source connect through a semiconductor channel. A diode junction separates the gate from the channel. For proper operation as an amplifying device, this junction must be reverse biased. This requires $v_{GS} < 0$ for the n-channel device and $v_{GS} > 0$ for the p-channel device. The principle noise sources in the JFET are thermal noise and flicker noise generated in the channel. If the gate bias current cannot be neglected, the shot noise generated by it must also be included.

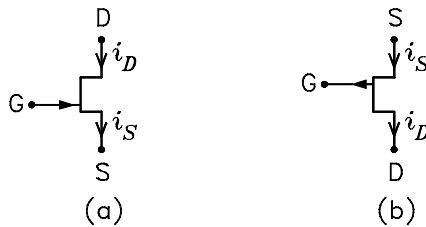


Figure 8.1: JFET circuit symbols. (a) N channel. (b) P channel.

8.1 Device Equations

The discussion here applies to the n-channel JFET. The equations apply to the p-channel device if the subscripts for the voltage between any two of the device terminals are reversed, e.g. v_{GS} becomes v_{SG} . The JFET must be biased with the gate-source junction reverse biased to prevent the flow of gate current, i.e. $v_{GS} < 0$ for the n-channel device and $v_{GS} > 0$ for the p-channel device. The gate current is then equal to the reverse saturation current of the junction. This current is very small and is usually neglected in bias and small-signal calculations. However, its effect is included in the noise model given here. The JFET is biased in the active

mode or the saturation region when $v_{DS} \geq v_{GS} - V_{TO}$, where V_{TO} is the threshold or pinch-off voltage, which is negative.

In the saturation region, the drain current is given by

$$\begin{aligned} i_D &= \beta (v_{GS} - V_{TO})^2 \text{ for } V_{TO} \leq v_{GS} \leq 0 \\ &= 0 \text{ for } v_{GS} < V_{TO} \end{aligned} \quad (8.1)$$

Note that $v_{GS} > 0$ is not allowed because a gate current would flow. The parameter β is the transconductance coefficient given by

$$\beta = \beta_0 (1 + \lambda v_{DS}) \quad (8.2)$$

In this equation, β_0 is the zero-bias value of β , i.e. the value with $v_{DS} = 0$, and λ is the channel-length modulation parameter which accounts for the change in β with drain-source voltage. Because $i_G \simeq 0$ in the pinch-off region, the source current is equal to the drain current, i.e. $i_S = i_D$.

A second way of writing the JFET current is

$$\begin{aligned} i_D &= I_{DSS} \left(1 - \frac{v_{GS}}{V_{TO}}\right)^2 \text{ for } v_{GS} \geq V_{TO} \\ &= 0 \text{ for } v_{GS} < V_{TO} \end{aligned} \quad (8.3)$$

where I_{DSS} is the drain-source saturation current, i.e. the value of i_D with $v_{GS} = 0$. It is given by

$$I_{DSS} = \beta V_{TO}^2 = \beta_0 (1 + \lambda v_{DS}) V_{TO}^2 \quad (8.4)$$

Typical device parameters are $\beta_0 = 2 \times 10^{-4}$ A/V², $V_{TO} = -4$ V, and $\lambda = 0.01$ V⁻¹.

Figure 8.2 shows the typical variation of the drain current i_D with gate-to-source voltage v_{GS} for $V_{TO} \leq v_{GS} \leq 0$. The slope of the curve is the small-signal transconductance g_m . For $v_{GS} < V_{TO}$, the drain current is zero. For $v_{GS} > 0$, gate current flows. Fig. 8.2 shows the typical variation of drain current i_D with drain-to-source voltage v_{DS} for eight values of V_{GS} in the range $V_{TO} < V_{GS} \leq 0$. The dashed line separates the linear or triode region from the active or saturation region. In the saturation region, the slope of the curves is the reciprocal of the small-signal drain-source resistance r_0 .

8.2 Small-Signal Models

There are two small-signal circuit models which are commonly used to analyze JFET circuits. These are the hybrid- π model and the T model. The two models are equivalent and give identical results. They are described below.

8.2.1 Hybrid- π Model

Let the drain current and each voltage be written as the sum of a dc component and a small-signal ac component as follows:

$$i_D = I_D + i_d \quad (8.5)$$

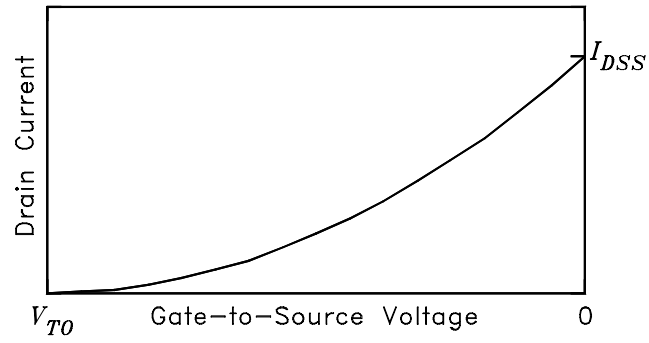


Figure 8.2: Plot of I_D versus V_{GS} for constant V_{DS} .

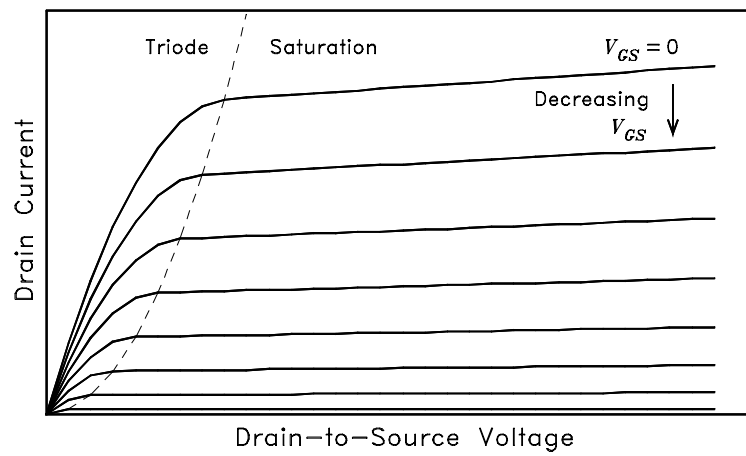


Figure 8.3: Plot of I_D versus V_{DS} for eight values of V_{GS} .

$$v_{GS} = V_{GS} + v_{gs} \quad (8.6)$$

$$v_{DS} = V_{DS} + v_{ds} \quad (8.7)$$

If the ac components are sufficiently small, we can write

$$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} \quad (8.8)$$

where the derivatives are evaluated at the dc bias values. Let us define

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2\beta(V_{GS} - V_{TO}) = 2\sqrt{\beta I_D} \quad (8.9)$$

$$r_0 = \left[\frac{\partial I_D}{\partial V_{DS}} \right]^{-1} = \left[\beta_0 \lambda (V_{GS} - V_{TO})^2 \right]^{-1} = \frac{V_{DS} + 1/\lambda}{I_D} \quad (8.10)$$

The drain current can thus be written

$$i_d = i'_d + \frac{v_{ds}}{r_0} \quad (8.11)$$

where

$$i'_d = i'_s = g_m v_{gs} \quad (8.12)$$

The gate current is given by $i_g = i'_s - i'_d = 0$. The small-signal circuit which models these equations is given in Fig. 8.4(a). This is called the hybrid- π model. The resistor r_d is the parasitic resistance in series with the drain contact. It has a typical value of 50 to 100 Ω . Often it is neglected in calculations. This is done in the following. It is simple to account for r_d in any equation by adding it to the external drain load resistance.

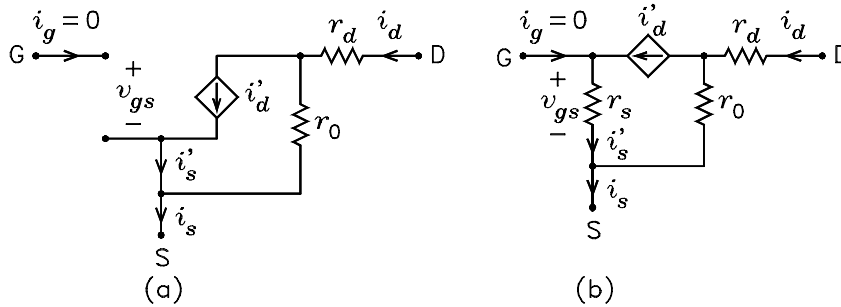


Figure 8.4: (a) JFET hybrid- π model. (b) T model.

8.2.2 T Model

The T model of the JFET is shown in Fig. 8.4(b). The resistor r_0 is given by Eq. (8.10). The resistor r_s is given by

$$r_s = \frac{1}{g_m} \quad (8.13)$$

where g_m is the transconductance defined in Eq. (8.9). The currents are given by

$$i_d = i'_d + \frac{v_{ds}}{r_0} \quad (8.14)$$

$$i'_d = i'_s = \frac{v_{gs}}{r_s} = g_m v_{gs} \quad (8.15)$$

$$i_g = i'_s - i'_d = 0 \quad (8.16)$$

The currents are the same as for the hybrid- π model. Therefore, the two models are equivalent.

8.3 Small-Signal Equivalent Circuits

Several equivalent circuits are derived below which facilitate writing small-signal low-frequency equations for the JFET. We assume that the circuits external to the device can be represented by Thévenin equivalent circuits. The Norton equivalent circuit seen looking into the drain and the Thévenin equivalent circuit seen looking into the source are derived. Several examples are given which illustrate use of the equivalent circuits.

8.3.1 Simplified T Model

Figure 8.5(a) shows the JFET T model with a Thévenin source in series with the gate. We wish to solve for the equivalent circuit in which the source i'_d connects from the drain node to ground rather than from the drain node to the gate node. We call this the simplified T model. Aside for the subscripts, the T model in Fig. 8.4(b) is identical to the T model in Fig. 7.6(b) for the BJT with $r_x = 0$. Therefore, the simplified T model for the JFET must be of the same form as the simplified T model for the BJT in Fig. 7.7(b). Because $i_g = 0$, the effective current gains of the JFET are $\alpha = 1$ and $\beta = \infty$. The simplified T model is shown in Fig. 8.5(b), where i'_d and r_s are given by

$$i'_d = i'_s \quad (8.17)$$

$$r_s = \frac{1}{g_m} \quad (8.18)$$

8.3.2 Norton Drain Circuit

Figure 8.6(a) shows the JFET with Thévenin sources connected to its gate and source leads. The equivalent circuit seen looking into the i_d branch can be represented by a Norton equivalent circuit consisting of a current source $i_{d(sc)}$ in parallel with a resistor r_{id} as shown in Fig. 8.6(b). The expressions for $i_{d(sc)}$ and r_{id} are derived below.

Figure 8.7 shows the simplified T model equivalent circuit. The drain current is given by

$$i_d = i_0 + i'_s \quad (8.19)$$

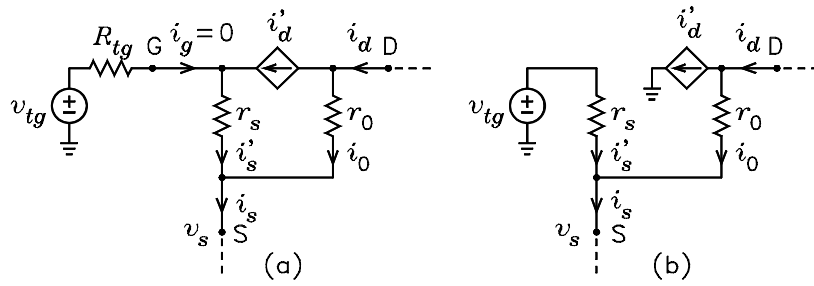


Figure 8.5: (a) JFET T model with Thévenin source connected to the gate. (b) Simplified T model.

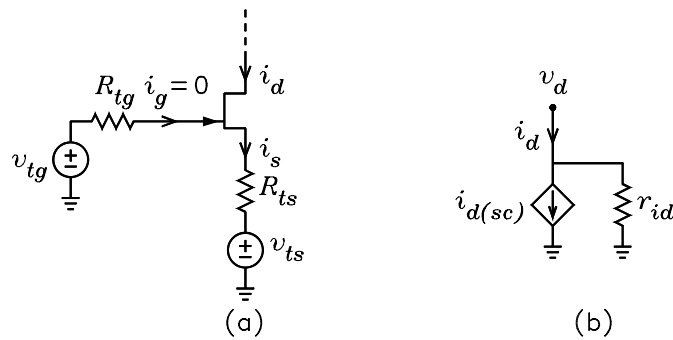


Figure 8.6: (a) JFET with Thévenin sources connected to the gate and the source. (b) Norton drain circuit.

Using superposition of v_d , v_{tg} , and v_{ts} , we can write

$$i_0 = \frac{v_d}{r_0 + r_s \parallel R_{ts}} - v_{tg} \frac{1}{r_s + R_{ts}} \frac{R_{ts}}{r_0 + R_{ts}} - v_{ts} \frac{1}{r_s \parallel r_0 + R_{ts}} \frac{r_s}{r_s + r_0} \quad (8.20)$$

$$i'_s = \frac{v_d}{r_0 + r_s \parallel R_{ts}} \frac{-R_{ts}}{R_{ts} + r_s} + v_{tg} \frac{1}{r_s + R_{ts}} \frac{1}{r_0} - v_{ts} \frac{1}{r_s \parallel r_0 + R_{ts}} \frac{r_0}{r_s + r_0} \quad (8.21)$$

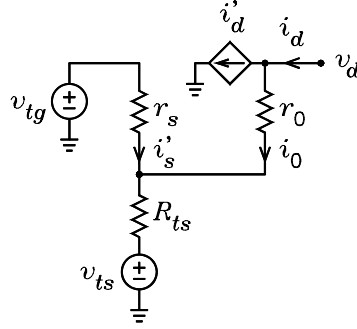


Figure 8.7: Simplified T model for the circuit of 8.6(a).

These equations can be solved for i_d to obtain an equation of the form

$$i_d = \frac{v_d}{r_{id}} + i_{d(sc)} \quad (8.22)$$

where r_{id} and $i_{d(sc)}$ are given by

$$r_{id} = \frac{r_0 + r_s \parallel R_{ts}}{1 - R_{ts}/(R_{ts} + r_s)} = r_0 \left(1 + \frac{R_{ts}}{r_s} \right) + R_{ts} \quad (8.23)$$

$$i_{d(sc)} = \frac{1}{r_s + R_{ts}} \frac{r_0}{r_0 + R_{ts}} v_{tg} - \frac{1}{r_s \parallel r_0 + R_{ts}} v_{ts} \quad (8.24)$$

It is convenient to define two transconductances G_{mg} and G_{ms} such that

$$i_{d(sc)} = G_{mg} v_{tg} - G_{ms} v_{ts}$$

where

$$G_{mg} = \frac{1}{r_s + R_{ts}} \frac{r_0}{r_0 + R_{ts}} \quad G_{ms} = \frac{1}{r_s \parallel r_0 + R_{ts}} \quad (8.25)$$

The Norton equivalent circuit seen looking into the drain is shown in Fig. 9.9(b).

If r_0 is sufficiently large, we can write

$$i_{d(sc)} = G_m (v_{tg} - v_{ts}) \quad G_m = \frac{1}{r_s + R_{ts}} \quad (8.26)$$

In the following, these equations are referred to as the large r_0 approximation for $i_{d(sc)}$.

8.3.3 Thévenin Source Circuit

Figure 8.8(a) shows the JFET with a Thévenin source connected to its gate lead. The equivalent circuit seen looking into the i_s branch can be represented by a Thévenin equivalent circuit consisting of a voltage source $v_{s(oc)}$ in series with a resistor r_{is} as shown in Fig. 8.8(b). The expressions for $v_{s(oc)}$ and r_{is} are derived below.

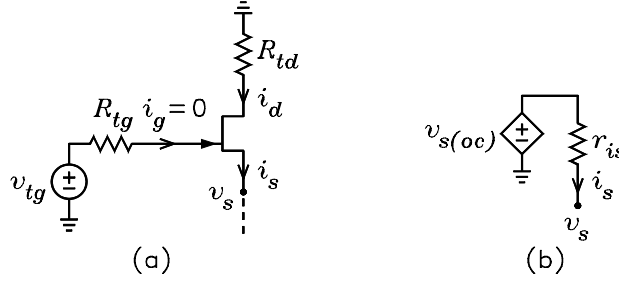


Figure 8.8: (a) JFET with Thévenin source connected to the gate. (b) Thévenin equivalent circuit seen looking into the source.

Figure 8.9 shows the simplified T model equivalent circuit. The current i'_s is given by

$$i'_s = (v_{tg} - v_s) \frac{1}{r_s} \quad (8.27)$$

Using superposition of v_{tg} , the i'_s controlled current source, and i_s , we can write

$$v_s = \frac{v_{tg}}{1 + \chi} \frac{r_0 + R_{td}}{r_s + r_0 + R_{td}} - i'_s \frac{R_{td} r_s}{R_{td} + r_0 + r_s} - i_s [r_s \parallel (r_0 + R_{td})] \quad (8.28)$$

These two equations can be solved for v_s as a function of v_{tg} and i_s to obtain

$$v_s = \frac{v_{tg}}{1 + \chi} \frac{r_0}{r_0 + r_s} - i_s r_s \frac{r_0 + R_{td}}{r_0 + r_s} \quad (8.29)$$

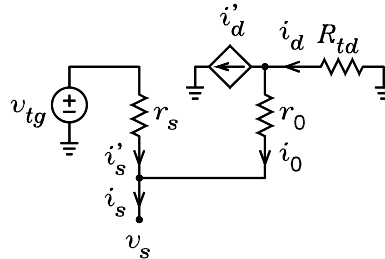


Figure 8.9: Simplified T model for the circuit of 8.8(a).

The equation for v_s is of the form

$$v_s = v_{s(oc)} - i_s r_{is} \quad (8.30)$$

where

$$v_{s(oc)} = \frac{v_{tg}}{1 + \chi} \frac{r_0}{r_0 + r_s} \quad r_{is} = r_s \frac{r_0 + R_{td}}{r_0 + r_s} \quad (8.31)$$

The equivalent circuit is shown in Fig. 9.11(b).

If r_0 is sufficiently large, $v_{s(oc)}$ and r_{is} can be written

$$v_{s(oc)} = v_{tg} \quad r_{is} = r_s \quad (8.32)$$

In the following, these equations are referred to as the large r_0 approximations for $v_{s(oc)}$ and r_{is} .

8.3.4 Summary of Models

Figure 8.10 summarizes the equivalent circuits derived above. For the case where the body is connected to the source, set $\chi = 0$ in all equations.

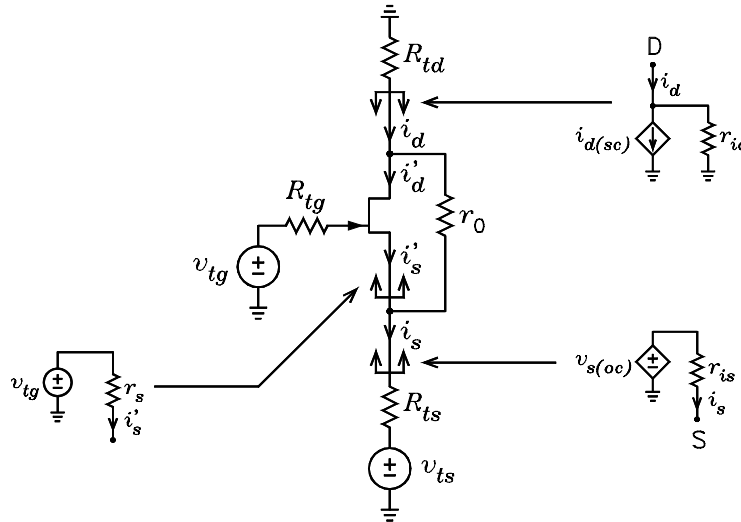


Figure 8.10: Summary of the small-signal equivalent circuits.

8.4 Small-Signal High-Frequency Models

8.4.1 Hybrid-Pi and T Models

Figure 8.11 shows the hybrid- π and T models for the JFET with the gate-source capacitance c_{gs} and the gate-drain capacitance c_{gd} added. The capacitor c_{gss} is the gate-substrate capacitance which is present in integrated-circuit devices but is

omitted in discrete devices. These capacitors model charge storage in the device which affect its high-frequency performance. They are given by

$$c_{gs} = \frac{c_{gs0}}{(1 + V_{SG}/\psi_0)^{1/3}} \quad (8.33)$$

$$c_{gd} = \frac{c_{gd0}}{(1 + V_{DG}/\psi_0)^{1/3}} \quad (8.34)$$

$$c_{gss} = \frac{c_{gss0}}{(1 + V_{SSG}/\psi_0)^{1/2}} \quad (8.35)$$

where V_{SG} , V_{DG} , and V_{SSG} are dc bias voltages; c_{gs0} , c_{gd0} , and c_{gss0} are the zero-bias values; and ψ_0 is the built-in potential. The voltage V_{SSG} is the gate to substrate voltage.

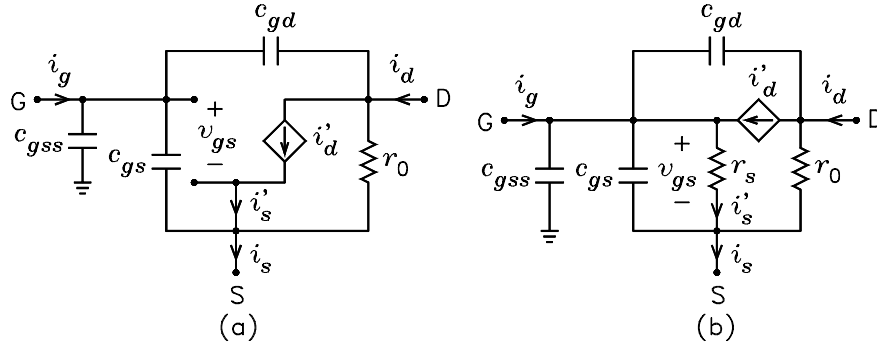


Figure 8.11: Small-signal high-frequency models of the JFET. (a) Hybrid- π model. (b) T model.

8.4.2 Gain-Bandwidth Product

The gain-bandwidth product f_T is a measure of the available bandwidth of the BJT when used as an amplifier. It is defined as the frequency at which the ratio of the short-circuit phasor drain current $I_{d(sc)}$ to the phasor gate current I_g satisfies $|I_{d(sc)}/I_g| = 1$, where $I_{d(sc)}$ is the value of I_d with both the drain and the source connected to signal ground. At low frequencies, the gate current is zero. However, as frequency is increased, a gate current flows in the capacitors in the high-frequency model. The solution for f_T follows that for the BJT in Sec. 7.7.2 with the substitutions $a = 1$, $\beta = \infty$, $r_e = r_s$, $c_\pi = c_{gss} + c_{gs}$, $c_\mu = c_{gd}$, and $c_T = c_{gss} + c_{gs} + c_{gd}$. From Eq. (7.68), it follows that f_T is given by

$$\begin{aligned} f_T &= \frac{1}{2\pi r_s c_T} \sqrt{\frac{1}{1 - (c_{gd}/c_T)^2}} \\ &\simeq \frac{1}{2\pi r_s c_T} = \frac{g_m}{2\pi (c_{gss} + c_{gs} + c_{gd})} \end{aligned} \quad (8.36)$$

where the approximation assumes that $(c_{gd}/c_T)^2 \ll 1$.

8.5 Noise Model

The principle noise sources in a JFET are thermal noise and flicker noise in the drain current. The flicker noise is generated in the space-charge region between the gate and the channel, mostly at the surface. It is reduced by surface pacification techniques and can be made small in well-designed units. If the gate current cannot be neglected, then the shot noise in the gate current must be included. Fig. 8.12 shows the JFET symbols with the noise sources added. The polarity of the sources is arbitrary. Each has been chosen so as to cause an increase in the drain current. The source i_{shg} models the shot noise in the gate bias current I_G . This noise is usually neglected when the gate-source junction is reverse biased. The thermal noise and flicker noise in the drain bias current I_D are modeled by $i_{td} + i_{fd}$. In the band Δf , these have the mean-square values

$$i_{shg}^2 = 2qI_G\Delta f \quad (8.37)$$

$$i_{td}^2 = 4kT \left(\frac{2g_m}{3} \right) \Delta f \quad (8.38)$$

$$i_{fd}^2 = \frac{K_f I_D^m \Delta f}{f^n} \quad (8.39)$$

where $n \simeq 1$ and m is usually taken to be unity. These values are assumed in the following.

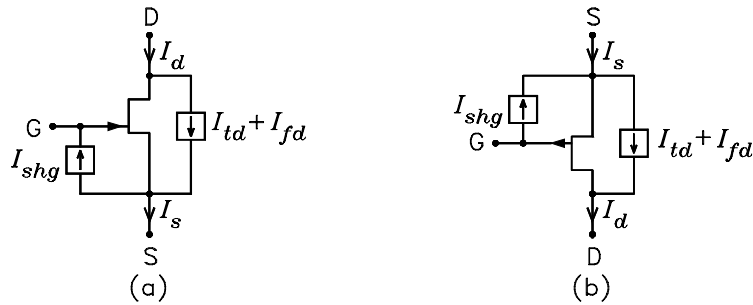


Figure 8.12: JFET symbols with noise sources added.

8.5.1 Equivalent Noise Input Voltage

Figure 8.13(a) shows the n-channel JFET with the drain connected to signal ground. The external gate and source circuits are modeled by Thévenin equivalent circuits. With $v_2 = 0$, the circuit models a common-source or CS stage. With $v_1 = 0$, it models a common-gate or CG stage. The noise sources v_{t1} , and v_{t2} , respectively, model the thermal noise in R_1 and R_2 . In the band Δf , these have the mean-square values

$$v_{t1}^2 = 4kTR_1\Delta f \quad (8.40)$$

$$v_{i2}^2 = 4kTR_2\Delta f \quad (8.41)$$

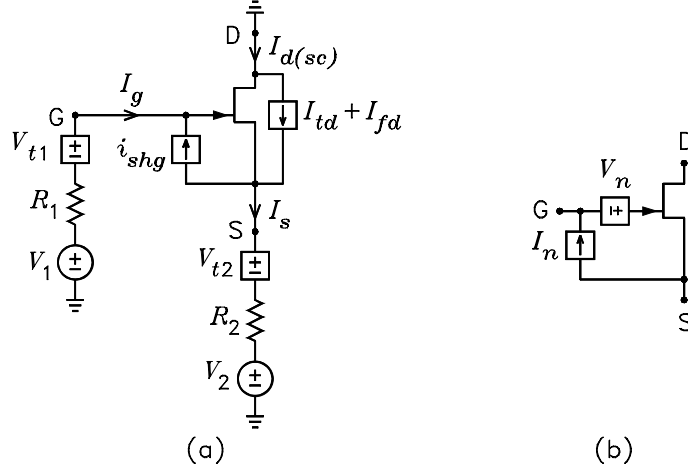


Figure 8.13: (a) JFET with Thévenin sources connected to the gate and the source. (b) JFET $V_n - I_n$ model.

We assume that r_0 is large enough so that Eq. (8.26) can be used to solve for $I_{d(sc)}$. In this case, we can write

$$I_{d(sc)} = G_m (V_{tg} - V_{ts}) + I_{td} + I_{fd} \quad (8.42)$$

where G_m is given by Eq. (8.19) with $R_{ts} = R_2$ and

$$V_{tg} = V_1 + V_{t1} + I_{shg}R_1 \quad (8.43)$$

$$V_{ts} = V_2 + V_{t2} + (I_{td} + I_{fd} - I_{shg})R_2 \quad (8.44)$$

The equivalent noise input voltage v_{ni} can be expressed as a voltage in series with either V_1 or V_2 . Because the common-source amplifier is most often seen, we will express it as a voltage in series with V_1 . First, we factor G_{mg} from Eq. (8.42) to obtain

$$\begin{aligned} I_{d(sc)} = G_m & \left\{ V_1 + V_{t1} + I_{shg}R_1 \right. \\ & - [V_2 + V_{t2} + (I_{td} + I_{fd} - I_{shg})R_2] \\ & \left. + \frac{I_{td} + I_{fd}}{G_m} \right\} \end{aligned} \quad (8.45)$$

The equivalent noise voltage in series with V_1 is given by all terms in the brackets except the V_1 and V_2 terms. It is given by

$$\begin{aligned} V_{ni} = & V_{t1} - V_{t2} + I_{shg}[R_1 + R_2] \\ & + \frac{I_{td} + I_{fd}}{G_m}(1 - G_mR_2) \end{aligned} \quad (8.46)$$

After some algebra, this can be reduced to

$$V_{ni} = V_{t1} - V_{t2} + I_{shg}(R_1 + R_2) + (I_{td} + I_{fd})r_s \quad (8.47)$$

The mean-square value of V_{ni} is given by

$$v_{ni}^2 = v_{t1}^2 + v_{t2}^2 + i_{shg}^2(R_1 + R_2)^2 + (i_{td}^2 + i_{fd}^2)r_s^2 \quad (8.48)$$

which further reduces to

$$v_{ni}^2 = 4kT(R_1 + R_2)\Delta f + 2qI_G\Delta f(R_1 + R_2)^2 + 4kT\left(\frac{2}{3g_m}\right)\Delta f + \frac{K_f I_D \Delta f}{g_m^2 f} \quad (8.49)$$

This expression gives the mean-square equivalent noise input voltage for the CS amplifier. Note that the thermal noise current generated in the channel, when expressed as an equivalent voltage in series with the gate, is the same as the open-circuit thermal noise voltage of a series resistor of value $R_{ser} = 2/3g_m$. The noise factor is given by

$$F = \frac{v_{ni}^2}{4kTR_s} \quad (8.50)$$

where $R_s = R_1$ for the CS amplifier and $R_s = R_2$ for the CG amplifier.

8.5.2 $V_n - I_n$ Noise Model

The $V_n - I_n$ noise model of the JFET is shown in Fig. 8.13(b). We use Eq. (8.47) to solve for the values of V_n and I_n in this circuit. Because V_{ni} given by this equation is the voltage in series with the gate, R_1 must be considered to be the resistance of the signal source. In the $V_n - I_n$ model, the I_n noise source connects between the gate and source. For this reason, R_2 must be set to zero in the circuit to solve for I_n . Otherwise, the noise contributed by R_2 would appear in the model and I_n would connect from the gate to the lower node of R_2 . With $R_2 = 0$, Eq. (8.47) becomes

$$V_{ni} = V_{t1} + I_{shg}R_1 + (I_{td} + I_{fd})r_s \quad (8.51)$$

This equation is of the form $V_{ni} = V_{ts} + V_n + I_n R_s$, where $V_{ts} = V_{t1}$ and $R_s = R_1$. It follows that V_n and I_n are given by

$$V_n = (I_{td} + I_{fd})r_s \quad (8.52)$$

$$I_n = I_{shg} \quad (8.53)$$

The correlation coefficient is zero. The mean-square values are

$$\begin{aligned} v_n^2 &= \frac{i_{td}^2 + i_{fd}^2}{g_m^2} = 4kT \left(\frac{2}{3g_m} \right) \Delta f + \frac{K_f I_D \Delta f}{g_m^2 f} \\ &= \frac{4kT \Delta f}{3\sqrt{\beta I_D}} + \frac{K_f \Delta f}{4\beta f} \end{aligned} \quad (8.54)$$

$$i_n^2 = i_{shg}^2 = 2qI_G \Delta f \quad (8.55)$$

If the gate shot noise can be neglected, the dominant noise above the flicker noise range is the thermal noise generated in the channel. Its mean-square value is inversely proportional to $\sqrt{I_D}$. It follows that this noise decreases by 1.5 dB each time the drain bias current is doubled. Thus there is no optimum bias current which minimizes the thermal noise. The JFET is often biased at $I_D = I_{DSS}/2$ in low-noise design, where $I_{DSS} = \beta V_{TO}^2$ is the drain-source saturation current, i.e. the drain current with $v_{GS} = 0$.

The gate bias current I_G is commonly assumed to be zero when the gate-channel junction is reverse biased. For a high source impedance, the effect of the gate current on the noise might not be negligible. In particular, attention must be paid to the variation of the gate current with drain-gate voltage. In general, the gate current increases with drain-gate voltage. Some devices exhibit a threshold effect such that the gate current increases rapidly when the drain-gate voltage exceeds some value. The drain-gate voltage at which this occurs is called the I_G breakpoint. It is typically in the range of 8 to 40 V.

8.5.3 Flicker Noise Corner Frequency

Figure 8.14 shows a plot of the spectral density $v_n^2/\Delta f$ as a function of frequency for the JFET. The lower frequency at which the plot is twice its high frequency limit is called the flicker noise corner frequency. This is labeled f_{fk} in the figure. At this frequency, the thermal noise and the flicker noise are equal. The flicker noise corner frequency can be solved for by equating the thermal and flicker noise components in Eq. (8.54). It is given by

$$f_{flk} = \frac{3K_f}{16kT} \sqrt{\frac{I_D}{\beta}} \quad (8.56)$$

For $f > f_{flk}$, the thermal noise dominates. For $f < f_{flk}$, the flicker noise dominates. An experimental method for determining the flicker noise coefficient is to measure the flicker noise corner frequency and use Eq. (8.56) to calculate K_f .

8.6 Comparison of the JFET and the BJT

An exact comparison of the BJT and the FET is impossible, in general, because the noise performance of each is so dependent on device parameters and bias currents. At low frequencies, the JFET exhibits only v_n noise, whereas the BJT exhibits both v_n and i_n noise. For a low source resistance, the BJT v_n noise is its dominant

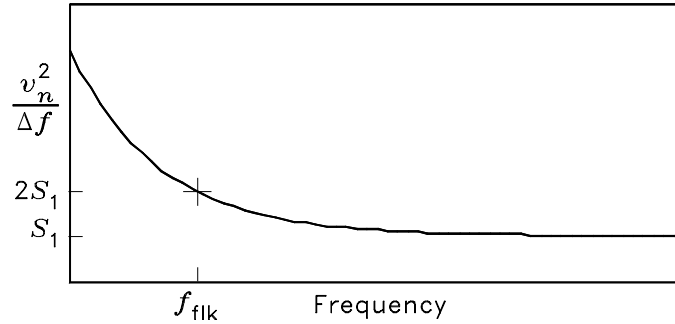


Figure 8.14: Plot of $v_{ni}^2/\Delta f$ versus frequency showing the flicker noise corner frequency.

noise. In this case, the BJT usually has a lower noise than the JFET. For a high source resistance, the BJT i_n noise can cause it to exhibit more noise than the FET. This assumes that the BJT bias current remains fixed as the source resistance is increased. If the BJT is biased for minimum noise, the collector bias current must be decreased as the source resistance is increased. In this case, the FET may not be the better choice device for the lowest noise.

To make an example comparison of the noise performance of the BJT and the JFET, typical numerical values for device parameters must be assumed. Although the conclusions may not be applicable to specific devices, such an example serves to illustrate the differences between the devices. Because flicker noise is so device dependent, it will be neglected. For the BJT, we will assume that $r_x = 40 \Omega$, $V_A = \infty$, and $\beta = 500$. For the JFET, we will assume the parameters $\beta = 5 \times 10^{-4} \text{ A/V}^2$, $\lambda = 0$, and $V_{T0} = -2 \text{ V}$. For these values, the drain-to-source saturation current is $I_{DSS} = \beta V_{T0}^2 = 2 \text{ mA}$.

Let the BJT be connected as a common-emitter amplifier with its emitter connected to ac ground. We calculate the noise both for a constant collector bias current and for the optimum collector bias current $I_{C(opt)}$. Let the JFET be connected as a common-source amplifier with its source connected to ac ground. We calculate the noise for a constant drain bias current. For the constant current cases, we will assume that both the BJT and the JFET are biased at 1 mA so that the devices are compared at the same power dissipation. This assumes the same bias voltage across each device.

Let R_s be the source resistance. For $I_C = 1 \text{ mA}$, the BJT spot noise voltage in

$V/\sqrt{\text{Hz}}$ is

$$\begin{aligned} \frac{v_{ni}}{\sqrt{\Delta f}} &= \left[4kT(R_s + r_x) + 2qI_B(R_s + r_x)^2 \right. \\ &\quad \left. + 2qI_C \left(\frac{R_s + r_x}{\beta} + \frac{V_T}{I_C} \right)^2 \right]^{1/2} \\ &= \left[3.58 \times 10^{-14} 1.30 \times 10^7 (R_s + 40) + 500 (R_s + 40)^2 \right. \\ &\quad \left. + (R_s + 13000)^2 \right]^{1/2} \end{aligned} \quad (8.57)$$

For $I_C = I_{C(opt)}$, it is

$$\begin{aligned} \frac{v_{ni}}{\sqrt{\Delta f}} &= \left[4kT(R_1 + r_x + R_2) \Delta f \times \frac{\sqrt{1 + \beta}}{\sqrt{1 + \beta} - 1} \right]^{1/2} \\ &= 1.32 \times 10^{-10} \sqrt{R_s + 40} \end{aligned} \quad (8.58)$$

For $I_D = 1 \text{ mA}$, the JFET spot noise voltage is

$$\frac{v_{ni}}{\sqrt{\Delta f}} = \left[4kTR_s + \frac{4kT\Delta f}{3\sqrt{\beta}I_D} \right]^{1/2} = 1.29 \times 10^{-10} \sqrt{R_s + 471} \quad (8.59)$$

Figure 8.15 shows the plots of $v_{ni}/\sqrt{\Delta f}$ versus R_s for the three cases. Curve (a) is a plot of (8.57). Curve (b) is a plot of (8.58). Curve (c) is a plot of (8.59). For R_s small, the two BJT cases give the lowest noise. Although the curves almost coincide, the noise is slightly lower for the BJT biased at $I_{C(opt)}$. For R_s large, the JFET and the BJT biased at $I_{C(opt)}$ give the lowest noise. Although the curves almost coincide, the JFET noise is slightly lower than the BJT noise. For R_s in the 3 to 4 k Ω range, the JFET and the BJT biased at $I_C = 1 \text{ mA}$ give approximately the same noise, while the BJT biased at $I_{C(opt)}$ gives slightly lower noise.

It can be concluded that the BJT gives better noise performance for low R_s . For large R_s , the BJT and JFET give approximately the same noise performance provided that the BJT is biased at $I_{C(opt)}$. For large R_s , $I_{C(opt)}$ for the BJT can become very small. A very small bias current is a disadvantage when the amplifier slew rate, e.g. in an op-amp design, is a consideration. For this reason, the JFET may be preferable when the source resistance is high. These conclusions neglect flicker noise effects. Flicker noise is so device dependent that it is difficult to make general conclusions. However, the JFET usually exhibits more flicker noise at low frequencies than the BJT. In JFET's not selected for low flicker noise, the flicker noise corner frequency can be as high as several kHz. In MOSFET's, it can be even higher.

A consideration in the noise comparisons of the CE BJT and CS JFET amplifiers is the difference in input bias currents. To prevent the BJT input bias current from flowing through the signal source, either a coupling capacitor or an offset current source is required. The value of a coupling capacitor may be large if it is chosen

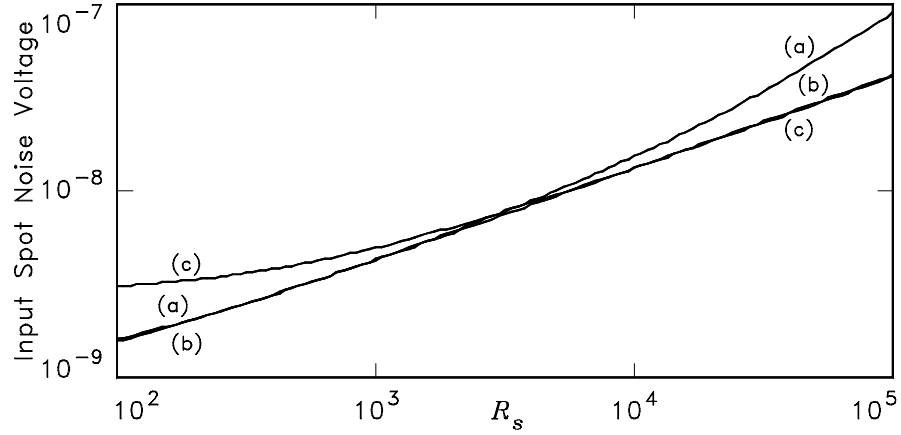


Figure 8.15: Spot noise voltage versus source resistance. (a) BJT biased at 1 mA. (b) BJT biased at $I_{C(opt)}$. (c) JFET biased at 1 mA.

to minimize the noise. Because there is no such thing as a noiseless current source, an offset current source can increase the noise. The zero FET gate current can eliminate the need for the capacitor and offset current source.

8.7 The JFET at High Frequencies

Figure 8.16 shows the high-frequency T model of the JFET with the source and drain connected to signal ground and the gate driven by a voltage source having the output impedance $Z_s = R_s + jX_s$. The gate-source capacitance c_{gs} and the drain-gate capacitance c_{gd} are given by Eqs. (8.33) and (8.34). All noise sources are shown in the circuit except the drain flicker noise current which is assumed to be negligible at high frequencies.

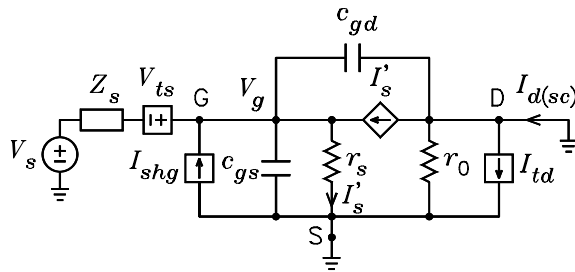


Figure 8.16: T model of a common-source amplifier with the source connected to signal ground.

Following Eq. (7.128) for the common-emitter BJT at high frequencies, we can

write

$$\begin{aligned} I_{d(sc)} &= G_{mg}(\omega) [V_s + V_{ts} + I_{shg}Z_s] + I_{td} \\ &= G_{mg}(\omega) \left[V_s + V_{ts} + I_{shg}Z_s + \frac{I_{td}}{G_{mg}(\omega)} \right] \end{aligned} \quad (8.60)$$

where $G_{mg}(\omega)$ is given by

$$G_{mg}(\omega) = g_m \frac{1 - j\omega c_{dg}/g_m}{1 + j\omega c_T Z_s} \quad (8.61)$$

and $c_T = c_{gs} + c_{gd}$. This equation is obtained from Eq. (7.129) for the BJT by setting $\alpha = 1$, $\beta = \infty$, and $r_e = 1/g_m$. It follows that V_{ni} is given by

$$\begin{aligned} V_{ni} &= V_{ts} + I_{shg}Z_s + \frac{I_{td}}{G_{mg}(\omega)} \\ &= V_{ts} + I_{shg}Z_s + \frac{1 + j\omega c_T Z_s}{1 - j\omega c_{gd}/g_m} \frac{I_{td}}{g_m} \end{aligned} \quad (8.62)$$

This has the mean-square value

$$\begin{aligned} v_{ni}^2 &= 4kTR_s\Delta f + 2qI_G\Delta f |Z_s|^2 \\ &\quad + \frac{(\omega c_T R_s)^2 + (1 - \omega c_T X_s)^2}{1 + (\omega c_{gd}/g_m)^2} \frac{4kT\Delta f}{3\sqrt{\beta I_D}} \end{aligned} \quad (8.63)$$

The noise factor is given by

$$F = \frac{v_{ni}^2}{4kTR_s\Delta f}$$

Equation (8.62) is of the form $V_{ni} = V_{ts} + V_n + I_n Z_s$. It follows that V_n and I_n are given by

$$V_n = \frac{1}{1 - j\omega c_{gd}/g_m} \frac{I_{td}}{g_m} \quad (8.64)$$

$$I_n = I_{shg} + \frac{j\omega c_T}{1 - j\omega c_{gd}/g_m} \frac{I_{td}}{g_m} \quad (8.65)$$

The mean-square values and correlation coefficient are given by

$$\begin{aligned} v_n^2 &= \frac{1}{1 + (\omega c_{gd}/g_m)^2} 4kT \left(\frac{2}{3g_m} \right) \Delta f \\ &= \frac{1}{1 + (\omega c_{gd}/g_m)^2} \frac{4kT\Delta f}{3\sqrt{\beta I_D}} \end{aligned} \quad (8.66)$$

$$\begin{aligned} i_n^2 &= 2qI_G\Delta f + \frac{(\omega c_T)^2}{1 + (\omega c_{gd}/g_m)^2} 4kT \left(\frac{2}{3g_m} \right) \Delta f \\ &= 2qI_G\Delta f + \frac{(\omega c_T)^2}{1 + (\omega c_{gd}/g_m)^2} \frac{4kT\Delta f}{3\sqrt{\beta I_D}} \end{aligned} \quad (8.67)$$

$$\begin{aligned}
\gamma &= \frac{1}{v_n i_n} \frac{-j\omega c_T}{1 + (\omega c_{gd}/g_m)^2} 4kT \left(\frac{2}{3g_m} \right) \Delta f \\
&= \frac{1}{v_n i_n} \frac{-j\omega c_T}{1 + (\omega c_{gd}/g_m)^2} \frac{4kT\Delta f}{3\sqrt{\beta I_D}}
\end{aligned} \tag{8.68}$$

For the case $I_G = 0$, the correlation coefficient simplifies to $\gamma = -j$. The $v_n - i_n$ noise model is given in Fig. 8.13(b).

If the shot noise of the gate current is neglected, the correlation coefficient reduces to $\gamma = -j$. For this case, it follows that the optimum source impedance which minimizes F is given by

$$Z_{opt} = \left(\sqrt{1 - \gamma_i^2} - j\gamma_i \right) \frac{v_n}{i_n} = \frac{j}{\omega c_T} \tag{8.69}$$

Because this has no real part, a noise conventional matching network cannot be designed to optimize the noise factor. However, an inductor in series with the source having the impedance Z_{opt} can be used to improve the signal-to-noise ratio at the operating frequency. In this case, the minimum noise factor is given by

$$F = 1 + \frac{(\omega c_T R_s)^2}{\left[1 + (\omega c_{gd}/g_m)^2 \right] (4kT R_s \Delta f)} \frac{4kT_0 \Delta f}{3\sqrt{\beta I_D}} \tag{8.70}$$