LECTURE 200 – BICMOS TECHNOLOGY
(READING: Text-Sec. 2.11)

INTRODUCTION

Objective

- Illustrate BiCMOS technology

Outline

- Introduction
- Physical process illustration
- Summary

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Typical BiCMOS Technology

The following pages describe a 0.5µm BiCMOS process.

Masking Sequence:

1. Buried n+ layer
2. Buried p+ layer
3. Collector tub
4. Active area
5. Collector sinker
6. n-well
7. p-well
8. Emitter window
9. Base oxide/implant
10. Emitter implant
11. Poly 1
12. NMOS lightly doped drain
13. PMOS lightly doped drain
14. n+ source/drain
15. p+ source/drain
16. Silicide protection
17. Contacts
18. Metal 1
19. Via 1
20. Metal 2
21. Via 2
22. Metal 3
23. Nitride passivation

Notation:

BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN3 generated, during the field oxidation.

TEOS = Tetro-Ethyl-Ortho-Silicate. A chemical compound used to deposit conformal oxide films.

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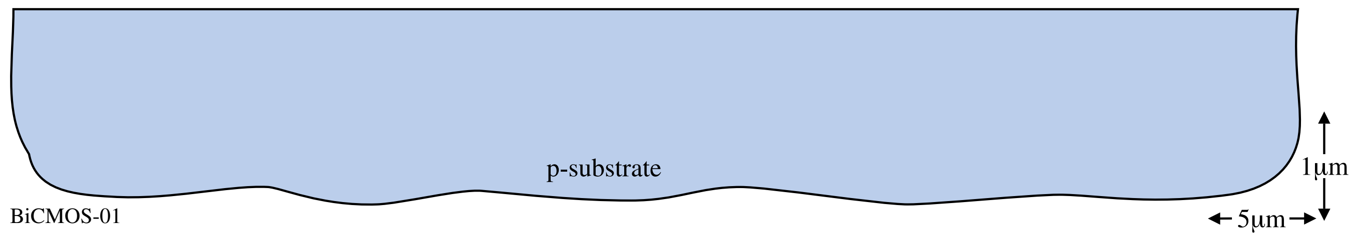
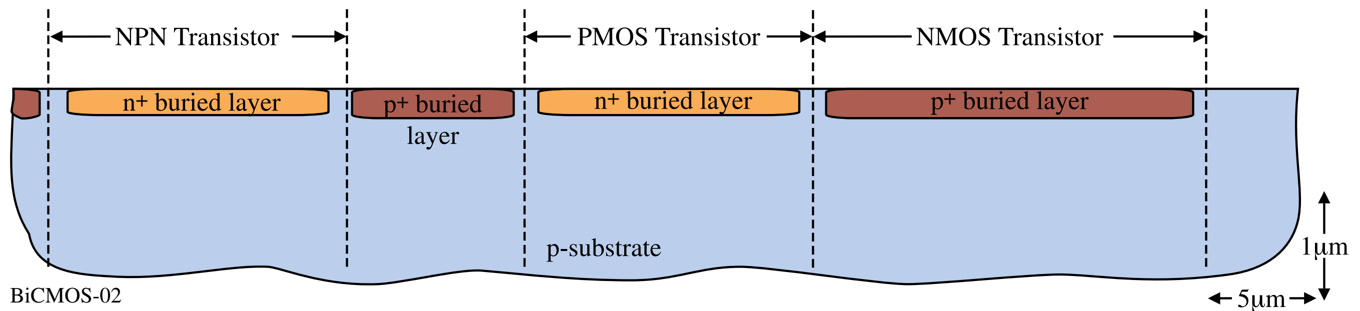
n+ and p+ Buried Layers

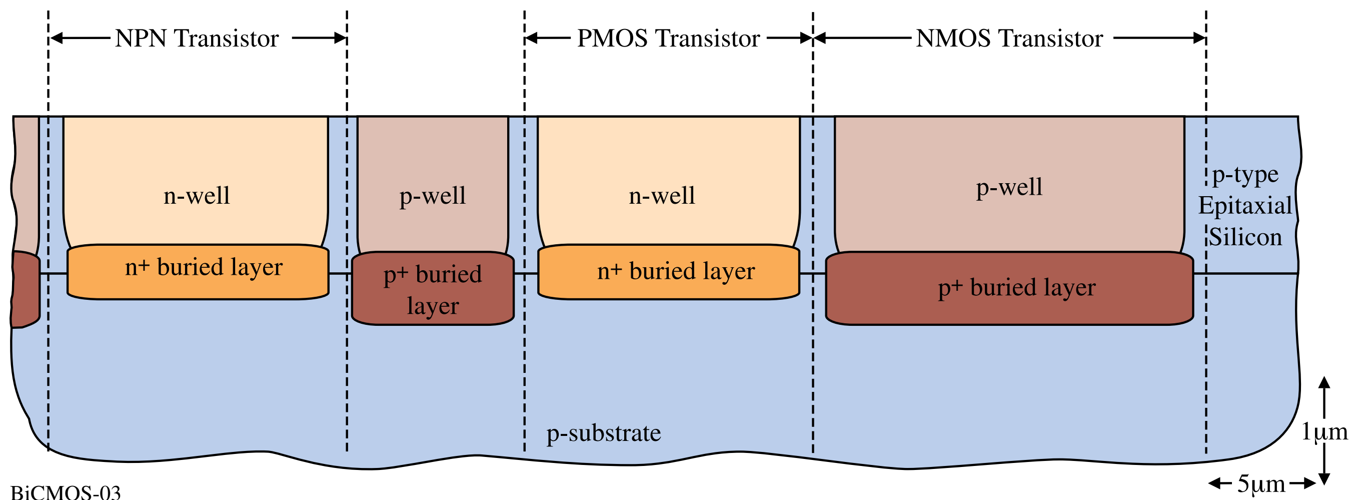
Starting Substrate:



n+ and p+ Buried Layers:



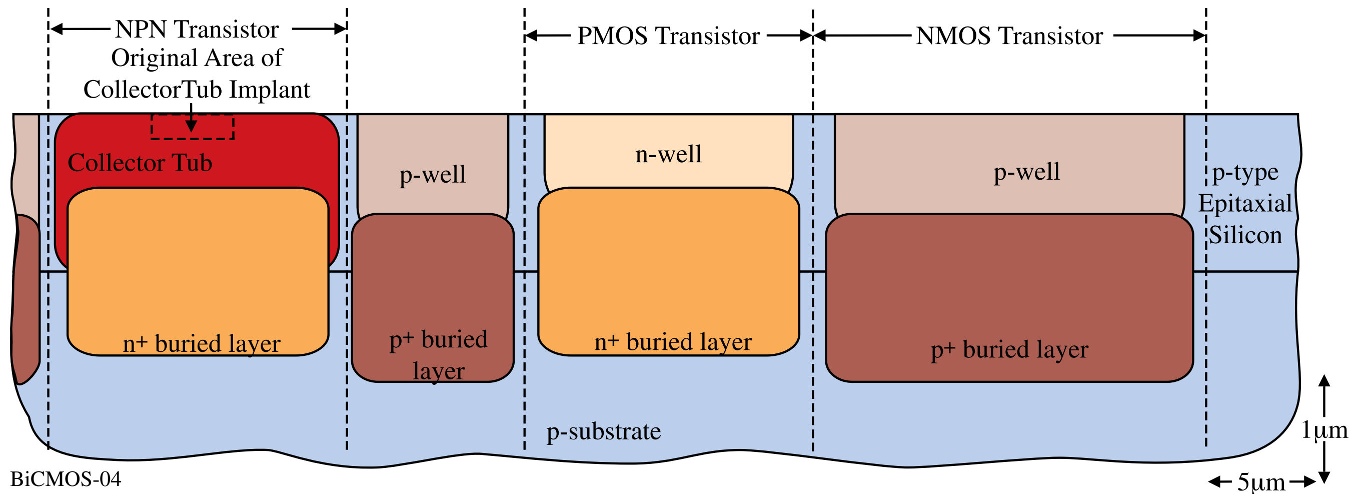
Epitaxial Growth



Comment:

- As the epi layer grows vertically, it assumes the doping level of the substrate beneath it.
- In addition, the high temperature of the epitaxial process causes the buried layers to diffuse upward and downward.

Collector Tub



Comment:

- The collector area is developed by an initial implant followed by a drive-in diffusion to form the collector tub.

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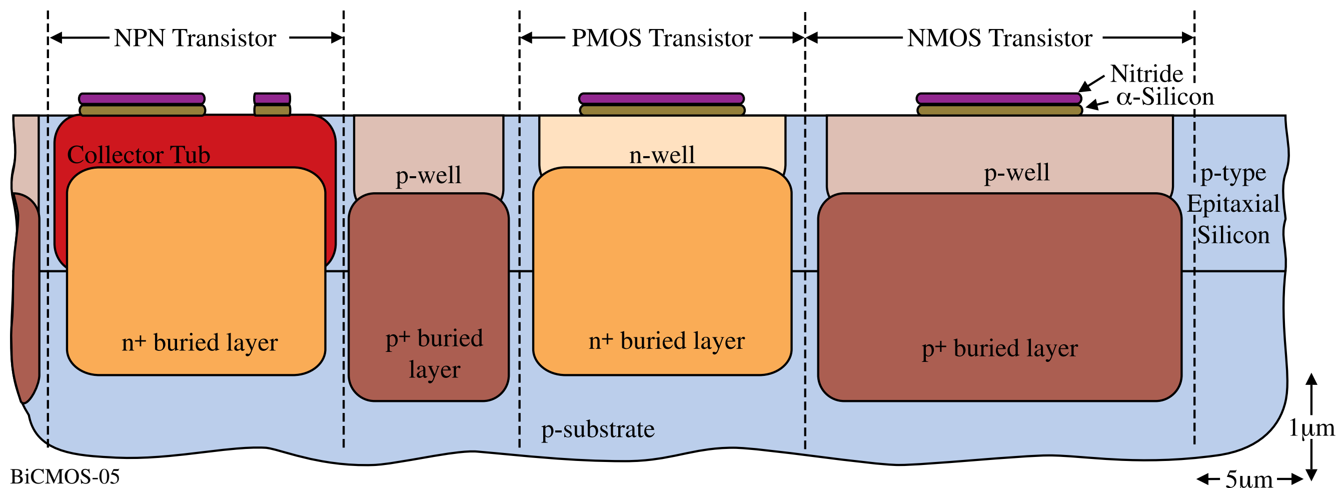
Active Area Definition



Comment:

- The silicon nitride is use to impede the growth of the thick oxide which allows contact to the substrate
- α-silicon is used for stress relief and to minimize the bird's beak encroachment

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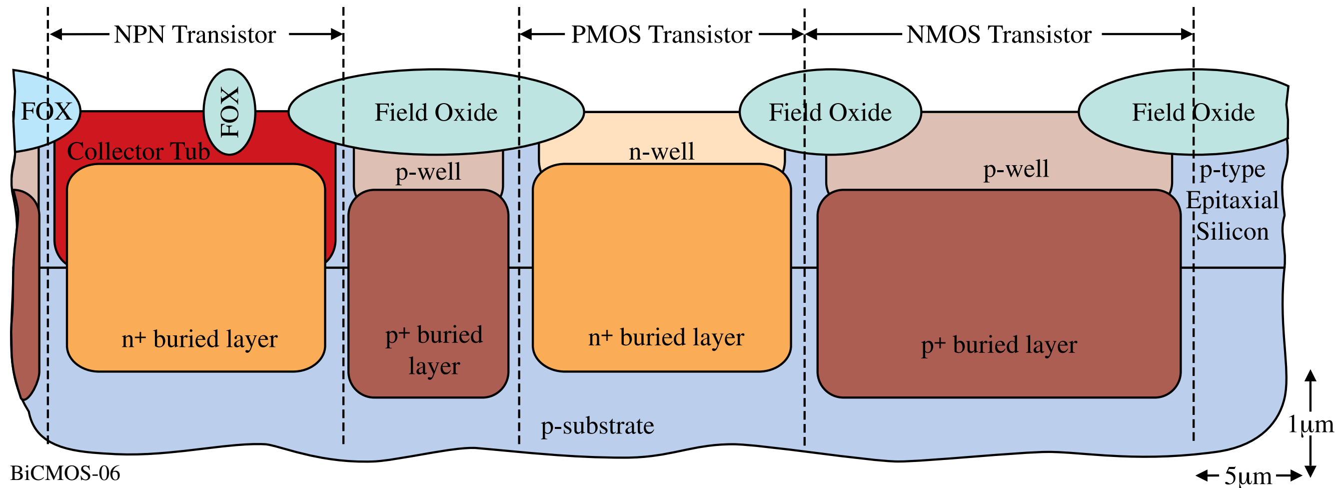
Field Oxide

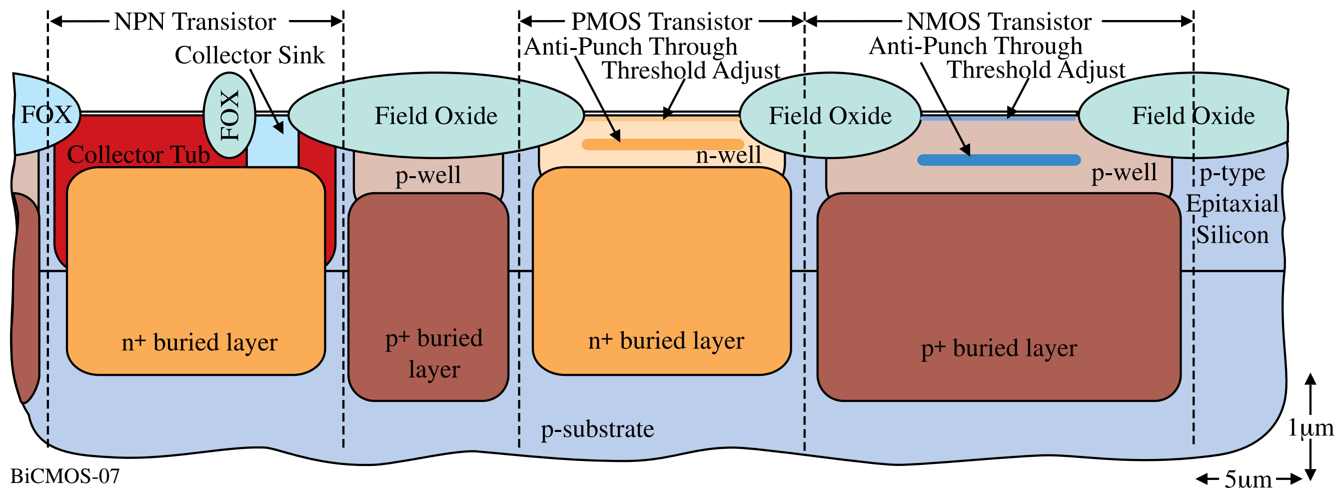


BiCMOS-06

Comments:

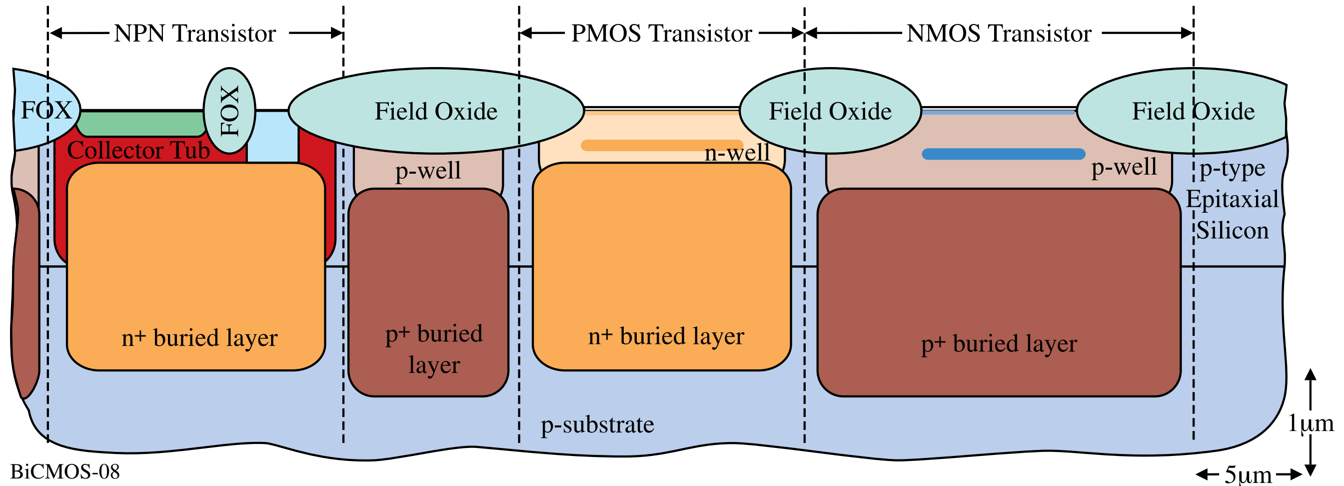
- The field oxide is used to isolate surface structures (i.e. metal) from the substrate

Collector Sink and n-Well and p-Well Definitions



BiCMOS-07

Base Definition



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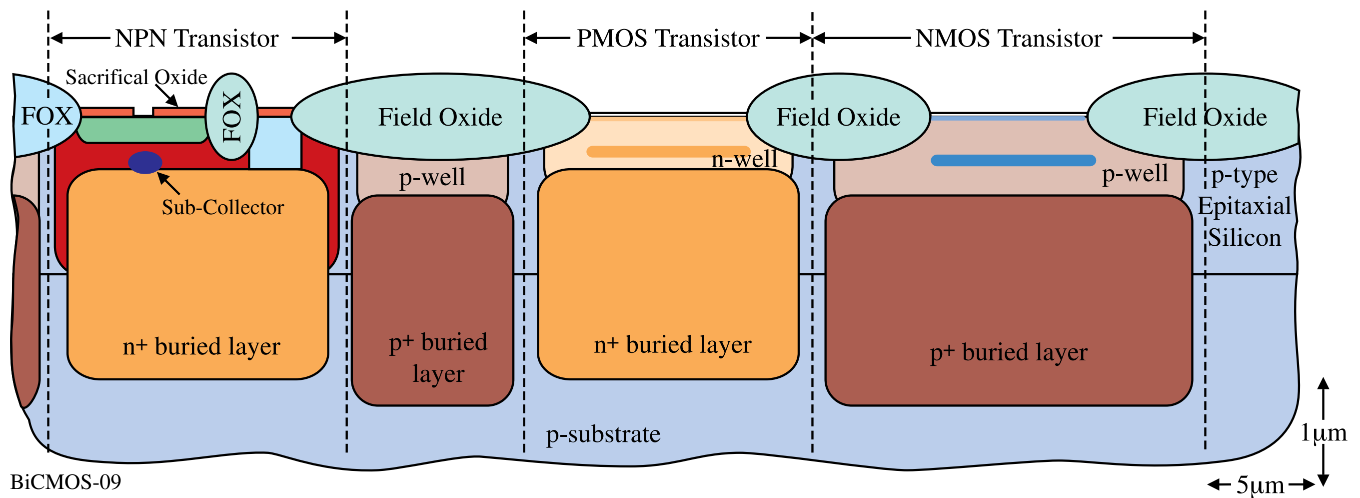
Definition of the Emitter Window and Sub-Collector Implant



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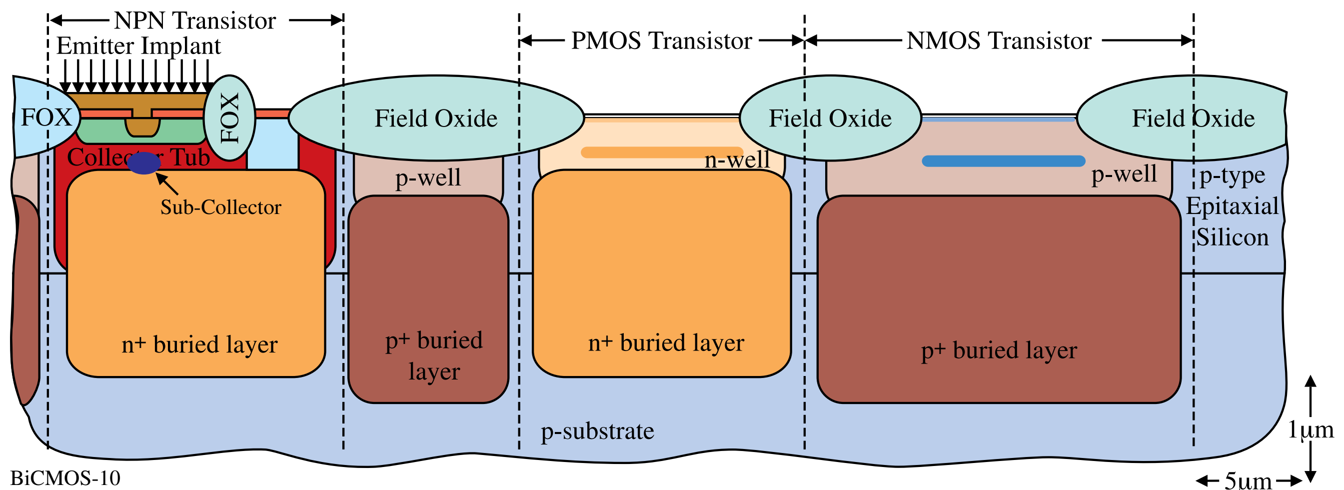
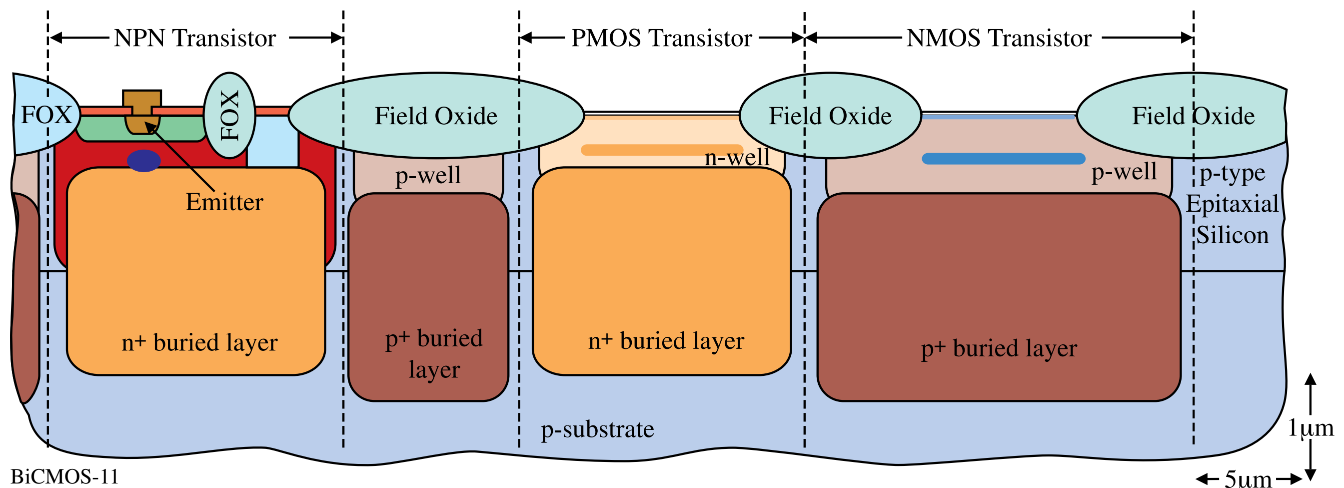
Emitter Implant



Comments:

- The polysilicon above the base is implanted with n-type carriers

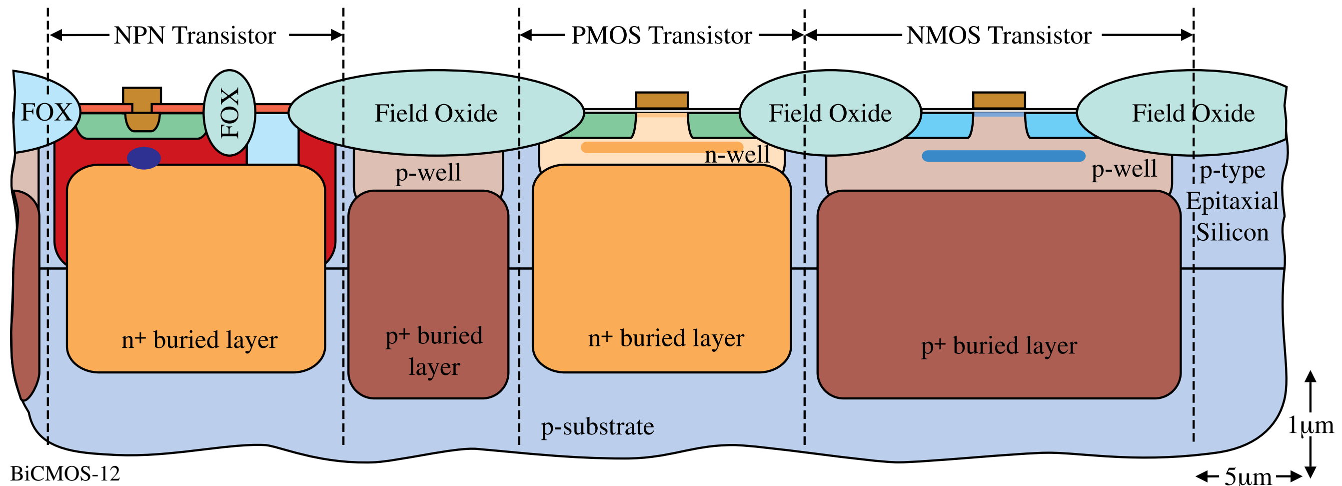
Emitter Diffusion



Comments:

- The polysilicon not over the emitter window is removed and the n-type carriers diffuse into the base forming the emitter

Formation of the MOS Gates and LD Drains/Sources

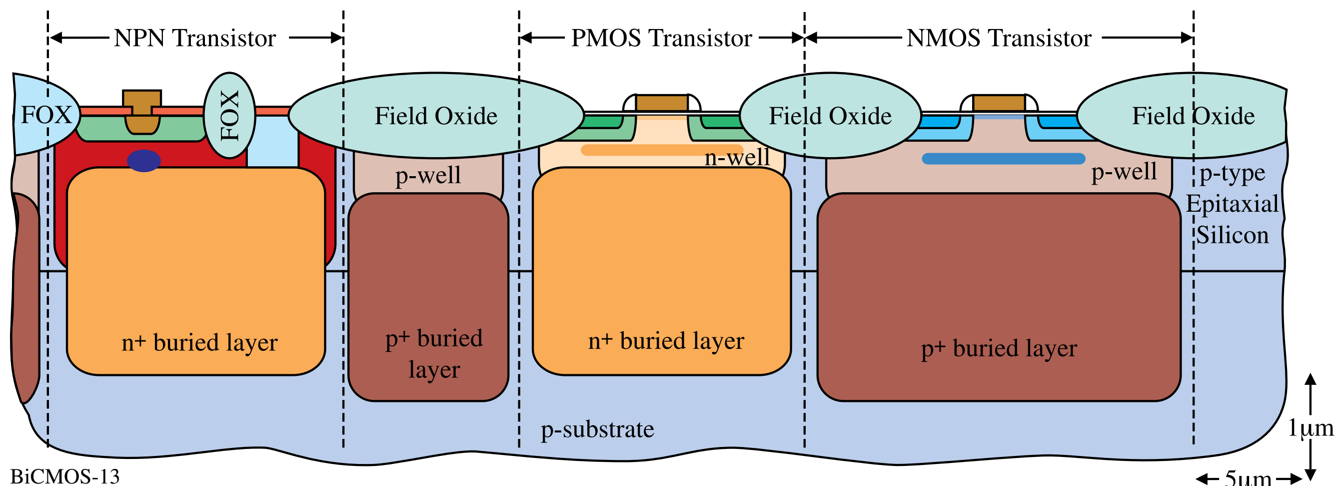


BiCMOS-12

Comments:

- The surface of the region where the MOSFETs are to be built is cleared and a thin gate oxide is deposited with a polysilicon layer on top of the thin oxide
- The polysilicon is removed over the source and drain areas
- A light source/drain diffusion is done for the NMOS and PMOS (separately)

Heavily Doped Source/Drain

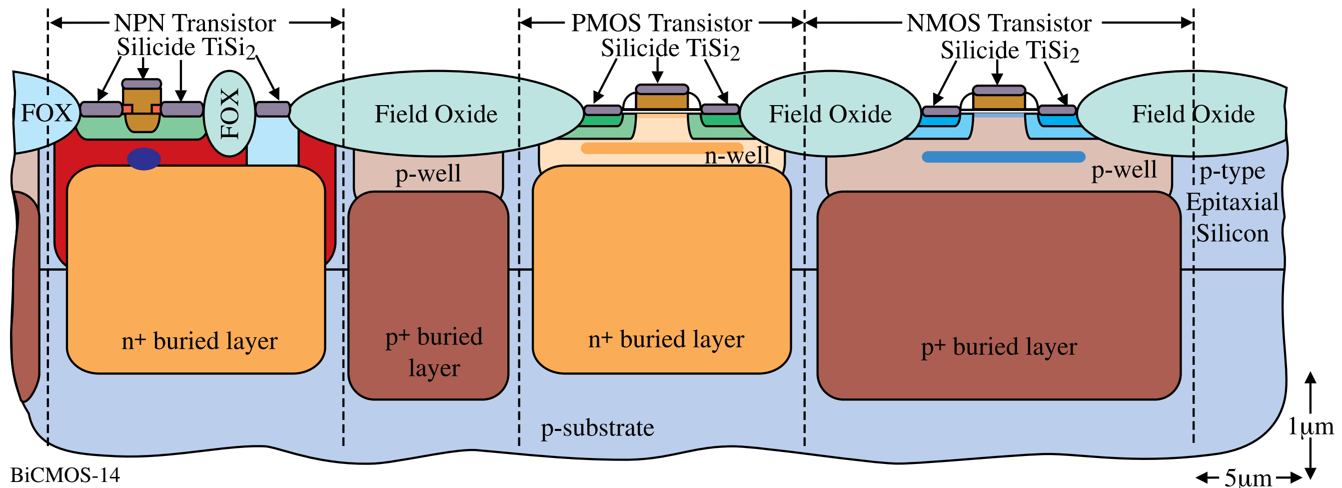


BiCMOS-13

Comments:

- The sidewall spacers prevent the heavy source/drain doping from being near the channel of the MOSFET

Siliciding

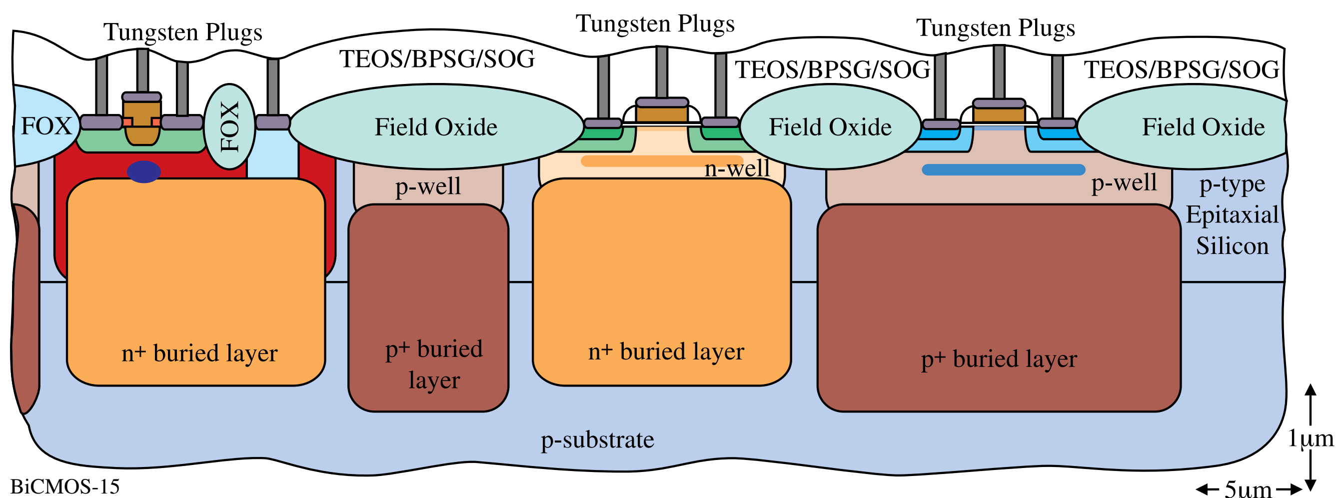


BiCMOS-14

Comments:

- Siliciding is used to reduce the resistance of the polysilicon and to provide ohmic contacts to the base, emitter, collector, sources and drains

Contacts

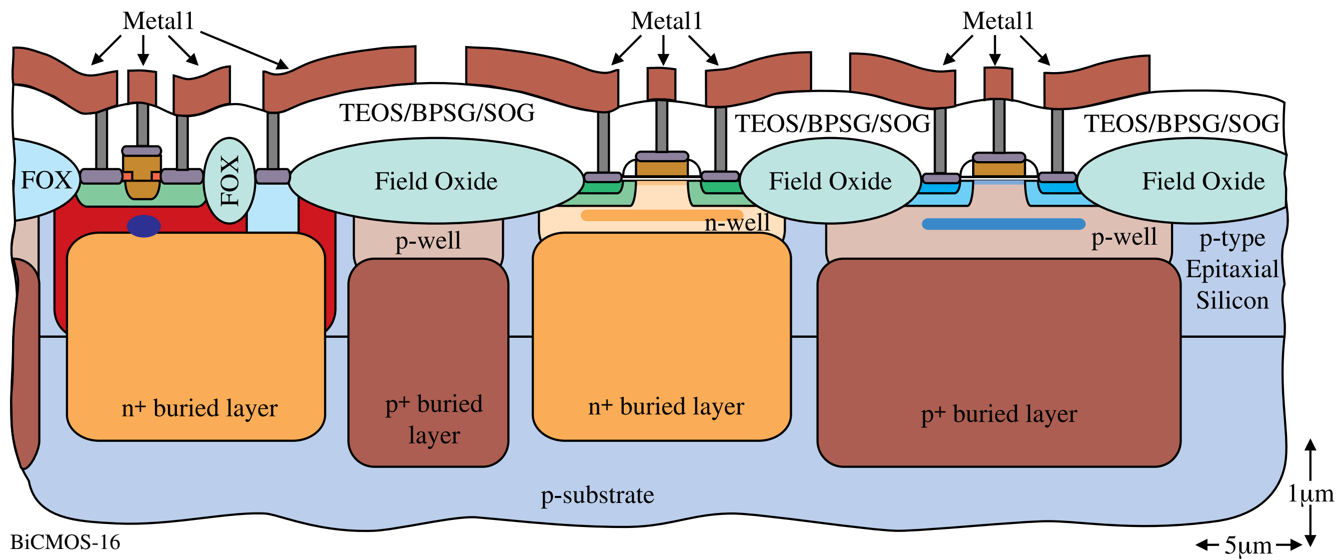


BiCMOS-15

Comments:

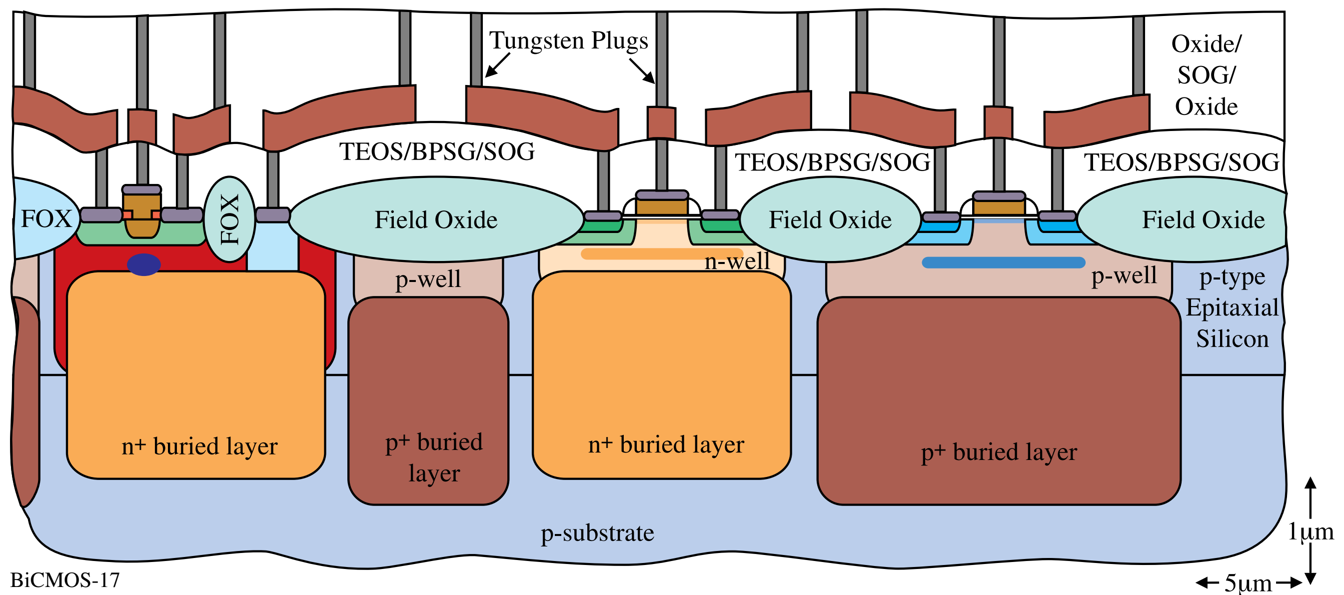
- A dielectric is deposited over the entire wafer
- One of the purposes of the dielectric is to smooth out the surface
- Tungsten plugs are used to make electrical contact between the transistors and metal1

Metal1



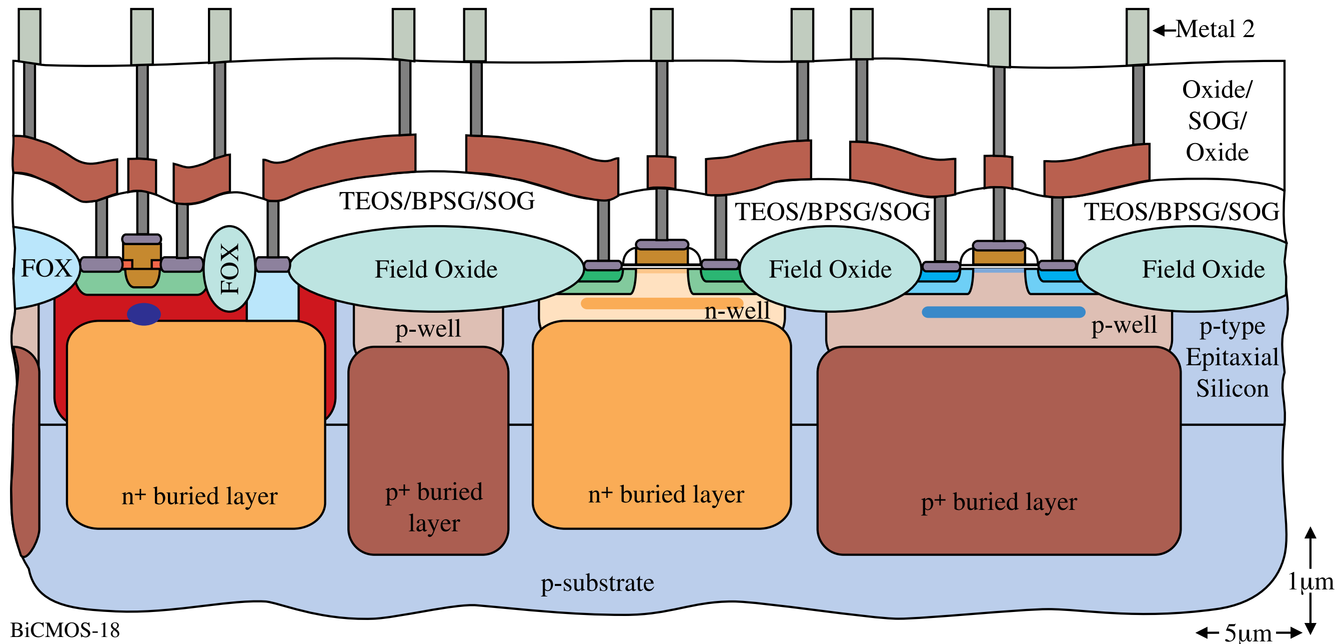
BiCMOS-16

Metal1-Metal2 Vias

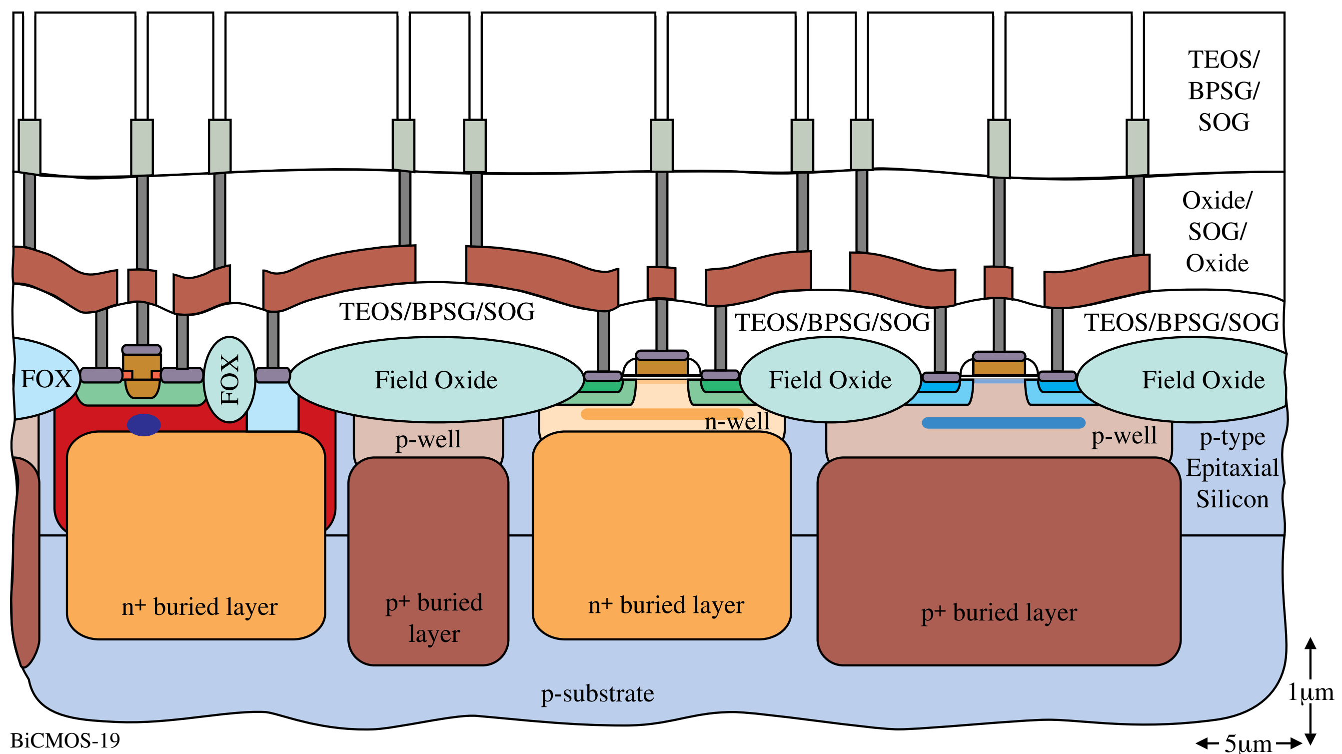


BiCMOS-17

Metal2



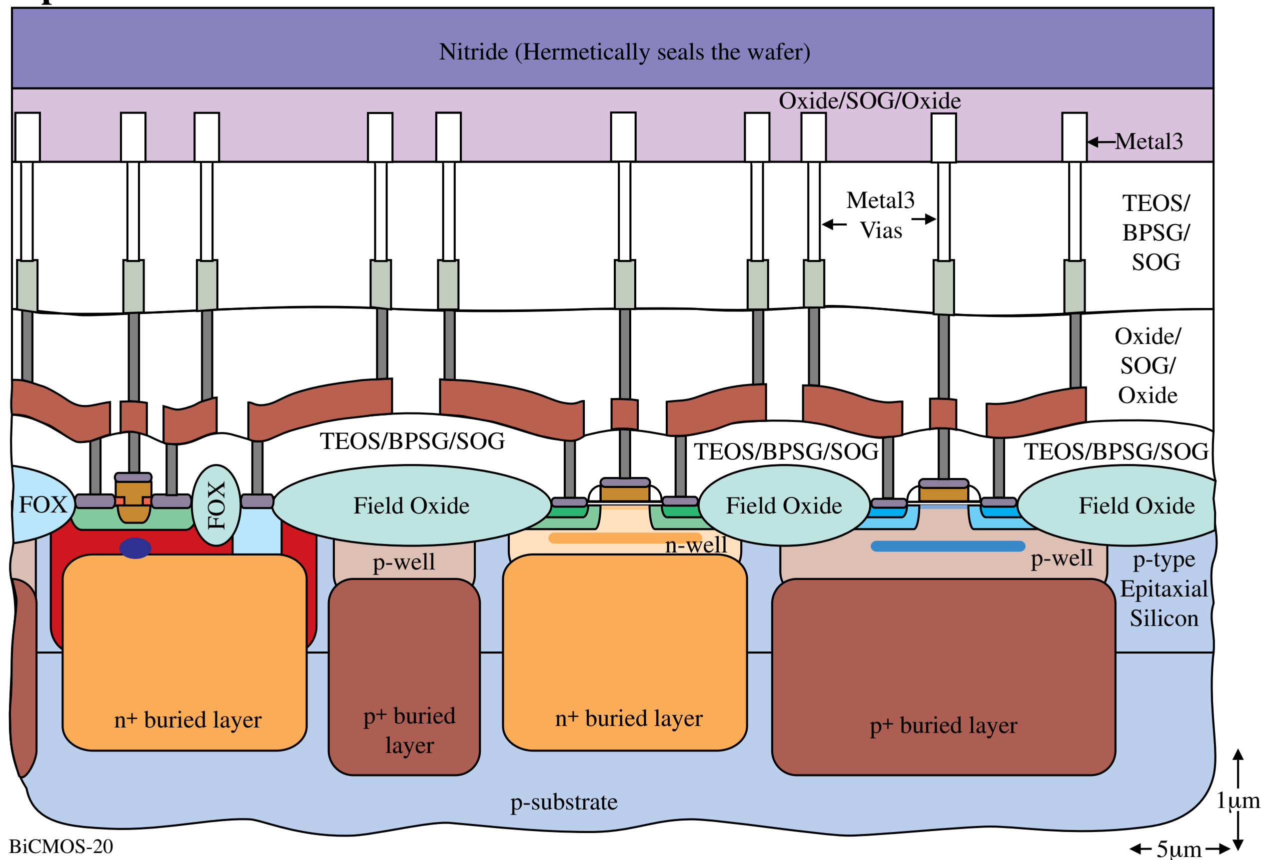
Metal2-Metal3 Vias



Comments:

- The metal2-metal3 vias will be filled with metal3 as opposed to tungsten plugs

Completed Wafer



SUMMARY

- This section has illustrated the major process steps for a 0.5micron BiCMOS technology.
- The performance of the active devices are:

  npn bipolar junction transistor:

  f_T = 12GHz, β_F = 100-140 BV_{CEO} = 7V

  n-channel FET:

  K' = 127µA/V^2 V_T = 0.64V $\lambda_N \approx 0.060$

  p-channel FET:

  K' = 34µA/V^2 V_T = -0.63V $\lambda_P \approx 0.072$

- Although today's state of the art is 0.25µm or 0.18µm BiCMOS, the processing steps illustrated above approximate that which is done in a smaller geometry.