CADENCE SETUP

This short tutorial shows how to configure Cadence to use the NCSU Cadence Design Kit (CDK) with access to the ON Semiconductor C5 0.5- μ m and the TSMC 0.35- μ m CMOS processes libraries.

In LINUX ◊ Right button of mouse -> Open Terminal



Make cadence directory

ece.gatech.edu> mkdir cadence

Oracle Move to cadence directory

ece.gatech.edu> cd cadence

\diamond Copy setup files (This should be done only once)

cp /tools/linsoft2/cadence/ic5141usr5/ncsu/cdssestup/cdsinit .cdsinit cp /tools/linsoft2/cadence/ic5141usr5/ncsu/cdssestup/cdsenv .cdsenv

♦ Edit cds.lib file

ece.gatech.edu> gedit cds.lib&

Add lines to cds.lib file

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♦ save and quit

◊ Source

> source /tools/linsoft2/cadence/ic612hf517/cshrc.meta

- > source /tools/linsoft2/cadence/ic612hf517/cshrc.ncsu61.lin
- > source /tools/linsoft2/cadence/mmsim71/cshrc.mmsim

If you edit .my-cshrc file, then you do not have to type this line always.

- How to edit my-cshrc file?
 - Go to root directory. ("cd").
 - gedit .my-cshrc&
 - Add line:
 - > source /tools/linsoft2/cadence/ic612hf517/cshrc.meta
 - > source /tools/linsoft2/cadence/ic612hf517/cshrc.ncsu61.lin
 - > source /tools/linsoft2/cadence/mmsim71/cshrc.mmsim
 - Save and quit
 - Go to cadence directory

Execution cadence

ece.gatech.edu> virtuoso &

◊ Tutorials

Below tutorials are useful materials. <u>http://www.eda.ncsu.edu/wiki/Tutorial:Contents</u> → Old Tutorials

• Analog Artist Tutorial http://www.cadence.ncsu.edu/NCSUCadenceTutorial/ArtistTutorial.pdf

<CAUTION> You should use the tech library and transistor model files of AMI 0.60 um technology. This is different from NCSTATE tutorial.

◊ Generation of a Cadence Library with attachment to an existing technology file

→ Generate Library with ON Semiconductor C5 0.5-µm In Library Manager, Click File -> New -> Library In the Name field, enter "Test" In the Technology Library box, select

Attach to existing tech library -> AMI 0.60u Press OK

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→ Generate Library with TSMC 0.35 um process

Do the same as shown above for generating a Library with the AMI 0.5 um tech file, but In the Technology Library box, select

Attach to existing tech library -> TSMC 0.40u CMOS035 (4M, 2P, HV FET) Press OK

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→ Making a cell for designing schematic In Library Manager, Click File -> New -> Cell View Select Library as "Test" In the Cell name field, enter "inv_test" In the type box, select "Schematic" Press OK

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→ Design a circuit (example: make a simple inverter) In schematic, press "I" for the component browser, and select library "NCSU_Analog_Parts", and "nmos4" in "N_Transistors". Find "pmos4" in "P_Transistors".

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→ Find proper sources (vdc, vsin) and ground (gnd) in Component Browser "AnalogLib" Library, and complete the circuit. (Wiring : press "w"). Also input the proper voltage for testing the circuit. (Select component and press "q") Save the schematic (Ctr + s).

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→ Select "Launch" -> "ADE_L" for the simulation.

→ Setup the simulator In Virtuoso Analog Design Environment, select "setup" -> "Simulator/Directory/Host", and select the "spectre" for the simulator. Press "OK"



→ Including transistor model file

In Virtuoso Analog Design Environment, select "setup" -> "Model Libraries", and add the model for AMI05.

- To use the ON Semiconductor C5 0.5-µm, browse and add 'ami06N.m' and 'ami06P.m' and 'ABN05'.
- For the TSMC 0.35-um process, browse and add the following transistor model files: 'tsmc35N.m' and 'tsmc35P.m'.

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The required transistor model files are located in /tools/linsoft/lincad/ic5141usr5/ncsu/models/spectre/standalone/.

*If you save the simulation state, then you don't need to setup model library and simulator again when you load your saved state. (Session -> Save state & Load state). Also you can load your saved sate for other schematic.

→ Choosing Analysis for the simulation In this example, transient simulation is selected. Click "OK" and run "Netlist and run" button.

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- ➔ To see the simulated waveforms, you might use calculator in "tools"-> "Calculator" in Virtuoso Analog Design Environment
- → For the transient waveforms, click "vt" (Voltage transient) and click the node where you want to see the waveforms.

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→ After simulation is done, you might make a symbol for the circuit. Add the proper pins for inputs and outputs of your circuit. (Hot key "p") Then click "Create"->"Cellview"->"From Cellview" to create symbol.





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➔ To create layout, you can create "layout" as same way to create "schematic". Just change the type to "layout".

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- → Create instance (hotkey: "I"), and find "nmos" and "pmos" in NCSU_TechLib_ami06 for AMI05. (NCSU_TechLib_tsmc03 for tsmc035 process)
- → Check the parameters are same in schematic design. (hotkey: "q" on the component)
- → Complete the layout with proper input and output pins in your schematic (Pin location hotkey: "Shift+p")

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→ For DRC, select "Verify"->"DRC" in the layout window.

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→ After DRC, you can see the results in the log file.

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→ After DRC has passed, create extracted circuit using "Verify"-> "Extract"

→ Then, you can see the extracted circuit in the cell view.



➔ For LVS, click "Verify"->"LVS", and select the extracted view. Left side should be your schematic, and right side should be its extracted circuit. Rule file is located on "/tools/solsoft/solcad/ic610/ncsu-cdk-1.6.0.beta/techfile/divaLVS.rul"

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- → Check LVS rule is correct. You can see the modify LVS Rules in "NCSU"-> "Modify LVS Rules" to change the options.
- → Run "LVS", and click "Output" to see the error reports.

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mouse L: showClickInfo()	M: schHiMousePopUp()	R: schHiMo	F/151 Mouro	V. 795 V. 165 (ES/Salact 0, Salah 0, DED: OFF, CA	E. OFF. dV: 1.65. dV: 10.05. Dist 10.195

< When LVS has errors : ptap and ntap for body terminals are missing >

C /nethome/yjis48/ECE_6414_PROJECT/LVS/si.out	🔣 Virtuoso Layout Suite L Editing: Test inv_test layout	
Elle Help	Launch Eile Edit View Create Verify Connectivity Options Tools Window Assura NCSU Help Car	denc
0(#)\$CDS: LVS version 6.1.2 08/28/2008 03:19 (cic6121mx) \$		
Command line: /tools/linooft2/cadence/ic612hf517/tools.lnxd6/dfII/bin/32bit/LVS -dir /netho Like matching is enabled Using terminal names as correspondence points.		
Net-list summary for /nethome/yjia48/ECE_6414_PR0JECT/LVS/layout/netlist		
4 terminals 1 page 1 1 nos		
Net-list summary for /nethome/yjia48/EOE_6414_PROJECT/LVS/schematic/netlist count 4 nets		
4 terminais 1 pnos 1 nnos		
Torsial correspondence points M4 M1 M3 N1 OUT M5 N0 VD0		
nz ns rss Devices in the rules but not in the netlist: res cap nfet pfet nacs4 pmos4		
Ill-defined correspondence points.	n an	
 ND Accepted because one is a subset of the other N2 Accepted because one is a subset of the other N0 Accepted because one is a subset of the other N2 N3 Accepted because one is a subset of the other 		
Device summary for layout bad total page 1 1		
TIROS 1 1	Il mouse L: showClickInfo() M: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9) R: _MHiMouse	ePopUp
	- 6/151	151 0

< When LVS has completed : Let-lists are matching in schematic and layout >

