Name ________________ Grade = /100
(1 point)

ECE 4430 Midterm Exam
Fall 2017

Each question is worth 3 points.
All of your answers need to be on this sheet.
Only the final answers, as indicated by the question, will be considered correct for each question.
You will only turn in this single sheet.

1. ________________	12. ________________	23. ________________
2. ________________	13. ________________	24. ________________
3. ________________	14. ________________	25. ________________
4. ________________	15. ________________	26. ________________
5. ________________	16. ________________	27. ________________
6. ________________	17. ________________	28. ________________
7. ________________	18. ________________	29. ________________
8. ________________	19. ________________	30. ________________
9. ________________	20. ________________	31. ________________
10. ________________	21. ________________	32. ________________
11. ________________	22. ________________	33. ________________

A few items to be used for this exam:

EKV equation in saturation, including σ:

$$I = 2\, I_{th} \ln^2\left(1 + \exp\left((\kappa(V_g - V_{T0}) - Vs - \sigma V_d)/ (2U_T) \right) \right)$$

For $z = \ln^2(1 + e^y)$, dz / dx (at $y = 0$) $= 0.5\, dy/dx$.

Parameters for devices (unless given otherwise)

$V_{T0} = 0.3V$

$K' = 0.14mA / V^2$

$I_{th}' = 125nA$

$\kappa = 0.7$

$\sigma = 0.001$, $V_A = 25V$ ($L = 800nm$)

Transistors are devices in a 200nm minimum (drawn) channel length process.

For drawn grids, a single grid step is 100nm.

$Cox = 0.1fF/ (100nm)^2$
Overlap capacitance = 0.1fF / (100nm)
Area source-drain capacitance at zero bias = $0.01fF/ (100nm)^2$
Perimeter source-drain capacitance at zero bias = 0.003fF / (100nm)

Small Signal Model Questions

You have a circuit design you want to bias *right at the threshold current* for your particular application. Use the value of σ given (0.001, or V_A = 25V), which is consistent for all regions of operation. Choose the closest answer wherever necessary.

1. How would you size your device (nearest size) if you wanted a bias current of 1μA operating at right at threshold?
a. W/L = 2
b. W/L = 4
c. W/L = 8
d. W/L = 16
e. W/L = 32

2. What is your transconductance (change in channel current for change in gate voltage) for this 1μA bias current at threshold?
a. 5 μA/V
b. 10 μA/V
c. 14 μA/V
d. 20 μA/V

3. What is your source conductance (change in channel current for change in source voltage) for this 1μA bias current at threshold?
a. 5 μA/V
b. 10 μA/V
c. 14 μA/V
d. 20 μA/V

4. What is your output resistance (1 / change in channel current for change in drain voltage) for this 1μA bias current at threshold?
a. 5MΩ
b. 10MΩ
c. 25MΩ
d. 50MΩ
e. 100MΩ

5.(A = true, B = False) If one use W/L = 1 (still for a 1μA bias), the saturated transistor is operating with subthreshold currents.

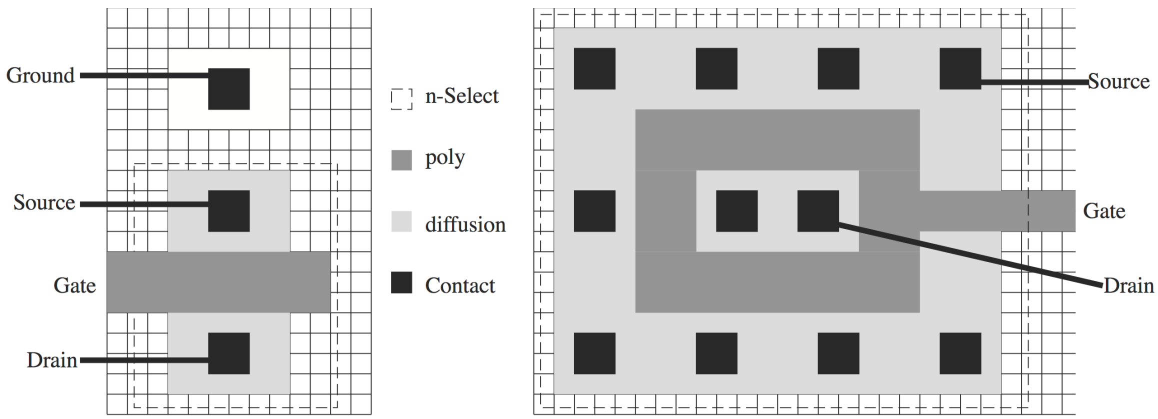
6. What is the transconductance of the MOSFET with W/L=1 for a 1μA bias?
a. 5 μA/V
b. 7 μA/V
b. 10 μA/V
c. 14 μA/V
d. 20 μA/V

7.(A = true, B = False) For our devices operating with 1μA bias current, the output resistance of the transistor biased at threshold current (saturation) would be the same for the device at W/L=1 (saturation).

8. (A = true, B = False) For our devices, the transistor gain would be the same between the transistor biased at threshold current would be the same for the device at W/L=1 and operating in saturation (both at 1μA bias current).

Transistor Layout Questions

These questions will refer to the following MOSFET transistor layouts. Transistors are biased with subthreshold currents (10nA) unless otherwise mentioned.



A B

MOSFET A

9. The overlap capacitance (Cdg):
a. 0.2fF
b. 0.4fF
c. 0.6fF
d. 0.8fF
e. 1fF

11. Capacitance from your drain region to substrate (Cdb):
a. 0.17fF
b. 0.23fF
c. 0.29fF
d. 0.32fF
e. 0.41fF

13. Capacitance from your source region to substrate (Csb):
a. 0.17fF
b. 0.23fF
c. 0.29fF
d. 0.33fF
e. 0.41fF

15. Capacitance looking into the Gate (Cgb) (subthreshold bias current):
a. 0.14fF
b. 0.27fF
c. 0.54fF
d. 1.2fF
e. 1.8fF

MOSFET B

10. The overlap capacitance (Cdg):
a. 0.3fF
b. 0.6fF
c. 1.2fF
d. 1.8fF
e. 2.4fF

12. Capacitance from your drain region to substrate (Cdb):
a. 0.17fF
b. 0.23fF
c. 0.29fF
d. 0.32fF
e. 0.41fF

14. Capacitance from your source region to substrate (Csb):
a. 0.3fF
b. 0.6fF
c. 1.25fF
d. 2.5fF
e. 5fF

16. Capacitance looking into the Gate (Cgb) (subthreshold bias current):
a. 4fF
b. 6fF
c. 8fF
d. 10fF
e. 12fF

MOSFET A

17. Transistor W/L

a. 1
b. 2
c. 4
d. 8
e. 16

MOSFET B

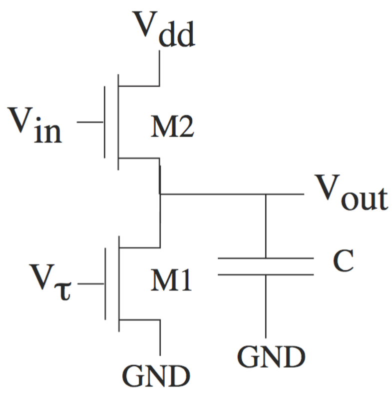
18. Transistor W/L

a. 1
b. 2
c. 4
d. 8
e. 16

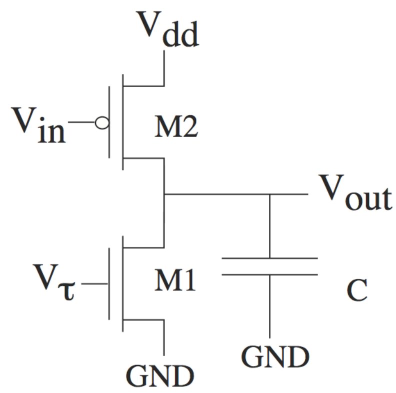
19. (A = true, B = False): We can use V_{gs} because for a MOSFET in a bulk CMOS process, the gate and source have the equal, although different sign, effects on the transistor surface potential.

<u>Basic Transistor Circuit Questions</u>

These questions will refer to the following MOSFET transistor circuits. C = 100fF. Vdd = 1.5V. Use W/L = 800nm / 800nm unless otherwise directed.



A



B

<u>Circuit A</u>

20. Circuit Type
a. Common Gate 1
b. Common Source
c. Common Gate 2
d. Common Drain

22. W/L (M2) required to obtain a corner frequency of 100MHz for a bias current of 2μA. (ignore parasitic capacitors)
a. 1
b. 2
c. 4
d. 8
e. 16

24. Corner frequency (20nA bias current)
a. 1.25MHz
b. 2.5MHz
c. 5MHz
d. 10MHz
e. 20MHz

26. What is the value for Vτ (20nA bias current)
a. 0.23V
b. 0.27V
c. 0.3V
d. 0.33V
e. 0.37V

<u>Circuit B</u>

21. Circuit Type
a. Common Gate 1
b. Common Source
c. Common Gate 2
d. Common Drain

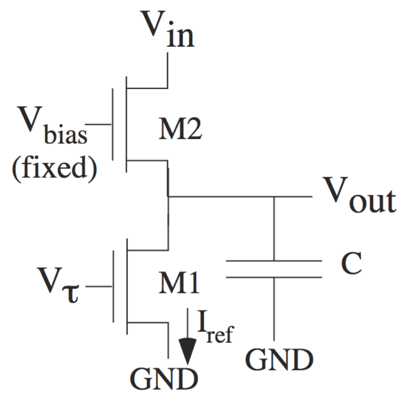
23. Minimum W/L (M1=M2) possible to obtain a corner frequency of 1MHz for a bias current of 2μA. (ignore parasitic capacitors)
a. 1
b. 2
c. 4
d. 8
e. 16

25. Circuit Gain (Magnitude, 20nA bias current)
a. 175
b. 350
c. 700
d. 1400
e. 2800

27. What minimum length would be required for a gain (magnitude) over 1000?
a. 1000nm
b. 1500nm
c. 2000nm
d. 2500nm
e. 3000nm

Another Transistor Circuit Question

This question uses the following circuit.
C = 10pF.



28. Circuit Type
a. Common Gate 1
b. Common Source
c. Common Gate 2
d. Common Drain

29. Gain from V_{in} to V_{out} for a subthreshold bias current
a. 10
b. 1
c. 0.1
d. 0.01
e. 0.001

30. Corner Frequency for I_{ref} =16nA
a. 100Hz
b. 1kHz
c. 10kHz
d. 100kHz
e. 1MHz

31. For I_{ref} at 10nA, what is the change in output voltage if this current (Iref) moves to 20nA?
a. -40mV
b. -20mV
c. 0
d. 20mV
e. 40mV

32. (A = true, B = False): For frequencies above the corner frequency, the gain from V_{in} to V_{out} increases with frequency.

33. What is the minimum W/L (M2) to have a corner frequency of 1MHz?
a. 0.1
b. 1
c. 10
d. 100
e. 1000