A Low-Power Programmable Bandpass Filter Section for Higher Order Filter Applications

David W. Graham, *Member, IEEE*, Paul E. Hasler, *Senior Member, IEEE*, Ravi Chawla, *Member, IEEE*, and Paul D. Smith, *Member, IEEE*

***Abstract*—We present a programmable, continuous-time bandpass filter that is extremely compact, power efficient, and can cover a wide range of frequencies (10 Hz–10 MHz). This capacitively coupled current conveyor (C^4) has a second-order bandpass transfer function and is capable of being used as a basic bandpass-filter element to create high-order filters. The use of floating-gate transistors helps to ease the difficulties of effectively utilizing G_m–C filters by providing precise, programmable current sources that set the filter's time constants. Additionally, we provide an algorithmic design approach for constructing these bandpass filters to meet any given specifications. This bandpass filter is ideally suited to large filter-bank applications because of its small size and low-power demands.**

***Index Terms*—Auto-zeroing floating-gate amplifier (AFGA), capacitively coupled current conveyor (C^4), electron tunneling, floating-gate (FG), hot-electron injection, programmable analog, quality factor (Q).**

I. Motivation for Low-Power, Tunable Filters

With the increasing trend of designing power-efficient analog circuits for portable applications, the demand is high for analog filters with better performance in terms of speed and power consumption. Continuous-time filters, particularly G_m–C filters, are the most often used solution for signal frequencies of several megahertz [1] as problems such as jitter and high dynamic power make discrete-time filters impractical at such frequencies. Irrespective of the frequency of operation, G_m–C filters suffer from limited linearity, a large overhead of tuning circuitry, and offsets due to device mismatch [2]–[4].

To address these common issues with G_m–C filter implementations, we present a programmable continuous-time bandpass-filter section that is also compact and power efficient. Fig. 1 shows this programmable filter element, referred to as the capacitively coupled current conveyor (C^4). This programmable filter section incorporates our programmable CMOS technology, which is based on modified EEPROM elements designed to work in a standard CMOS technologies and which greatly reduces overhead for tuning circuitry and the effects of device mismatch [5]. We present design equations for the C^4 that allow for easy synthesis to meet required specifications. We also present the design of high-order filters using our programmable filter element, as is depicted by the cascade of our filter sections in Fig. 1. These high-order filters can easily be tuned to desired transfer functions, such as Butterworth or Chebyshev, after fabrication by simply programming floating-gate current sources.

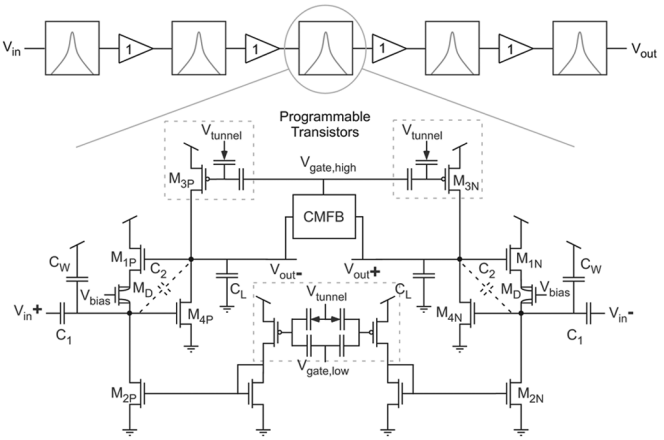

Fig. 1. Capacitively coupled current conveyor (C^4). The C^4 is a continuous-time bandpass filter with electronically tunable time constants that are independent of each other. Programmability of the time constants can be achieved by using floating-gate transistors as current sources to set each time constant. The C^4 can be used as a modular element for creating high-order filters, as is depicted; the C^4s are arranged in a cascade with a buffer between each stage.

The rest of this paper describes the basic operation and design of the C^4 bandpass filter. In Section II, we give a general overview of the C^4, especially geared towards wide-bandwidth applications. Then, in Section III, we focus on the design of the C^4 for narrow bandwidth applications and develop a set of synthesis equations for designing C^4s to meet given specifications. Section IV describes the use of the C^4 in constructing high-order filters, and Section V summarizes the performance of this bandpass filter.

II. C^4 Programmable Bandpass Element

The capacitively coupled current conveyor (C^4), shown in Fig. 1, is a very compact, capacitively based bandpass filter. Fig. 2(a) shows the single-ended version of the C^4 which will

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D. W. Graham was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332-250 USA. He is now with the Lane Department of Computer Science and Electrical Engineering, West Virginia University, Morgantown, WV 26506-6109 USA (david.graham@mail.wvu.edu).

P. E. Hasler is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-250 USA (e-mail:phasler@ece.gatech.edu).

R. Chawla was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-250 USA. He is now with Silicon Laboratories Inc., Austin, TX 78701, USA.

P. Smith was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-250 USA. He is now with GTronix Fremont, CA 94538 USA.

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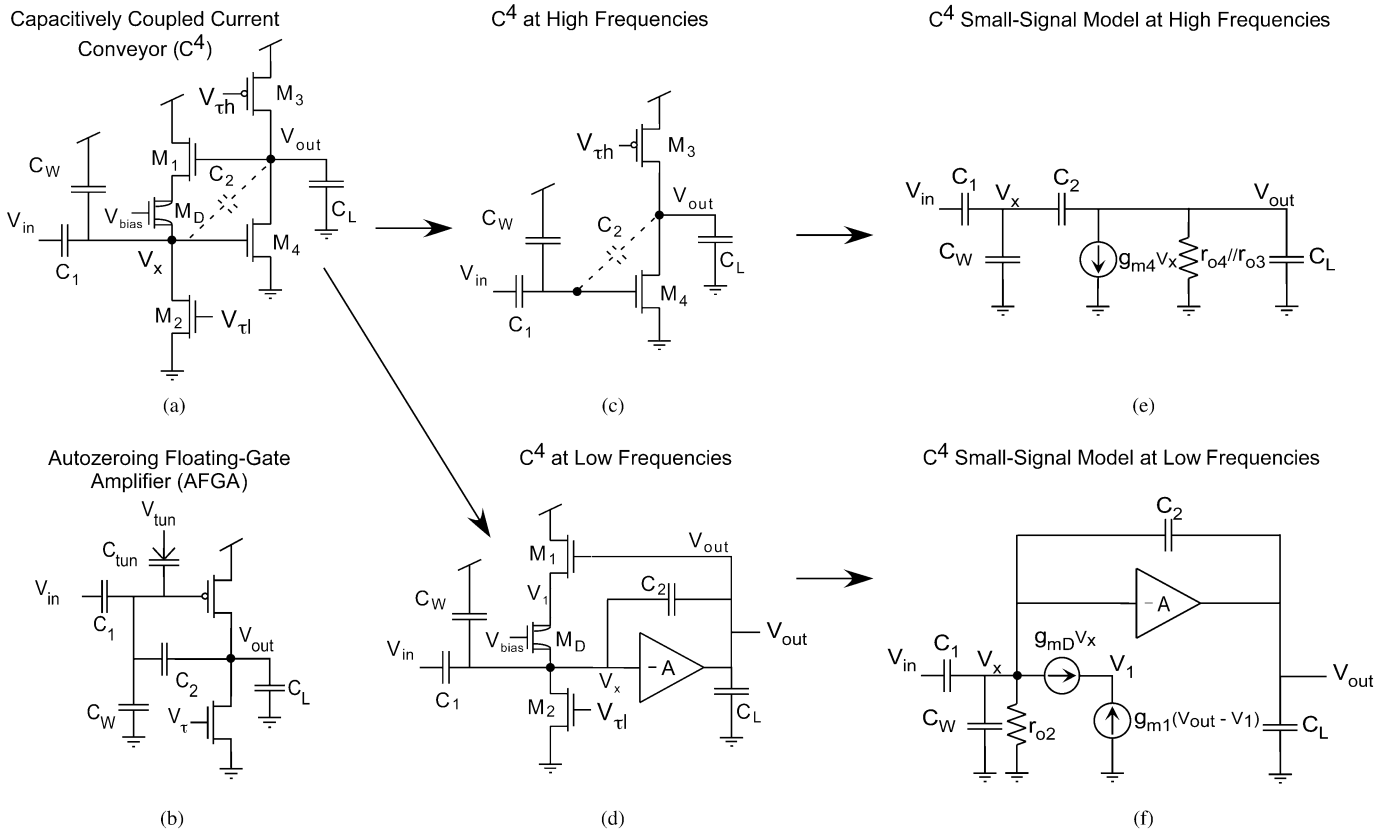

Fig. 2. Qualitative description of the C^4. (a) C^4 schematic. The time constants are set by the current-source transistors M_3 (high-frequency corner) and M_2 (low-frequency corner). (b) The C^4 approach has its roots in the AFGA circuit [6]. The upper time constant is set by the current-source transistor, and the lower time constant is set by the balance of electron tunneling and hot-electron injection. (c) Equivalent circuit schematic of the C^4 at high frequencies in which the feedback loop has minimal effect on the circuit response. (d) Equivalent circuit schematic of the C^4 at low frequencies in which the common-source amplifier with transistor M_4 acts as a constant gain amplifier with gain A. (e) Small-signal model for the high-frequency equivalent circuit. (f) Small-signal model for the low-frequency equivalent circuit.

be helpful in performing some of the analysis in this paper. We presented an early version of the single-ended C^4 in [7], [8], and it has been shown to be useful in systems applications [9].

The design of this programmable C^4 filter was inspired by creating an all-transistor version of the autozeroing floating-gate amplifier (AFGA) [10] [Fig. 2(b)] primarily as a tool to explain the AFGA's bandpass circuit dynamics. The bias-current level between the hot-electron injection and tunneling current sets the low-frequency AFGA time-constant, which can range from milliseconds to days. The C^4 was modified such that both time constants can be set using transistor currents, and the resulting circuit, shown in Fig. 2(a), is a simplified half circuit of the C^4 [7]. By adding programmability through floating-gate transistors and common-mode feedback through a standard differential amplifier [11] with high loop gain, the complete C^4 is as shown in Fig. 1. One can imagine the amplifiers (common-source and common-drain amplifiers) being replaced with other amplifiers (e.g., OTAs) where one can get further control of the characteristics and even include programmable devices for the resulting amplifiers.

A. High-Frequency Behavior of the C^4

Fig. 2(c) shows the reduced circuit to illustrate the high-frequency behavior of the C^4 (when the corner frequencies are significantly separated), and Fig. 2(e) shows the resulting small-signal circuit. From this circuit, the resulting transfer function is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_1}{C_2}\frac{1 - s\tau_f}{1 + s\tau_h} \tag{1}$$

where the time constants are given by

$$\tau_h = \frac{\left(C_T C_O - C_2^2\right)}{C_2 g_{m4}} \quad \tau_f = \frac{C_2}{g_{m4}} \tag{2}$$

and where the total capacitance and the output capacitance are given by $C_T = C_1 + C_2 + C_W$ and $C_O = C_2 + C_L$, respectively. The capacitances C_T, C_2, and C_O include drawn and parasitic capacitances. The passband gain of the filter element is set by capacitor ratios as $A = -C_1/C_2$. The zero in this expression, determined by τ_f, is due to capacitive feedthrough from the input to the output of the amplifier, or the effective circuit when operating at a sufficiently high frequency such that the amplifier behavior on the output voltage is negligible. The capacitive feedthrough normally has little effect on the bandpass-filter operation in either frequency or amplitude; the resulting feedthrough gain and τ_f should be calculated to verify this assumption when designing a specific C^4 filter.

From the simplified circuit of Fig. 2(c) and (e), we can estimate the noise and the signal-to-noise ratio (SNR) for this wide-band amplifier. The output thermal-noise voltage

integrated over the entire bandwidth of interest (set by τ_h) is computed as

$$V_{\text{noise}} = \sqrt{q\left(\frac{I_4}{g_{m4}}\right)\frac{C_T}{C_O C_2}} \tag{3}$$

where $q = 1.6 \times 10^{-19} C$, and I_4 is the bias current flowing through M_4. For the wide-band case for the complete C^4, the noise is divided by a term that is typically close to unity and is given by $1 + g_{m1}(C_O/C_2 - 1)/(\kappa g_{m4})$. For subthreshold-current levels, the noise takes on the form of kT/C noise where the effective capacitance is $\kappa C_2(C_O/C_T)$.

When designing a C^4, the $1/f$ noise corner frequency should be determined for the given biasing conditions; if the $1/f$ corner is not in the passband, then the effect of $1/f$ noise can be neglected. We describe the functional form of the $1/f$ noise spectrum for a transistor threshold voltage of $K_f df/(WLf)$, where K_f is a process dependant empirical parameter (measured values in the range of 500 $u\text{V}^2$ μm^2 for 0.5- and 0.35-μm CMOS processes, and f is a particular frequency of interest. We describe the $1/f$ corner frequency, the frequency where the $1/f$ noise is equal to the thermal noise, for a given bias current (I_{bias}) as

$$\frac{\kappa^2 K_f}{2U_t^2 WLq} I_{\text{bias}} \text{ (sub } V_T\text{) and } \frac{K\kappa K_f}{WLq} \text{ (above } V_T\text{).} \tag{4}$$

Therefore, the $1/f$ corner frequency decreases linearly with decreasing subthreshold bias current, just as the frequency response decreases linearly with decreasing subthreshold bias current. For a wide-band filter ($Q < 0.5$), one must consider how the $1/f$ noise generated by I_1 and I_2 affects the system; for most filters with moderate Q ($Q > 0.5$), pushing the $1/f$ noise out of the band of interest is straightforward if even a problem at all. For a wide-band filter, the high-frequency, low-pass filter corner easily is above the $1/f$ noise corner frequency, but depending upon how wide the passband might be, some $1/f$ noise might appear in the passband region. In this case, the noise increase is a small percentage increase on the total noise described in (3). The low-frequency, high-pass filter corner frequency typically starts above the $1/f$ corner frequency, or might require a slightly longer device length or higher C_2 capacitor to push the $1/f$ corner frequency below the signal corner frequency. Again, even if the $1/f$ corner frequency is at or slightly above the signal $1/f$ corner frequency, the total noise described in (3) remains roughly uneffected.

The output-referred linear range is given by $U_T C_T/(\kappa C_2)$ (subthreshold operation) and $V_{\text{on}} C_T/C_2$ (above-threshold operation), assuming $C_T C_O \gg C_2^2$ and that $V_{\text{on}} = \kappa(V_g - V_T) - V_s$ is the overdrive voltage at the bias condition. The linearity is set by choosing the desired capacitor value for C_W, which results from the capacitive attenuation at the input, and the linearity of the follower feedback amplifier (V_L). Linearity for low Q ($Q < 0.5$) is effectively looking at the linearity of the two resulting first-order systems; nonlinear analysis changes for higher Q, as we will discuss in Section III. Identifying the linear range terms for this circuit are critical for a nonlinear analysis of a G_m–C filter, as the normalization parameter computed for the given topology. Once these two parameters are determined, the nonlinear responses (distortion, two-tone responses) are explicitly known. For a differential signal (input or output) equal to the linear range of the high-gain (M_4+capacitive network) or follower (M_1) amplifier structure, we get maximum -46 dB and -44 dB, respectively, two-tone harmonic distortion occurring at the respective corner frequencies. The distortion amplitude decreases further in the passband. Harmonic distortion increases as a cubic function of the input amplitude from the linear range amplitude. We will anchor the signals at the linear range of the amplifier; therefore, for a larger or smaller desired amplitude one could either directly modify the linear range parameters at design time and/or directly calculate the resulting distortion for the given linear ranges of the amplifier. We will discuss more about the distortion for the moderate Q case in Section III. The resulting SNR for this amplifier is

$$\text{SNR} = 10\log_{10}\left(\frac{1}{q}\left(\frac{I_4}{g_{m4}}\right)\frac{C_T C_O}{C_2}\right). \tag{5}$$

The SNR is directly increased by the product of $C_T C_O$ divided by C_2, resulting in significantly smaller capacitor sizes for a given SNR than can be achieved by using other G_m–C techniques.

B. Low-Frequency Behavior of the C^4

Fig. 2(d) shows the reduced circuit to illustrate the low-frequency behavior of the C^4 (in the case of widely separated corner frequencies), and Fig. 2(f) shows the resulting small-signal circuit. The primary assumption is that the amplifier between V_X and the V_{out} has a constant gain, A, because transistors M_3 and M_4 form a high-gain inverting amplifier that yields a constant gain over the frequency range of interest. Assuming that $A \gg 1$, the resulting transfer function is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_1}{C_2}\frac{s\tau_l}{s\tau_l + 1} \text{ where } \tau_l = \frac{C_2}{g_{m1}}. \tag{6}$$

C_2 includes the overlap capacitance of M_4 and also the capacitance from the gate of M_1 to the source of M_D, which is small since M_D cascodes M_1. M_D is a short-channel device ($0.5\text{ V} < V_A < 10\text{ V}$) that is used to increase the linearity from V_{out} back to V_X. This linear range, which is given by $V_{L1} = I_1/g_{m1}$, typically falls between 0.5 and 10 V.

C. Bandpass Behavior of the C^4

The low- and high-frequency time constants can be set independently of each other by tuning g_{m1} and g_{m4}, respectively, which is done by tuning the bias currents flowing through transistors M_1 and M_4. The transfer function incorporating both the low- and high-frequency responses is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_1}{C_2}\frac{s\tau_l(1 - s\tau_f)}{1 + s\left(\tau_l + \tau_f\left(\frac{C_O}{C_2} - 1\right)\right) + s^2\tau_h\tau_l}. \tag{7}$$

Fig. 3(a) shows the frequency response of the C^4 illustrating that both high (10, 11, 12 kHz) and low (100, 200, 300 Hz) corners can be individually tuned to the desired frequencies accurately. As is shown in Fig. 3(b), the C^4 can be biased to give a low-pass response (high-frequency approximation), a high-pass

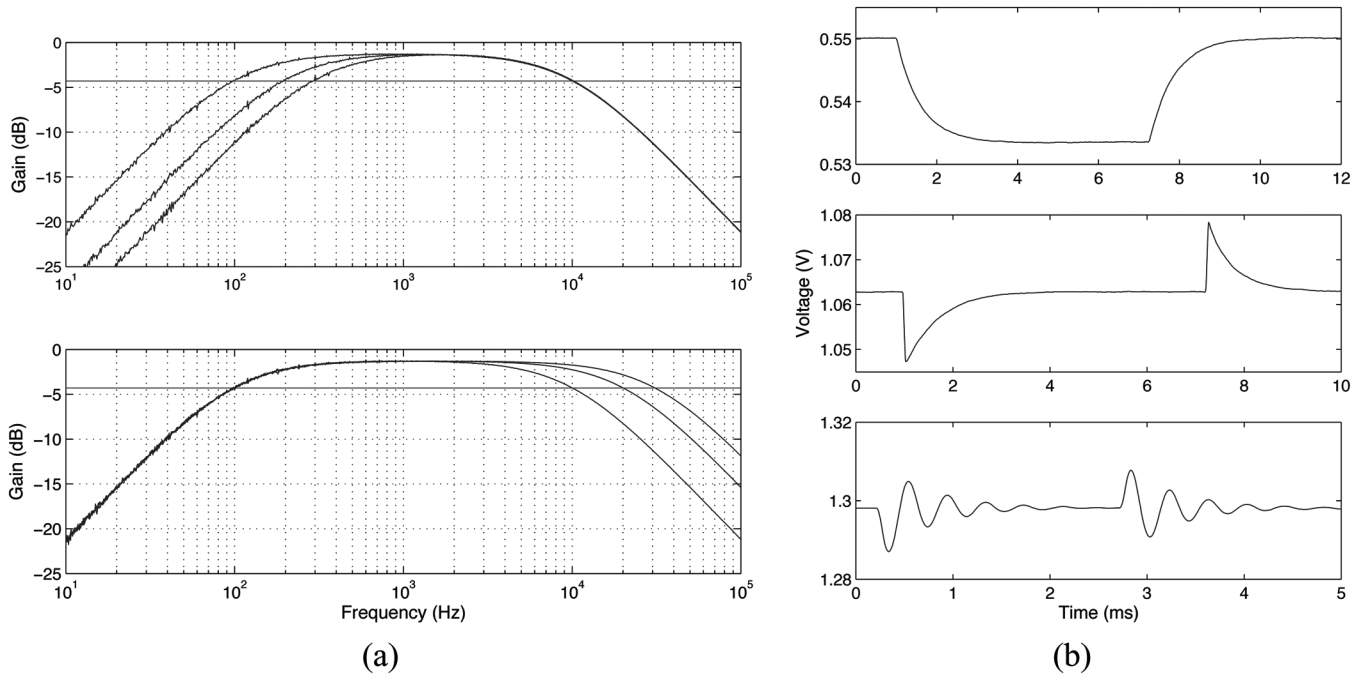

Fig. 3. Experimental measurements from a C^4 illustrating various modes of operation. (a) Frequency response of the C^4 for widely tuned corner frequencies. These measurements show that the tuning of the high- and low-corner frequencies are independent of each other. (b) Step response of the C^4. (Top) Step response of the C^4 when biased as an integrator. (Middle) Step response of the C^4 when biased as a differentiator. (Bottom) Step response of the C^4 when the two corner frequencies have crossed each other.

response (low-frequency approximation), or a combination of the responses leading to resonance.

D. C^4 Programmability Through Floating-Gate Transistors

The designed filters are programmed to a desired bias current using floating-gate devices; programming matches devices and reduces distortion components due to mismatch issues. We have presented a general overview of floating-gate devices elsewhere [10], [12]–[14], and we also give a short overview on programming current sources for C^4 filters here. Fig. 4(a) shows the layout cross-section of our floating-gate device along with programming a single device in an array. A floating gate is a MOS gate surrounded by silicon-dioxide with no dc path to ground. Charge on the floating gate is stored permanently, providing a long-term memory because it is completely surrounded by a high-quality insulator. The floating-gate voltage, determined by the charge stored on the floating gate, can modulate a channel between a source and drain, and, therefore, can be used in computation. Our programming scheme is based on using both hot-electron injection and electron tunneling. We use these techniques in standard CMOS processes.

One of the critical aspects in the design of the programmable filters is programming accuracy. Our adaptive programming method enables us to perform accurate and fast programming [5], [7]. Fig. 4(b) shows a measurement of a programmed 5-nA$_{pp}$ sine wave riding on a 10-nA dc current for a 1×128 array. The programmed current shown in Fig. 4(b) is related to the charge stored on each floating-gate node. We obtained a worst case programming error of 0.2% and it takes 10 or fewer pulses of 100-μs pulses for programming each floating gate transistor.

While the accuracy of the programmed current, itself, will not achieve perfect responses out of the bandpass filter due to device mismatch, floating-gate programming provides an easy mechanism for achieving high accuracy in tuning the filter's poles and zeros. By performing a single calibration step, as we described in [15], the C^4's corner frequencies may be placed at any desired location very precisely. By measuring the output of the C^4 (taking a frequency response, step response, or some other system metric) after performing an initial program of the floating-gate transistor currents, the known bias currents and the measured time constants can be compared to find the exact current that must be programmed into the floating-gate transistors to achieve the desired response. Since these currents can be set precisely, the time constants of the C^4 can also be set precisely. This calibration step, which only needs to be performed once, has the added advantage of accounting for device mismatch and, hence, decreasing the variability the filter parameters (corner frequencies, quality factor, etc.).

E. Input Impedance of the C^4

One characteristic of the C^4 that must be accounted for when cascading C^4s for high-order filters (Fig. 1) is that the input impedance of the C^4 varies with frequency. Therefore, the effective load capacitance seen by one stage will vary with frequency because the next stage's input impedance varies with frequency. This shift could potentially modify the target response in an un-designable fashion. However, by increasing C_W such that it becomes the dominant capacitance, the frequency dependence of the input impedance decreases, as is shown in Fig. 5(c), because the V_X node becomes more constant with frequency. Another approach to achieve designed transfer functions is to use a unity-gain buffer between each stage. Fig. 1

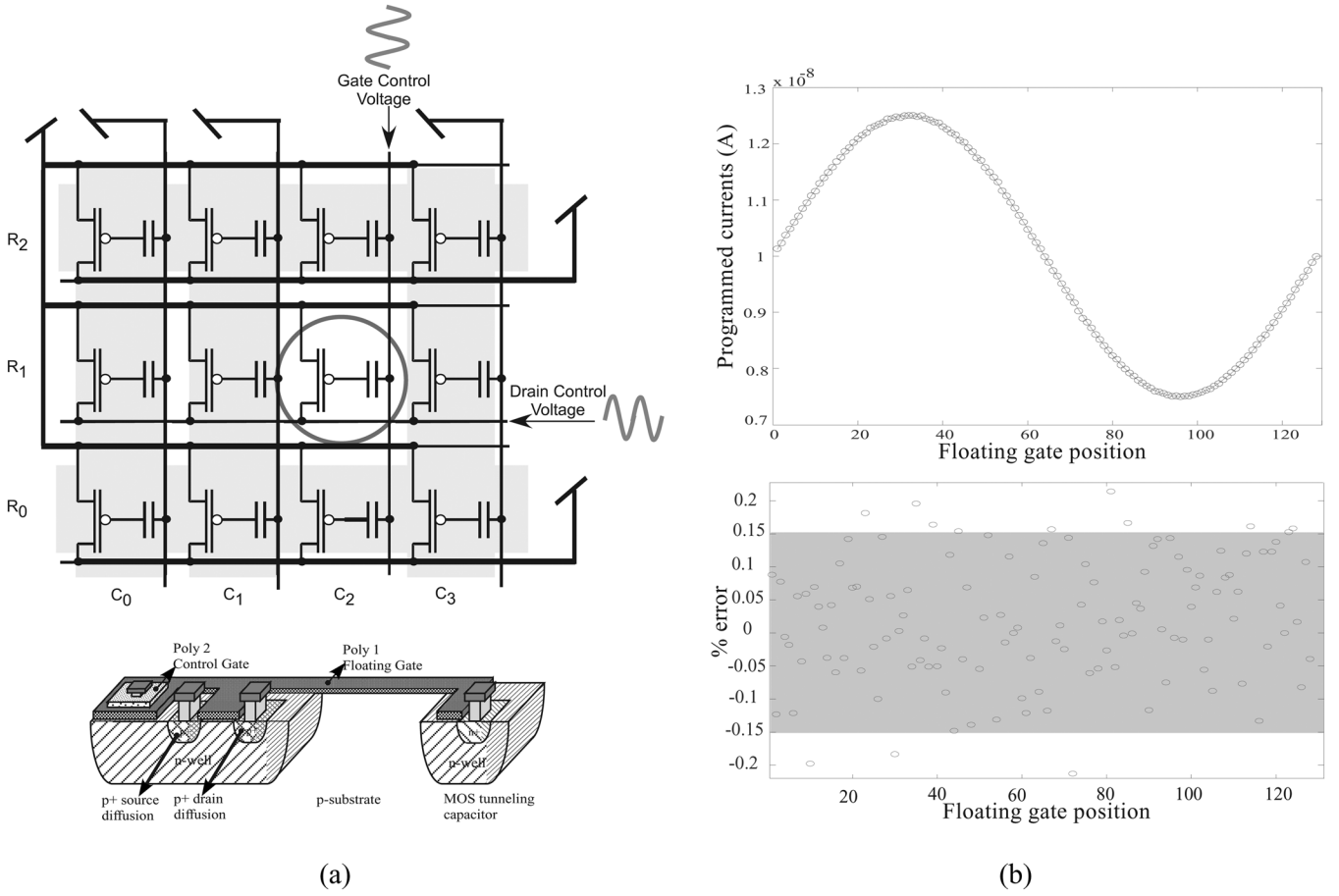

Fig. 4. Floating-gate MOS device. (a) Array of floating-gate devices that can be programmed individually along with the cross-section of a floating-gate transistor. The floating-gate device is a standard pFET transistor in an n-well process. The floating-gate charge can be changed by using electron tunneling and hot-electron injection processes. Each device can be selected by connecting the nonselected row (drain) and column (gate) lines to V_{dd}; therefore, the remaining desired device can be characterized as well as strengthened through hot-electron injection. [5]. (b) Measurement showing the output waveform when a single column (128 floating-gate devices) are programmed to have a 5-nA$_{pp}$ sine wave riding on a 10-nA dc current. The worst-case programming error was 0.2% for a programming time of 1 ms.

shows that we have used buffers to isolate stages, where the buffer was designed to have a good frequency response and linearity and, thus, had no effect on the performance of the system other than dissipating more power and contributing slightly to the output noise levels.

III. C^4 Bandpass Element With Resonance ($Q > 0.5$) for Practical Applications

In the previous section, we considered the general case for the C^4 bandpass filter; in this section, we will focus on using the C^4 filter as a bandpass filter with a narrow passband region (with resonance). We will focus on a procedure that allows the algorithmic design of C^4 filters. When designing C^4 filters for high linearity and high SNR, $C_T = C_1 + C_2 + C_W \gg C_1, C_2$, and $C_O = C_2 + C_L \gg C_2$. We also assume that the capacitive feedthrough term (the τ_f term) has a negligable effect on the transfer function in the region of interest.

A. General Directions for $Q > 1$

By moving the time constants close to each other, the C^4 takes on a bandpass response. Crossing the time constants introduces resonance into the filter response, as shown in Fig. 5(b). The resulting transfer function is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_1}{C_2}\frac{\frac{sC_2}{g_{m1}}}{1 + s\left(\frac{C_2}{g_{m1}} + \frac{C_o}{g_{m4}}\right) + s^2\frac{C_oC_T}{g_{m4}g_{m1}}} \tag{8}$$

where the capacitive feedthrough term τ_f is assumed to have a negligible effect on the transfer function of interest. The small-signal model shown in Fig. 5(a) gives another method for obtaining the above results; because of the Miller effect and frequency-dependent amplifier gain, the circuit model displays effective inductance and conductance parameters on the V_X node. The Miller capacitance is amplified by loop gain, which is also frequency dependent; therefore, not only is this capacitance amplified, but a resulting conductance and inductance (due to the gyrator like structure) are, as well.

This circuit model can be used to compute the performance of the C^4 for $Q > 1$. The center frequency f_{center} is set by $\left(C_OC_T \ll C_2^2\right)$

$$f_{\text{center}} = \frac{1}{2\pi\tau} = \frac{\sqrt{g_{m4}g_{m1}}}{2\pi\sqrt{C_oC_T}} \tag{9}$$

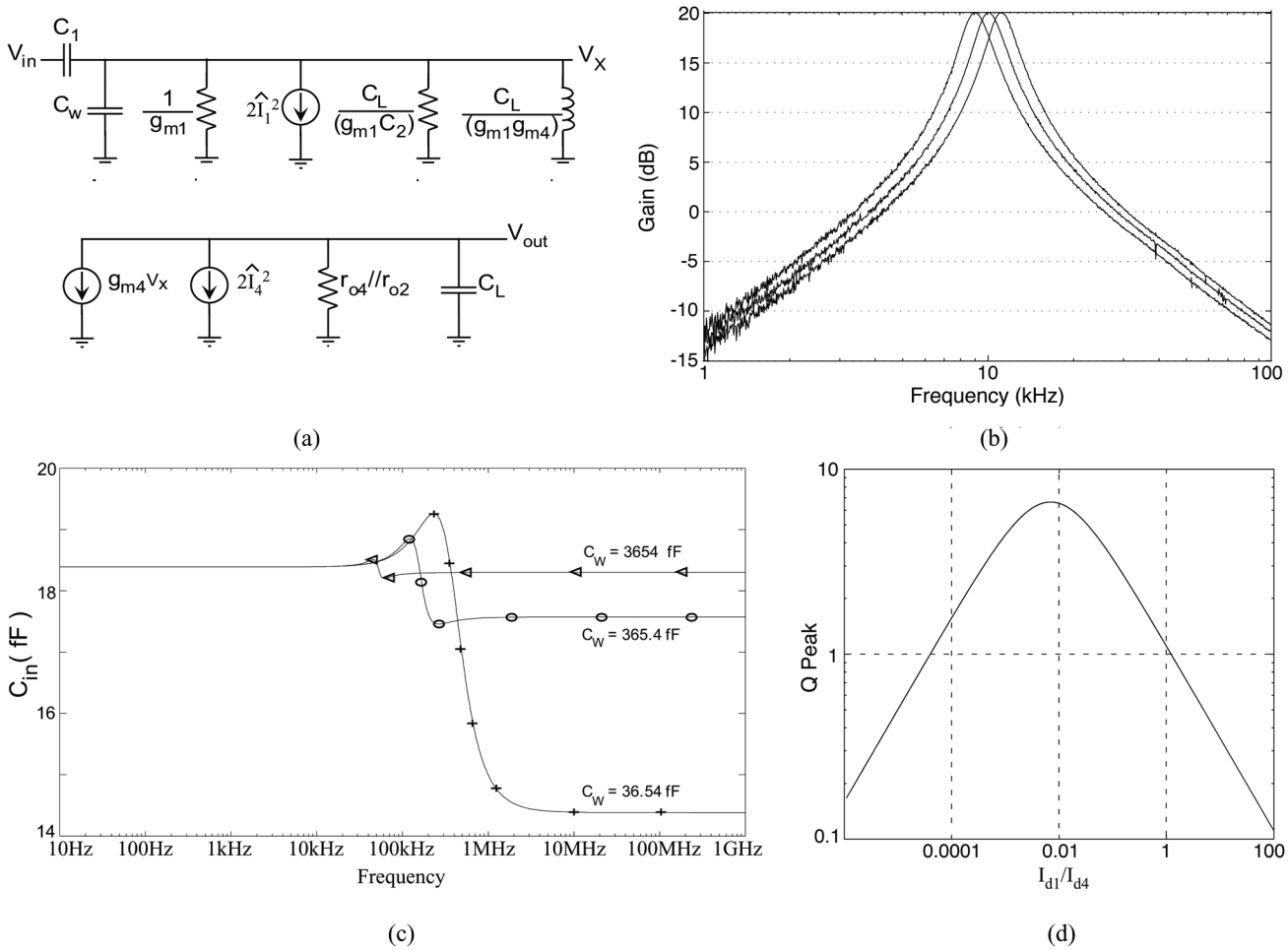

Fig. 5. Analysis and measurements of a C^4 biased with $Q > 0.5$. (a) Small-signal model of the C^4 for $Q > 0.5$. This model shows the effective inductance and conductance that depends on real circuit parameters. This model gives intuition of the filter operation, as well as easily enabling hand calculation for linear performance parameters for the high-Q case. (b) Measured frequency response of the C^4 tuned to 9, 10, and 11 kHz. This plot shows that the center frequencies can be fine-tuned by setting the desired bias current accurately using floating-gate transistors. (c) Input capacitance dependence on frequency. Simulation results showing that the input capacitance of the C^4 varies with frequency. (d) Quality factor, Q, versus bias current ratio. A maximum Q peak is defined for a given ratio of bias currents. As the current ratio changes from the maximum value, Q decreases.

the passband gain A_v is set by

$$A_v = -\frac{C_1}{C_2}\frac{1}{1+\frac{g_{m1}}{g_{m4}}\frac{C_o}{C_2}} \tag{10}$$

and the quality factor, Q, of the resonance is given by

$$Q = \frac{\sqrt{C_T C_O}}{C_2\sqrt{\frac{g_{m4}}{g_{m1}}} + C_O\sqrt{\frac{g_{m1}}{g_{m4}}}}. \tag{11}$$

Transistors M_1 and M_4 can operate in weak, moderate, or strong inversion depending on the desired frequency response. Fig. 5(b) shows the measured frequency response of second-order filter tuned at 9, 10, and 11 kHz. The plot shows that the center frequencies can be fine-tuned by setting the desired bias currents accurately using floating-gate transistors. As can be seen from the above equations, the corner frequency and the quality factor depend on the transconductances and, therefore, the dc bias currents. Thus, the filter element can be easily fine-tuned after fabrication to the desired corner frequencies and Qs by tuning g_{m1} and g_{m4} using floating-gate current sources.

Fig. 6(a) shows the measured response of a single C^4 and a cascade of two C^4s (with an isolation buffer) when programmed over several decades of frequency (100 Hz–10 MHz). SPICE simulation results match closely to the measured responses, as can be seen in Fig. 6(a). The measurements were limited to 1 MHz due the output buffers ($f_{-3\text{ dB}} \approx 10$ MHz). Figs. 5(b) and Fig. 6(a) show that the C^4 can be both programmed over a wide frequency range and fine tuned over a small frequency range.

For these filters, capacitor ratios set a maximum quality factor, $Q_{\max}$. Fig. 5(d) shows that Q changes with the ratio of I_4/I_1, or accordingly, g_{m4}/g_{m1}, which is consistent with (11). This plot illustrates that a maximum Q peak occurs for a certain value of I_4/I_1 (and thus g_{m4}/g_{m1}) and decreases as the ratio is either increased or decreased. $Q_{\max}$ is given by

$$Q_{\max} = \frac{1}{2}\sqrt{\frac{C_T}{C_2}} \text{ where } \frac{g_{m4}}{g_{m1}} = \frac{C_o}{C_2}. \tag{12}$$

We achieved an effective quality factor Q_{eff} of $Q_{\text{eff}} = 70$ at 1 MHz for a cascade of two C^4s. Increasing Q requires either increasing C_T or decreasing C_2; C_2 includes the gate-to-drain

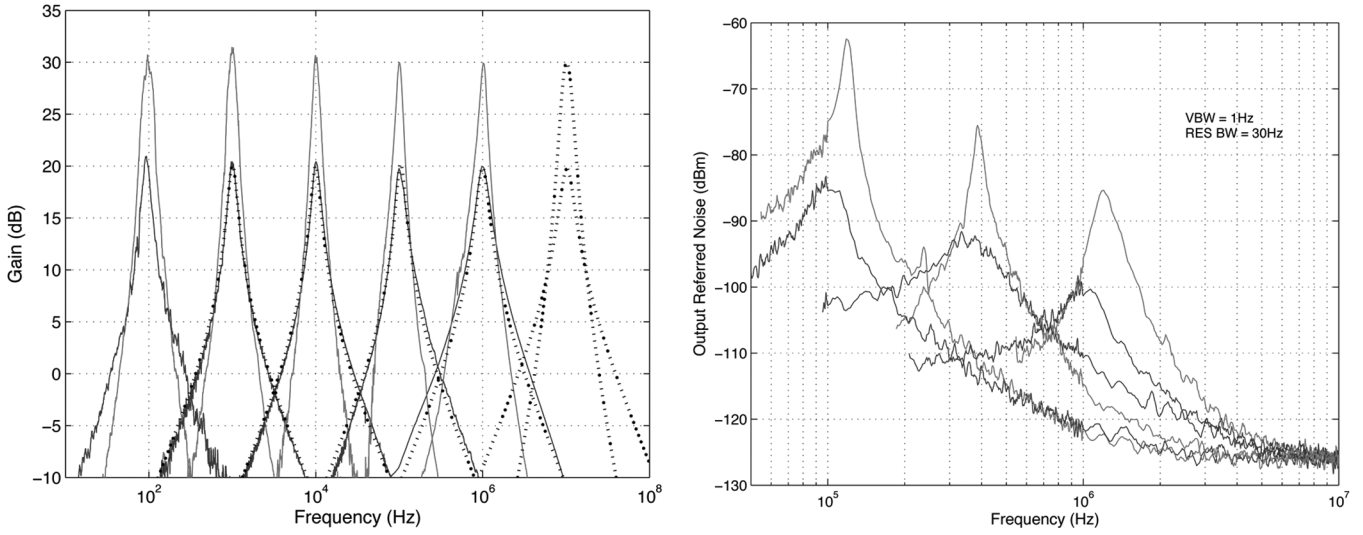

Fig. 6. Measurement of the performance of C^4s. (a) Frequency response of the C^4 and a cascade of two C^4s showing that these filters can be programmed over a wide range of frequencies (100 Hz–10 MHz). We have programmed filters with corner frequencies below 1 Hz with moderate Q values. Dashed lines show the results of SPICE simulations, which match closely to the actual performance. (b) Output-referred noise of the C^4. This plot shows the measured output-referred noise spectrum of a C^4 and a cascade of two C^4s, which are both tuned to several different center frequencies.

capacitance (overlap capacitance) of M_4 and the effective capacitance from gate to source of the M_1 and M_D transistor combination. The resulting center frequency at $Q_{\max}$ is

$$f_{\text{center}} = \frac{g_{m4}}{4\pi C_o Q_{\max}} = \frac{g_{m1}}{4\pi C_2 Q_{\max}} \tag{13}$$

and the gain at the center frequency for the $Q_{\max}$ case is $A_v = -C_1/2C_2$.

B. Noise in C^4s for $Q > 0.5$

Next, we address the noise generated by the filter. The generated frequency-dependent noise model for the C^4 amplifier is computed as

$$\hat{V}_{\text{out}}(s) = \frac{\sqrt{2}\hat{I}_4(s) g_{m1}(1 + s\frac{C_T}{g_{m1}}) + \sqrt{2}\hat{I}_1(s) g_{m4}(1 + s\tau_f)}{s^2 C_O C_T + s(C_L g_{m1} + g_{m4} C_2) + g_{m1} g_{m4}} \tag{14}$$

where $\hat{I}_1(f)$ and $\hat{I}_4(f)$ are the thermal-noise quantities contributed by M_1 and M_4, respectively. These thermal-noise expressions are given by

$$\hat{I}_1(f) = 2qI_1\Delta f \text{ and } \hat{I}_4(f) = 2qI_4\Delta f \tag{15}$$

where Δf is the bandwidth of the filter and I_1 and I_4 are the bias currents. We can solve for the in-band noise by integrating over the bandwidth, or solve for the noise over the entire spectrum by integrating over all frequencies. In most cases, the in-band noise is by far the largest noise component. When integrating over the bandwidth, we center our integration around f_{center} and integrate over the bandwidth ($\Delta f = f_{\text{center}}/Q$). Solving for the total in-band noise, we get

$$\hat{V}_{\text{out}} = \int_f \frac{\sqrt{2}\hat{I}_4(f) C_T - j\sqrt{2}\hat{I}_1(f) g_{m4}\tau}{(g_{m1} C_L + g_{m4} C_2)} df \tag{16}$$

$$\hat{V}_{\text{out}} = \frac{\sqrt{qI_4 \frac{C_T C_2 g_{m4} + C_O g_{m1})}{C_O}} - j\sqrt{qI_1\left(\frac{C_2}{g_{m1}} + \frac{C_O}{g_{m4}}\right) g_{m4}}}{(g_{m1} C_L + g_{m4} C_2)} \tag{17}$$

where we defined the effective noise bandwidth as $1/(4\tau Q)$ [16]. Noise at low frequencies (not in band) is nearly constant independent of frequency as determined by the thermal-noise level, and the total noise in this region is the same as for the wide-band stage, which is important if adding together the results of multiple elements, as in a programmable filter [7].

We simplify the noise modeling when biased in the $Q_{\max}$ case, which helps in providing intuition about the noise behavior over the range of potential bias currents. For the $Q_{\max}$ case, the noise expression becomes

$$\hat{V}_{\text{out}} = \sqrt{\frac{I_4}{g_{m4}} \frac{qC_T}{2C_2 C_O}} + j\sqrt{\frac{qV_L}{2C_2}} \tag{18}$$

where $V_L = I_1/g_{m1}$. Since $C_O > C_2$ and the linear range defined by the high-gain term is not significantly larger than V_L, the second term (the j term) typically sets most of the noise for the filter. If we are not at the $Q_{\max}$ case, we can have the case on either side of the maximum, defined as Case I in which $g_{m4}C_2 > C_O g_{m1}$ and Case II in which $g_{m4}C_2 < C_O g_{m1}$. For Case I, the noise power is within a factor of 2 of the $Q_{\max}$ case and can generally be approximated as roughly equal to the $Q_{\max}$ case (in the limit when g_{m4} is large). For Case II, we can approximate the noise power as

$$\hat{V}_{\text{out}} = \hat{V}_{\text{out}}(Q_{\max}) \sqrt{\frac{g_{m4} C_2}{g_{m1} C_O}} \tag{19}$$

where $\hat{V}_{\text{out}}(Q_{\max})$ is the noise level for g_{m1} at the $Q_{\max}$ level.

Fig. 6(b) shows the output-referred noise measurement of a single C^4 and a cascade of two C^4s for various center frequencies. The noise spectrum is similar in nature to the frequency response of the filter, as is expected from the noise modeling experiments. Fig. 6(b) also shows that the overall noise spectrum decreases as the programmed center frequency is increased, consistent with the total noise over the bandwidth being roughly independent of the center frequency. Further, we see the constant noise level expected at low frequencies, which indicates that $1/f$ noise was not significant over the measured bandwidth. The measured output spot-noise at 1 MHz for the C^4 was found to be -100 dBm (using $\mathrm{VBW} = 1$ Hz).

C. Linearity and Distortion in C^4s

Next, we briefly consider the linearity and associated distortion terms for the C^4 filter. The complete analysis requires a detailed study of the forced nonlinear dynamics of the transistor circuit, and is beyond the scope of this paper. However, we will explain some of the qualitative features here.

Using the analysis from the wide-band case and focusing on subthreshold operation, the output-referred linear range from input to output is given by

$$\frac{C_T}{\kappa C_2} U_T = \frac{4Q_{\max}^2 U_T}{\kappa} \tag{20}$$

and the linear range from the output to the input is V_L, which is the effective I_1/g_{m1} seen by transistor M_4 including the degeneration device (M_D). In general, the smaller of these two linear ranges sets the linear range of interest, since both are output referred. For the differential C^4 approach, the third-order harmonic distortion at an input amplitude set at this linear range is better than -40 dB for subthreshold biases; lower distortion is achieved by scaling the input amplitude appropriately, assuming the third-order power law for third-order harmonic distortion.

One can perform a detailed perturbation theory analysis on the resulting nonlinear equations describing a C^4 circuit to describe the resulting nonlinear effects, including harmonic distortion and two-tone analysis; although a detailed analysis is beyond the scope of this paper, we will briefly describe some of the key results here. We addressed the nonlinear effects for the low Q $(Q < 0.5)$ case in the previous section; in this section we will consider the nonlinearities for the moderate Q $(Q > 0.5)$ case. When looking at a differential C^4 structure, composed of two parallel C^4 structures mentioned earlier, we can describe the nonlinear behavior by the following pair of differential equations:

$$\begin{aligned} C_T \frac{dV_x}{dt} &= C_1 \frac{dV_{\text{in}}}{dt} + C_2 \frac{dV_{\text{out}}}{dt} \\ &\quad + 2I_4 \sinh\left(\frac{\Delta V_x - \kappa \Delta V_{\text{out}}+}{2U_T}\right) \\ C_o \frac{dV_{\text{out}}}{dt} &= C_2 \frac{dV_x}{dt} - 2I_1 \sinh\left(\frac{\kappa \Delta V_x}{2U_T}\right) \end{aligned} \tag{21}$$

where ΔV_x, ΔV_{in} and ΔV_{out} are the differential voltages between the V_x, V_{in}, and V_{out} terminals, respectively. Identifying the linear range terms for this circuit are critical for a nonlinear analysis of this bandpass filter, as well as most G_m–C filters (i.e., second-order sections), since it is the normalization parameter computed for the given topology. Once these two parameters are determined, then harmonic distortion, two-tone responses, and other nonlinear tests are simply a one parameter function of desired Q. The input amplitude around the linear range would still be considered a small signal for the resulting amplifier; therefore, the distortion amplitude increases as a cubic power with increasing amplitude. Nonlinear distortion for this bandpass amplifier is computed using a two-tone test, with the two input sinusoidal signals symmetrically around the center frequency. This measurement is directly related to the 1-dB compression point measurement, since the same nonlinearities creating harmonic components equally create fundamental components that decrease the gain of the fundamental amplitude; the 1-dB compression point is roughly equal to where the two-tone harmonic distortion is -26 dB. For an input signal at the linear range defined for amplifier with M_4, at the maximum Q $(Q_{\max})$ biasing case, which is an average case condition, the resulting two-tone harmonic distortion for large input amplitudes follows the expression

$$3^{rd}\text{Harmonic} = 0.0078\,(Q_{\max} c + cj - 1) \tag{22}$$

where c is the relative follower linearity (M_1 transistor device) from U_T/κ $(c < 1)$. This model starts for an input signal of the size of the input linear range with a two-tone distortion around -42 dB for low $Q_{\max}$, reaches a minimum distortion level of -42 dB $+ 20\log_{10}(c)$ for a $Q_{\max} \approx (1/c)$, and increases as -42 dB $+ 20\log_{10}(cQ_{\max})$ for larger values of $Q_{\max}$. Certain linear range cases are optimal for this perturbation analysis for particular $Q_{\max}$; in general, the tradeoffs are a bit more complex, and beyond the discussion of this paper. These expressions would yield the resulting IIP3 point as a $11.2/\mathrm{sqrt}(Q_{\max} c + cj - 1)$ factor times the input linear range, and yield the 1-dB compression point as a $2.6/\mathrm{sqrt}(Q_{\max} c + cj - 1)$ factor times the input linear range. For example, for $Q_{\max} = 4$, $c = 1$, one would expect an 1-dB compression point is approximately the linear range, and the IIP3 point eight times the linear range; for a typical linear input range (defined by capacitor ratios) for subthreshold operation of 0.2 V, the resulting 1-dB compression point is at 0.2 V, and IIP3 point at 1.6 V. As another example, for $Q_{\max} = 4$, $c = 0.1$, one would expect an 1-dB compression point 3.33 times the linear range, and the IIP3 point 15 times the linear range; for a typical linear input range (defined by capacitor ratios) for subthreshold operation of 0.5 V, the resulting 1-dB compression point is at 1.5 V, and IIP3 point at 7.5 V. Distortion at the input linear range amplitude is significantly lower than other traditional G_m–C topologies due to no nonlinearities added in the initial input voltage to current conversion; in particular, the input device is a capacitor versus a transconductance amplifier.

Fig. 7(a) shows the measurement to compute the 1-dB compression point for a single C^4 and a cascade of two C^4s for two different quality factors. As expected, the linearity degrades as Q increases. The linearity for the filters (a C^4 with $Q = 2.5$ and a cascaded of two C^4s with $Q_{\text{eff}} = 5.2$) at 1 MHz were -24 dBm (83 mV_{pp}) and -42 dBm (11.5 mV_{pp}), respectively.

Fig. 7(b) shows the measurement to compute the 1-dB compression point for different bias values of M_D for a C^4 with low Q.

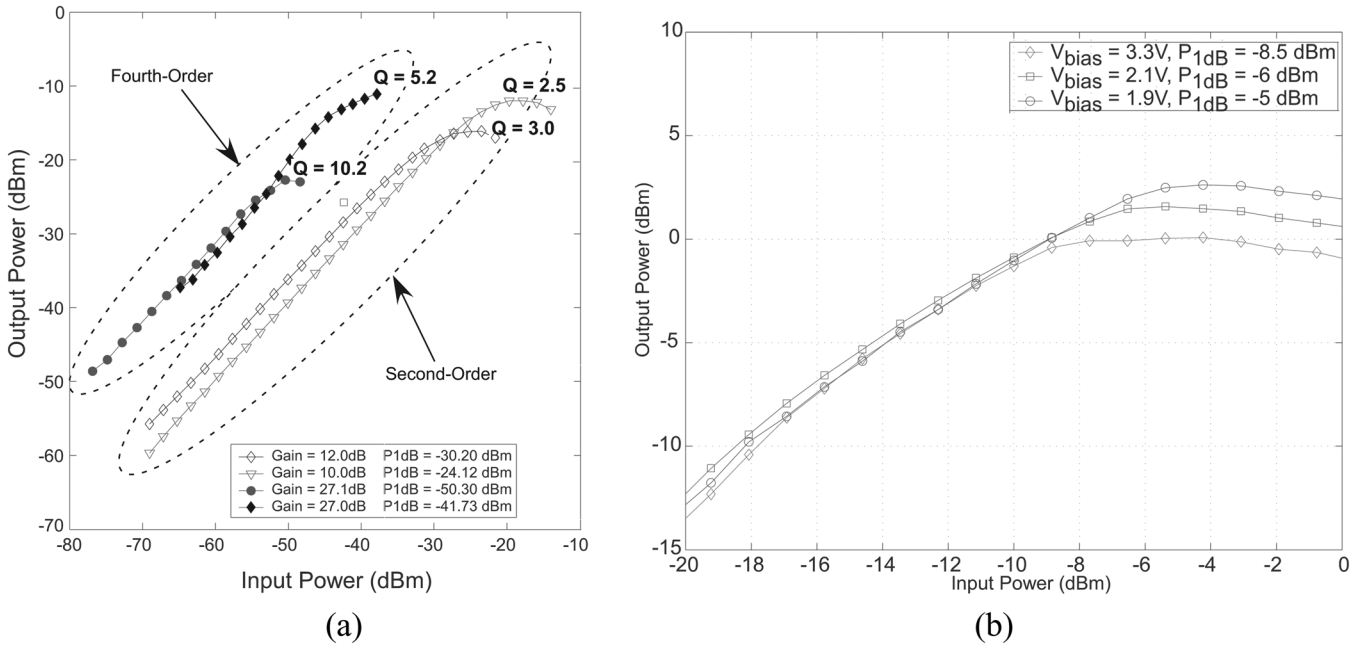

Fig. 7. Linearity of the C^4. (a) 1-dB compression point for different values of Q for a C^4 and a cascade of two C^4s. The 1-dB compression point was measured using a 100-kHz tone at the programmed center frequency of the filter. (b) Effect of the short-channel device, M_D. This increase in linearity is due to the source-degeneration effect achieved by properly biasing M_D.

It can be clearly seen that the linearity increases from -8.5 dBm to -5 dBm as the gate voltage of M_D is decreased from 3.3 V to 1.9 V. This increase in linearity comes at the cost of lowering of the low-frequency corner due to the source-degeneration effect. Thus, the current I_2 needs to be tuned to a higher value than before to achieve the same lower time constant.

D. SNR and Power Dissipation in C^4s

Finally, we calculate the SNR and power dissipation for this filter. Assuming the second term of (18) sets the noise for the amplifier $\left(=\sqrt{qV_L/C_2}\right)$, and that V_L sets the output linear range, the SNR is

$$\mathrm{SNR} = \frac{C_2 V_L}{q}. \tag{23}$$

The SNR can be improved by designing for a larger $Q_{\max}$ and increasing the resulting g_{m1}, typically consuming more power as a result.

The resulting power dissipation P for the C^4 is

$$P = 4\pi f_{\mathrm{center}} V_{dd} Q_{\max} \left(q \cdot \mathrm{SNR} + C_O \frac{I_4}{g_{m4}} \right). \tag{24}$$

P does not include additional biasing transistors needed for a particular implementation, but their effect on power dissipation can be minimized by design. Typically, the C_O term will be less than the SNR term, because M_4 is usually biased with currents near or below threshold and because C_O is less than an order of magnitude larger than C_2; therefore, the power dissipation can be estimated as

$$P = 8\pi q f_{\mathrm{center}} V_{dd} Q_{\max} \mathrm{SNR}. \tag{25}$$

Table I shows the resulting SNR and power dissipation for a few representative designs of the C^4.

TABLE I
SNR AND POWER DISSIPATION FOR A FEW REPRESENTATIVE C^4 AMPLIFIER DESIGNS. $V_{dd} = 3.3$ V, AND $Q = 4$

f_{center}	C_2	V_L	SNR	Power
20kHz	32fF	0.5V	50dB	0.11μW
20kHZ	160fF	1V	60dB	1.1μW
20MHz	64fF	0.25V	50dB	106μW
20MHZ	160fF	1V	60dB	1.06mW

Algorithmic Design of C^4 Bandpass Filters

In this subsection, we describe how to algorithmically design a C^4 filter from a given set of specifications including linear range (V_{lin}), quality factor (Q), noise level $(\hat{V}_n$ which is directly computed from SNR), input-signal level $(V_{\mathrm{in,max}})$, and center frequency (f_{center}). When designing a C^4 to meet given specifications, one major consideration is whether or not at $Q = Q_{\max}$ the resulting ratio of C_T/C_2 sets the linear range from input to output $(U_T C_T/(\kappa C_2))$ to be larger than the specifications. If so, we start with the $Q_{\max}$ design approach; otherwise, we take an alternate approach. Further, if the resulting desired SNR is an issue, $Q_{\max}$ can be designed to be quadratically higher by the desired decrease in the noise factor.

To design the C^4 amplifier at the $Q = Q_{\max}$ case, the following design equations should be used

$$\begin{aligned} C_2 &= \frac{qV_L}{\hat{V}_n^2} \\ C_T &= 4C_2 Q_{\max}^2 \\ C_1 &= 2C_2 \frac{V_{\mathrm{in,max}}}{V_L} \\ g_{m1} &= 4\pi f_{\mathrm{center}} C_2 Q_{\max} \\ \frac{g_{m4}}{g_{m1}} &= \frac{C_o}{C_2}. \end{aligned} \tag{26}$$

V_L sets the output linear range. As a result, we have one free parameter available at the last step that allows us to optimize the power dissipation. Even if $C_O = C_2$, which is the minimum value for C_O, there is a minimum required amount of power, and therefore C_O weakly effects the filter operation.

For the alternate design procedure (operating in the Case I noise analysis region), the following design equations can be used:

$$
\begin{aligned}
C_2 &= \frac{qV_L}{2\hat{V}_n^2} \text{ where } V_L = \frac{I_1}{g_{m1}} \\
C_T &= C_2 \frac{V_{lin}}{\left(\frac{I_4}{g_{m4}}\right)} \\
C_1 &= 2C_T \frac{\left(\frac{I_4}{g_{m4}}\right)}{V_{\text{in,max}}} \\
g_{m1} &= 2\pi f_{\text{center}} C_2 Q \\
g_{m4} &= 2\pi C_O f_{\text{center}} \frac{C_T}{QC_2} \\
P &= 2\pi f_{\text{center}} C_2 V_{dd} \left[1 + \frac{C_T C_O}{C_2^2 Q^2}\left(\frac{I_4}{g_{m4}}\right)\right]. \qquad (27)
\end{aligned}
$$

Again, we have a similar tradeoff for C_O, where C_O can be chosen to have a wide range for desired circuit performance, even when optimized for power.

These design approaches can be easily implemented by computer programs such as MATLAB, Excel, etc. Also, the design approach can be modified by using OTAs instead of the simple two-transistor high-gain or follower amplifiers, and achieve similar results.

IV. High-Order Filter Implementation

The C^4 can be used as a basic filter element in cascade to implement high-order filters, since the C^4s are simple and compact second-order bandpass filters. Fig. 1 shows the block diagram of a tenth-order filter using these core C^4 filters. These high-order filters can be tuned to any desired transfer function after fabrication, including Butterworth and Chebyshev responses. The coefficients can be set accurately by programming the floating-gate currents.

To illustrate the ability of using the C^4 as a basic bandpass-filter building block, we built an array of 16 tenth-order filters. Fig. 8(a) shows the frequency response of tuning a single sixth- and tenth-order filter from this array to have a center frequency of 1 MHz. Since these filters are easily tuned by programming floating-gate transistors, the filter can be programmed to have a wide range of center frequencies (10 Hz–10 MHz) and any desired bandwidth.

Since the C^4 is a very-compact filter element, a large number of C^4s can be placed onto a single die, and thus high-order filters can be achieved without consuming large amounts of area. Fig. 9 shows a die photograph of the array of 16 tenth-order filters. This 0.5-μm-process chip has the dimensions of 1.5 mm $\times$ 1.5 mm and includes all of the required floating-gate programming circuitry and also buffers between each C^4.

V. Conclusion

In this paper, we presented a capacitively coupled current conveyor that serves as a very-compact and power-efficient bandpass filter and can cover a wide range of frequencies. Additionally, the bandpass filter can be used as a basic bandpass-filter building block for creating high-order filters. This filter has been successfully built in several processes, and

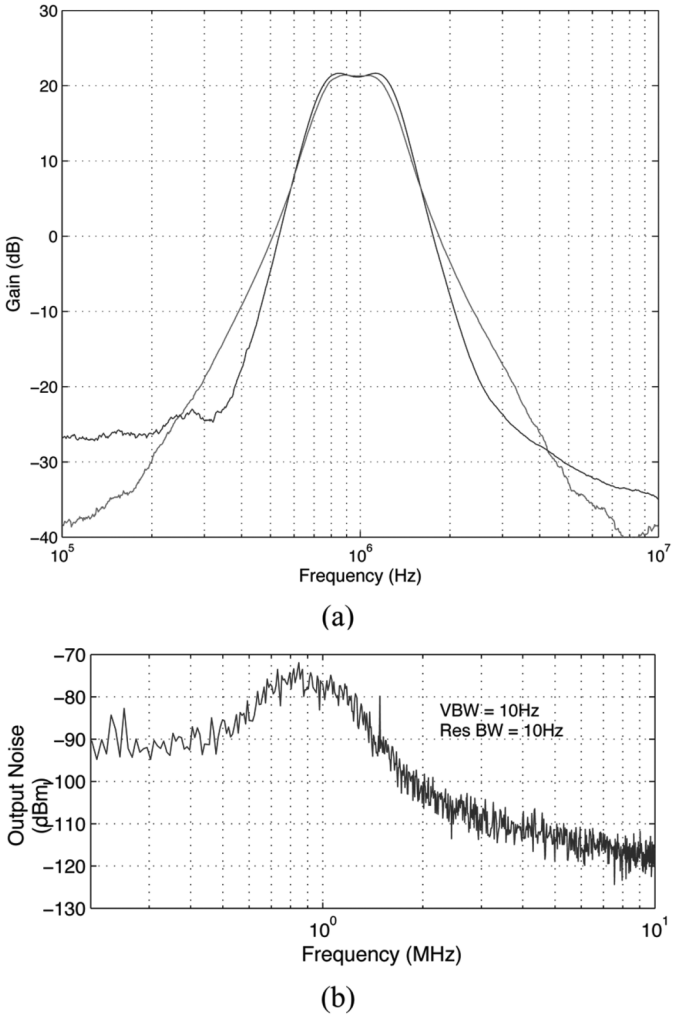

Fig. 8. High-order filters constructed from C^4s. (a) Frequency response of sixth- and tenth-order filters. (b) Output-referred noise spectrum for the tenth-order filter.

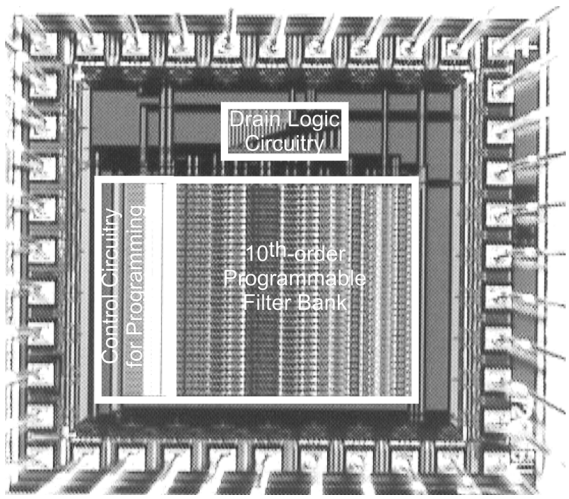

Fig. 9. Die photograph of an array of 16 tenth-order filters comprised of C^4s. This integrated circuit consumes an area of only 1.5 mm $\times$ 1.5 mm.

TABLE II
SUMMARY OF PERFORMANCE

Parameter	2nd-order	4th-order	10th-order
Frequency Range	10Hz-10MHz	10Hz-10MHz	N/A
Q range	< 9	< 72	N/A
Output Noise (dBm @ 1MHz) (VBW = 1Hz)	-100dBm	-84dBm	-78dBm (VBW = 10Hz)
Total Power (with buffers)	0.1nW-15μW	0.25nW-15μW	20μW @ 1MHz
SNR @ 1MHz	86dB	72dB	55dB
Area	2.1e3μm^2	4.8e3μm^2	13.2e3μm^2
Programming % error	$< \pm 0.2\%$	$< \pm 0.2\%$	$< \pm 0.2\%$

Table II summarizes the performance of the C^4 in a 0.5-μm process available through MOSIS as well as cascades of two C^4s (fourth-order filter) and five C^4s (tenth-order filter).

The use of floating-gate transistors in the design of the C^4 helps to ease the difficulties of effectively utilizing G_m–C filters, especially in terms of tuning, accuracy, and the problems of offsets. Floating-gate transistors are used as current sources to set the time constants of the bandpass filter, and since the floating-gate transistor currents can be programmed very precisely, the response of the C^4 can also be set very precisely using a single calibration step [15]. Additionally, the use of floating-gate transistors provides the ablity to program the circuit to a desired performance after fabrication, which is useful in cases in which specifications for the bandpass filter may change after fabrication.

The C^4 provides a useful bandpass filtering element but does not require large amounts of real estate. Even the addition of floating-gate transistors, which provides for a high-degree of functionality and precision, does not significantly add the the required real estate. As a consequence of the small amount of real estate, and also because of the low-power nature of this bandpass filter, the C^4 is ideal for array signal-processing applications including speech recognition [12], noise suppression [18], and even cochlear modeling [19].

REFERENCES

[1] D. A. Johns and K. Martin, Eds., *Analog Integrated Circuit Design*. New York: Wiley, 1997.

[2] P. Kallam, E. Sanchez-Sinencio, and A. Karsilayan, "An enhanced adaptive Q-tuning scheme for a 100-MHz fully symmetric ota-based bandpass filter," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 585–593, Apr. 2003.

[3] T. Pham and P. Allen, "A highly accurate step-response-based successive-approximation frequency tuning scheme for high-Q continuous-time bandpass filters," *IEEE Trans. Circuits Syst. I, Analog Digit. Signal Process.*, vol. 50, no. 5, pp. 221–227, May 2003.

[4] C. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 63–70, Jan. 2003.

[5] G. Serrano, P. D. Smith, H. J. Lo, R. Chawla, T. S. Hall, C. M. Twigg, and P. Hasler, "Automatic rapid programming of large arrays of floating-gate elements," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, BC, Canada, May 2004, vol. 1, pp. 1373–1376.

[6] P. Hasler, B. A. Minch, and C. Diorio, "An autozeroing floating-gate amplifier," *IEEE Trans. Circuits Syst II, Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 74–82, Jan. 2001.

[7] P. Hasler, M. Kucic, and B. A. Minch, "A transistor-only circuit model of the autozeroing floating-gate amplifier," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Las Cruces, Aug. 1999, pp. 157–160.

[8] P. D. Smith, D. W. Graham, R. Chawla, and P. Hasler, "A five-transistor bandpass filter element," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, BC, Canada, May 2004, vol. 1, pp. I-861–I-864.

[9] M. Kucic, A. Low, P. Hasler, and J. Neff, "A programmable continuous-time floating-gate fourier processor," *IEEE Trans. Circuits Syst II, Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 90–99, 2001.

[10] P. Hasler, B. A. Minch, C. Diorio, and C. A. Mead, "An autozeroing floating-gate amplifier," *IEEE Trans. Circuits Syst II, Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 74–82, 2001.

[11] R. Chawla, G. Serrano, D. Allen, A. Periera, and P. Hasler, "Fully differential floating-gate programmable OTAs with novel common-mode feedback," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, BC, Canada, May 2004, vol. 1, pp. 817–820.

[12] P. Smith, M. Kucic, R. Ellis, P. Hasler, and D. V. Anderson, "Mel-frequency cepstrum encoding in analog floating-gate circuitry," in *Proc. IEEE Int. Symp. Circuits Syst.*, Phoenix, AZ, May 2002, vol. IV, pp. 671–674.

[13] P. Hasler, B. A. Minch, and C. Diorio, "Adaptive circuits using pFET floating-gate devices," in *Proc. 20th Anniversary Conf. Adv. Res. VLSI*, Atlanta, GA, Mar. 1999, pp. 215–229.

[14] P. Hasler and J. Dugger, "Correlation learning rule in floating-gate pFET synapses," *IEEE Trans. Circuits Syst II, Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 65–73, Jan. 2001.

[15] D. W. Graham, P. D. Smith, R. Chawla, and P. Hasler, "A programmable bandpass array using floating-gate elements," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, BC, Canada, May 2004, vol. 1, pp. I-97–I-100.

[16] R. Sarpeshkar, R. F. Lyon, and C. Mead, "A low-power wide-linear-range transconductance amplifier," *Anal. Integr. Circuits Signal Process.*, vol. 13, no. 1–2, pp. 123–151, 1997.

[17] T. Massengill, D. Wilson, P. Hasler, and D. W. Graham, "Empirical comparison of analog and digital auditory preprocessing for automatic speech recognition," in *Proc. IEEE Int. Symp. Circuits Syst.*, Scottsdale, AZ, May 2002, vol. 5, pp. V-77–V-80.

[18] R. Ellis, H. Yoo, D. W. Graham, P. Hasler, and D. V. Anderson, "A continuous-time speech enhancement front-end for microphone inputs," in *Proc. IEEE Int. Symp. Circuits Syst.*, Scottsdale, AZ, May 2002, vol. 2, pp. II-728–II-731.

[19] D. W. Graham and P. Hasler, "Capacitively-coupled current conveyer second-order sections for continuous-time bandpass filtering and cochlea modeling," in *Proc. IEEE Int. Symp. Circuits Syst.*, Scottsdale, AZ, May 2002, vol. 5, pp. V-485–V-488.

David W. Graham (S'00–M'07) received the B.A. degree in natural science from Covenant College, Lookout Mountain, TN, in 2001, and the B.S. degree in electrical engineering, and the M.S. and Ph.D. degrees in electrical and computer engineering all from Georgia Institute of Technology (Georgia Tech), Atlanta, in 2001, 2003, and 2006, respectively.

He is an Assistant Professor in the Lane Department of Computer Science and Electrical Engineering, West Virginia University, Morgantown. His research interests are in developing biologically inspired electronics, cooperative analog and digital signal-processing systems, and programmable analog devices.