Capacitor Circuits

Switched Capacitor Circuits

- Clear out charge with transistors
- Discrete-Time Circuits

Floating-Gate Circuits

- “Program” floating-gate charge

More advanced: SET, etc.

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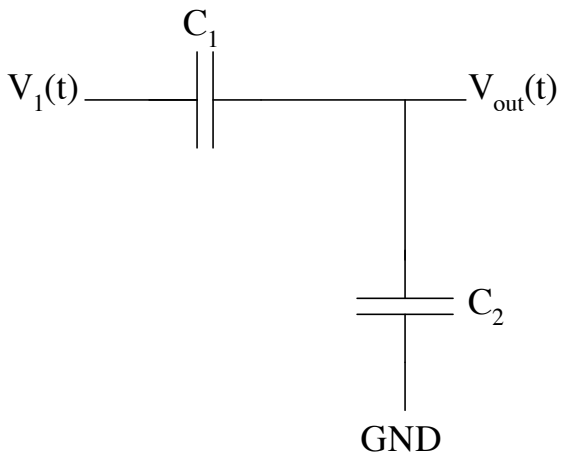
More advanced: SET, etc.

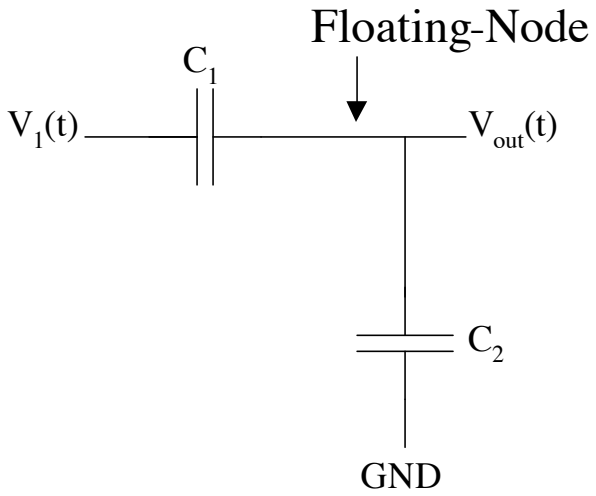
We will start by looking at a capacitive voltage divider circuit

Capacitor Circuits



- Capacitive Voltage Divider

Capacitor Circuits



- Capacitive Voltage Divider
- How to analyze this circuit?

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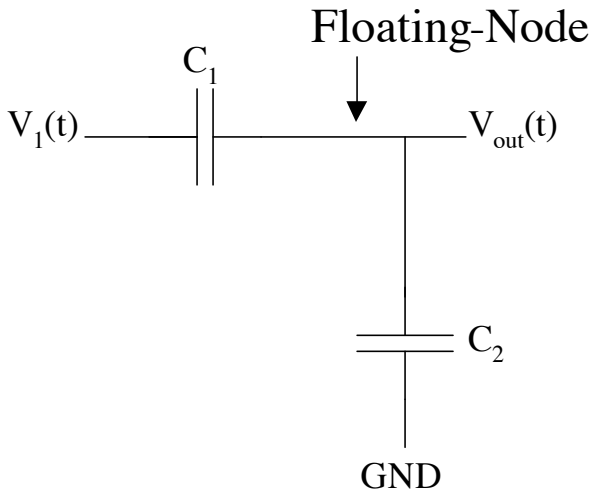

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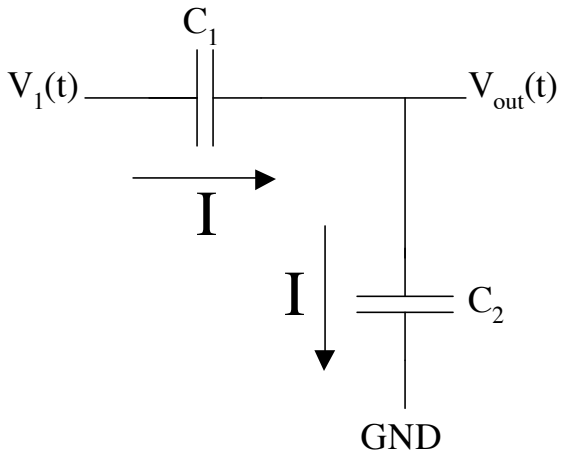

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Balancing Current

Current is not actually moving through the capacitors

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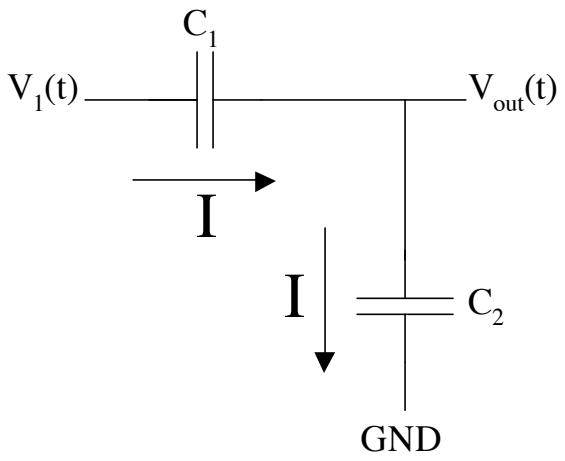

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$$C_1 \left(\frac{dV_1(t)}{dt} - \frac{dV_{out}(t)}{dt} \right) = C_2 \frac{dV_{out}(t)}{dt}$$

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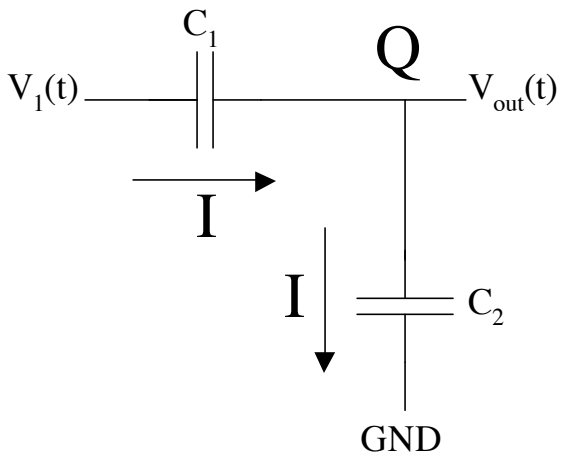

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$$Q + C_1 V_1(t) = (C_2 + C_1) V_{out}(t)$$

where Q is the constant of integration,
which equals the charge on the floating-node

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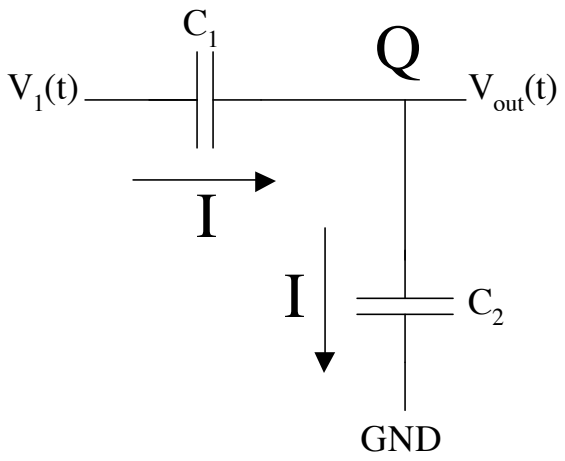

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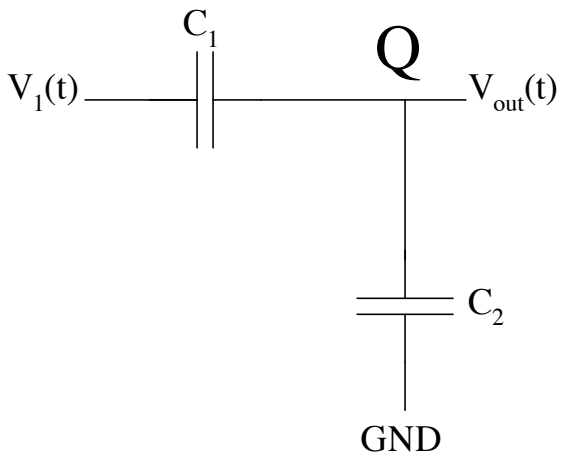

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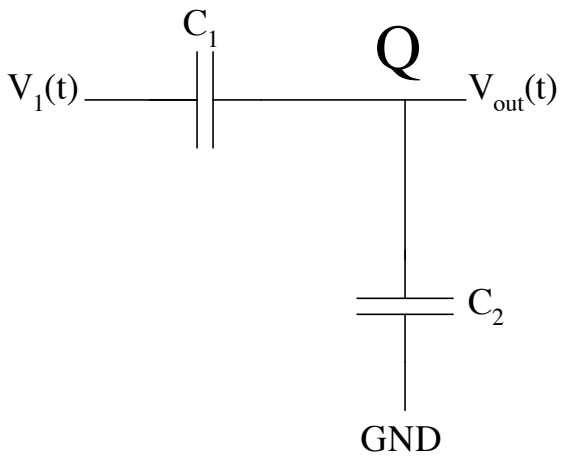

Balancing Charge

Total charge must be distributed on capacitor plates

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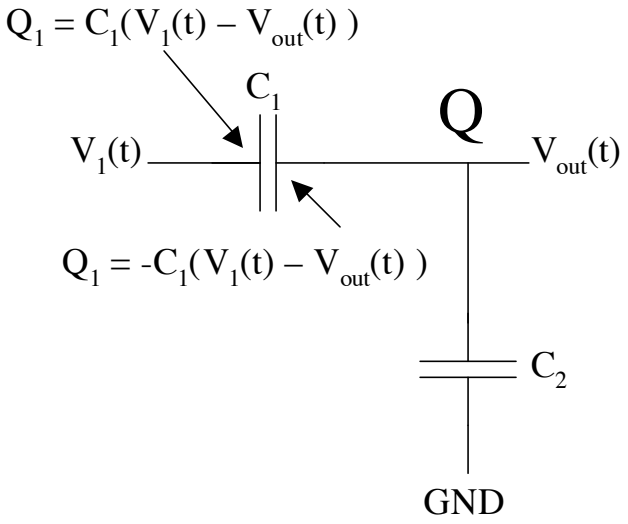

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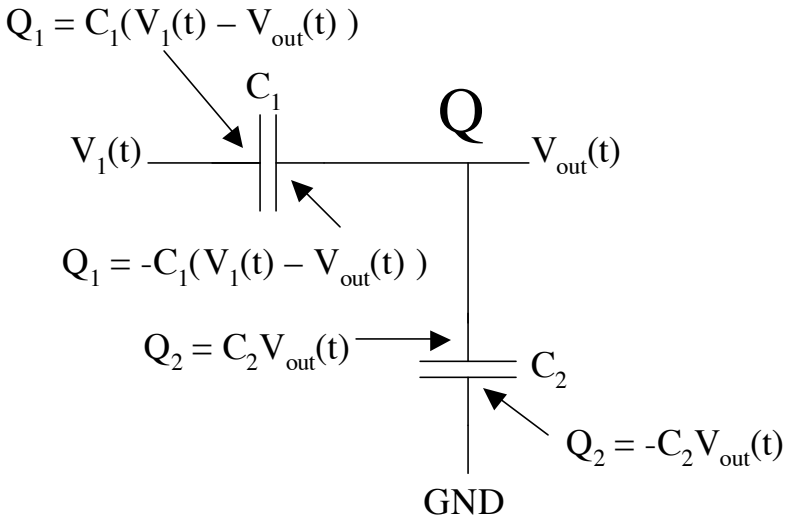

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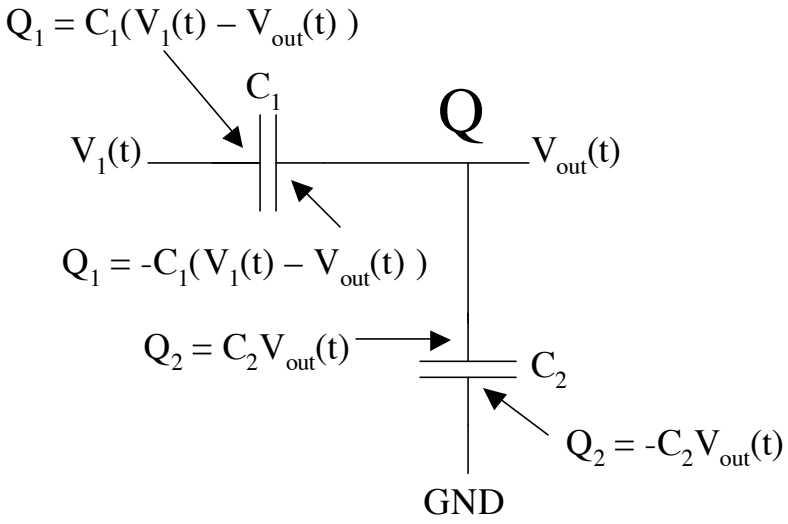

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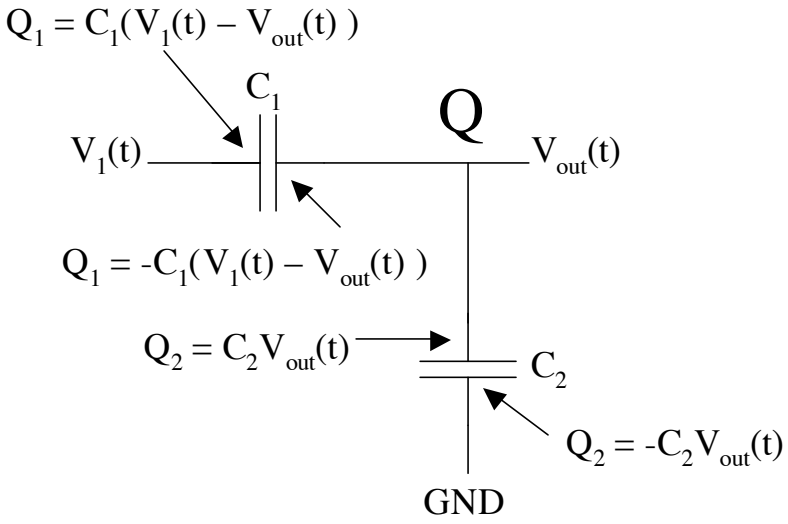

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Capacitor Circuits

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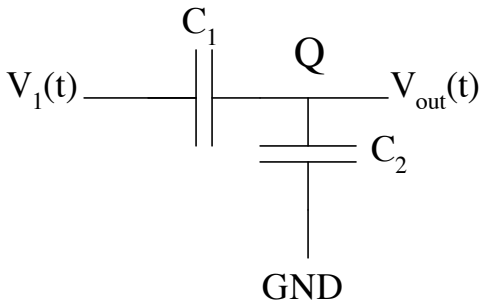

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Capacitor Circuits

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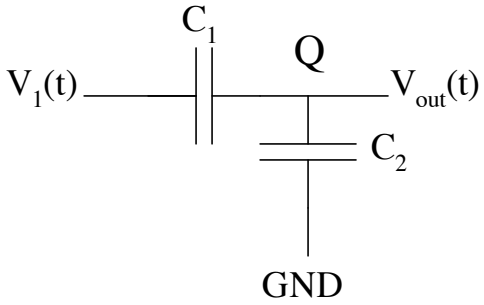
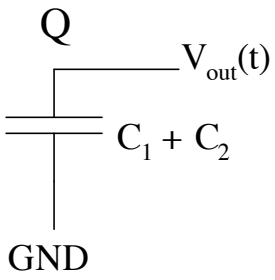


$$V_{out}(t) = \frac{C_1}{C_2 + C_1} V_1(t) + \frac{Q}{C_2 + C_1}$$

If $V_1(t) = 0$, we get

$$V_{out}(t) = \frac{Q}{C_2 + C_1}$$

We would derive this result directly if we started with the problem with a known charge Q



Capacitor Circuits

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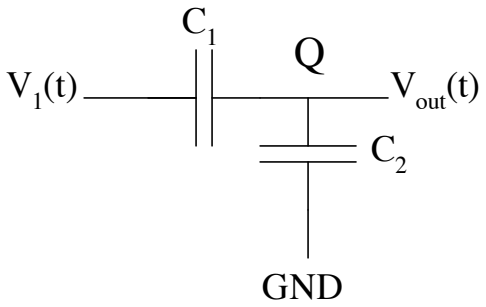
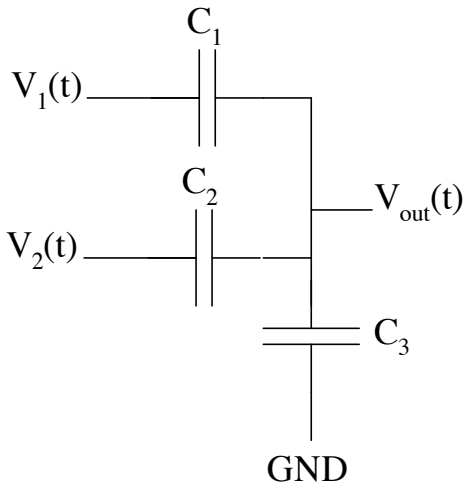


$$V_{out}(t) = \frac{C_1}{C_2 + C_1} V_1(t) + \frac{Q}{C_2 + C_1}$$

Multiple Input Capacitive Voltage Divider



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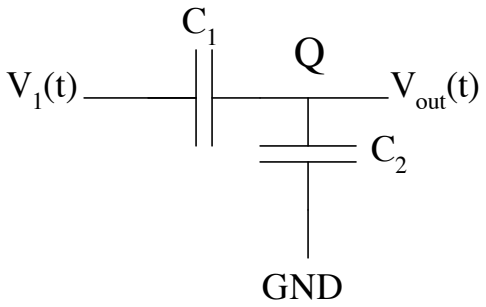

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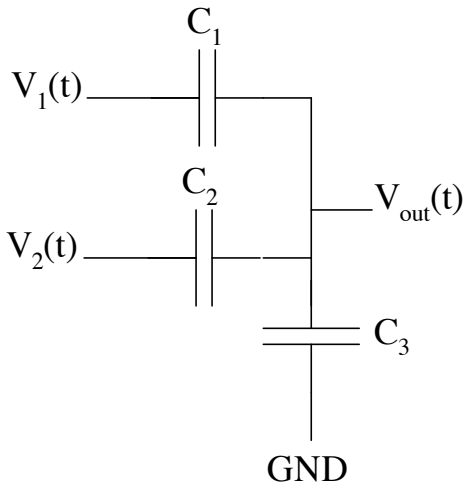

Balancing Current

$$(C_1 + C_2 + C_3)\frac{dV_{out}(t)}{dt} = C_1\frac{dV_1(t)}{dt} + C_2\frac{dV_2(t)}{dt}$$

Integrating with time, we get

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where Q is the constant of integration,
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Capacitor Circuits

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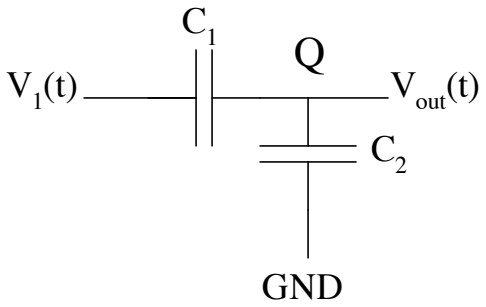

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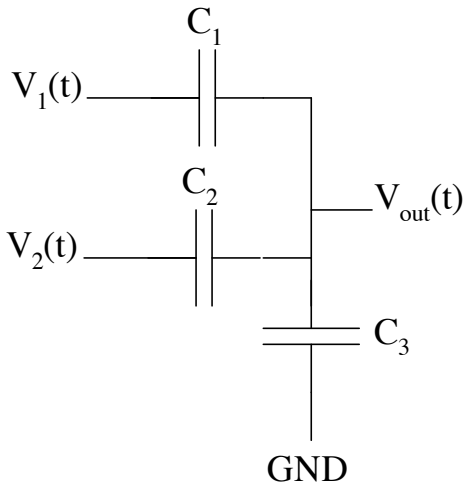

$$V_{out}(t) = \frac{C_1}{C_3 + C_2 + C_1} V_1(t) + \frac{C_2}{C_3 + C_2 + C_1} V_2(t) + \frac{Q}{C_3 + C_2 + C_1}$$

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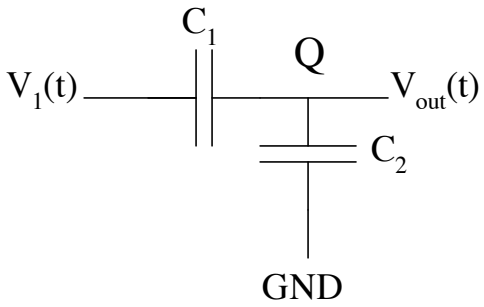

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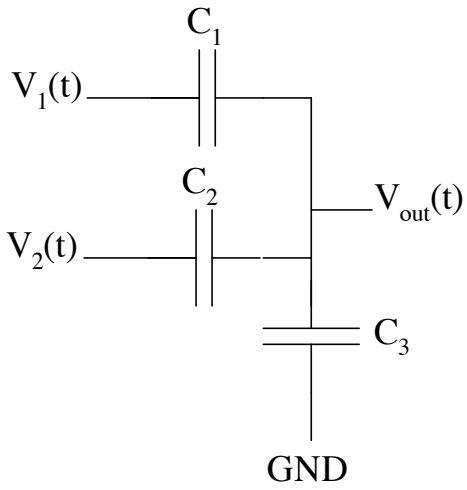

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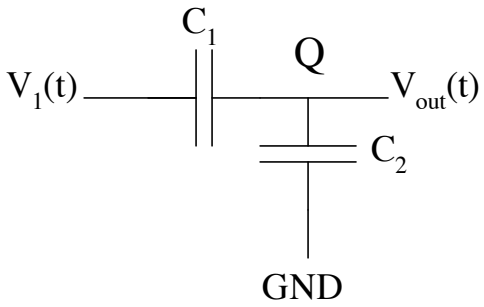

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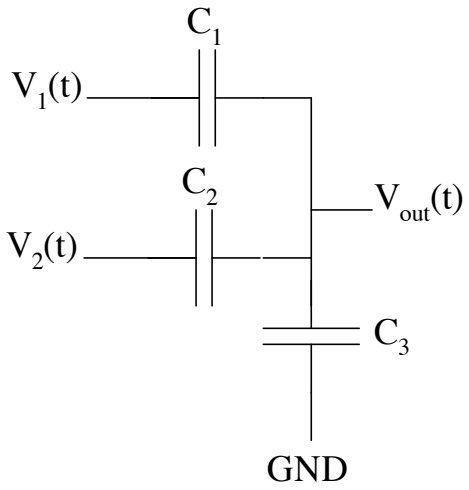

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We define C_T = total capacitance connected to the floating-node

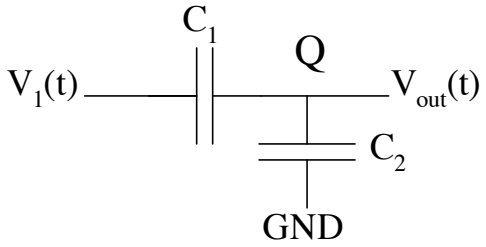
$C_T = C_1 + C_2$ (Capacitive Voltage Divider)

$C_1 + C_2 + C_3$ (Multiple Input Capacitive Voltage Divider)

[Minch, et. al, 1996]

Capacitor Circuits

Capacitive Voltage Divider



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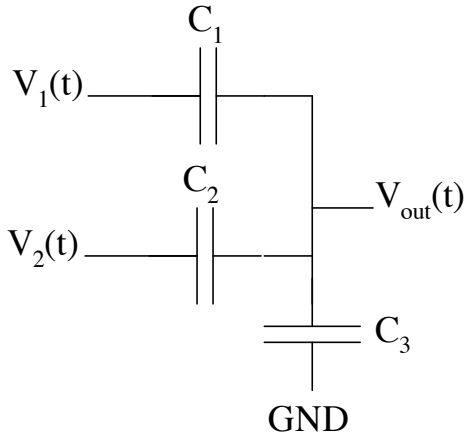
Multiple Input Voltage Divider



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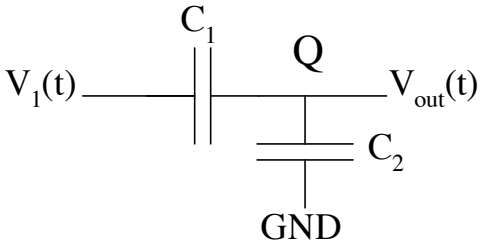

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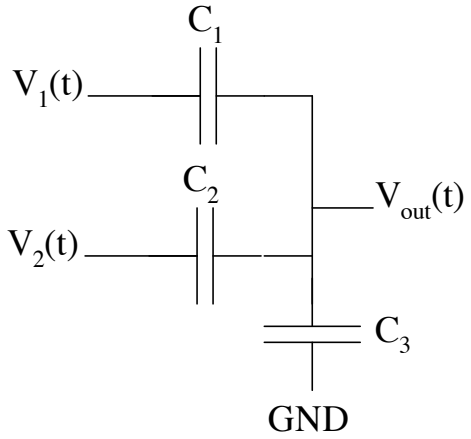

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Now on to other circuit approaches…..

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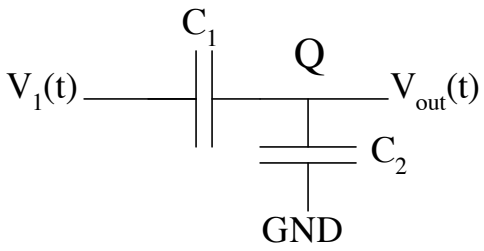

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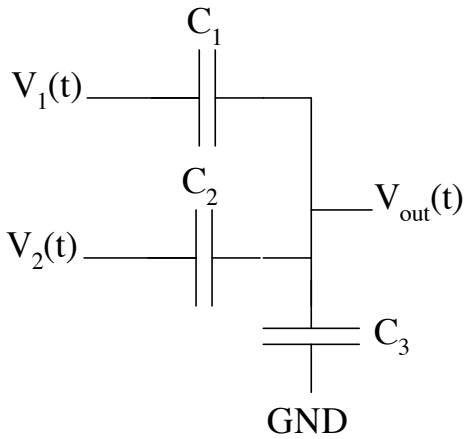

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What about Op-Amp circuits?

- Will assume MOSFET inputs
  (i.e. capacitive only input load
  therefore we have capacitive circuits
  and no significant leakage)

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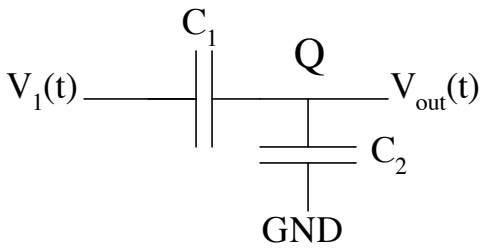

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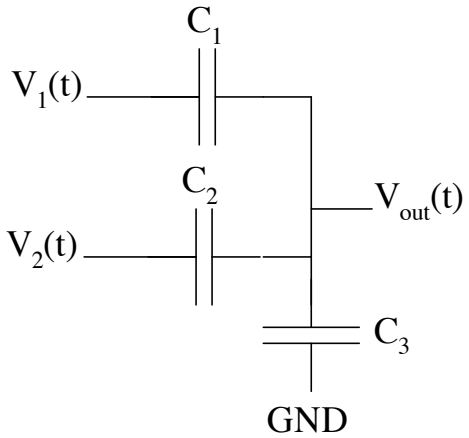
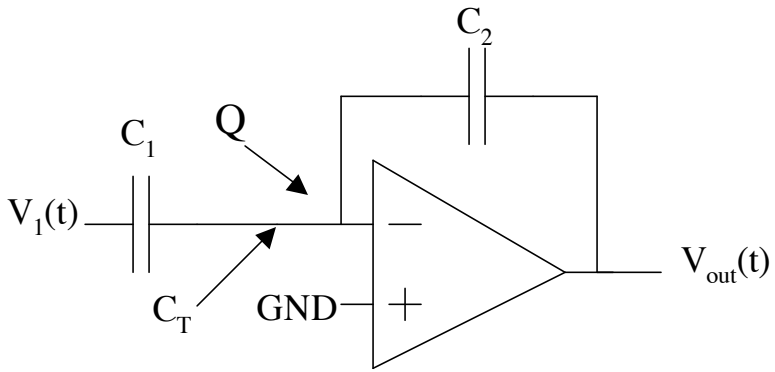


$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{C_2}{C_T} V_2(t) + \frac{Q}{C_T}$$

Capacitive Feedback

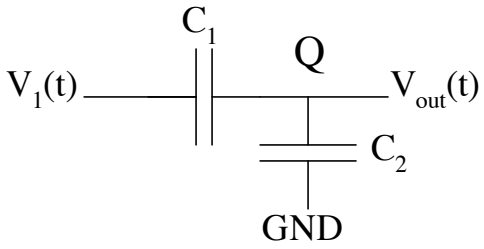


C_T is all of the capacitance at this node, including C_1, C_2, and any additional capacitance to a fixed potential (like gate capacitance, etc.)

We define C_w as the total capacitance connected to this node and to a "fixed" potential

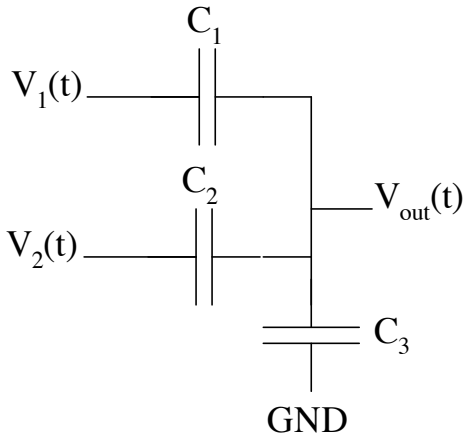
Capacitor Circuits

Capacitive Voltage Divider



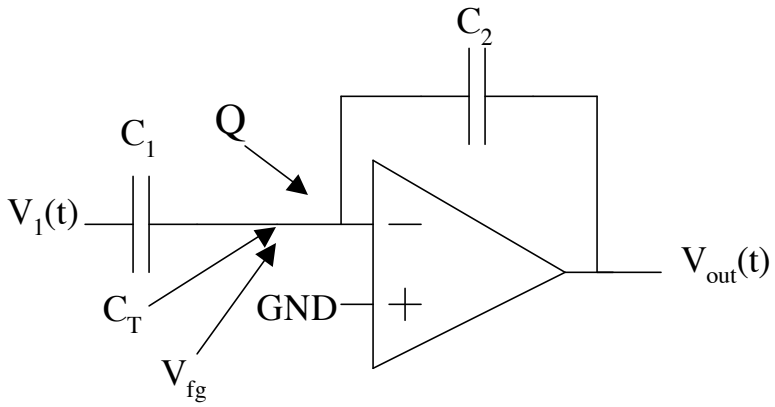
$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{Q}{C_T}$$

Multiple Input Voltage Divider



$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{C_2}{C_T} V_2(t) + \frac{Q}{C_T}$$

Capacitive Feedback



$$C_T \frac{dV_{fg}(t)}{dt} = C_1 \frac{dV_1(t)}{dt} + C_2 \frac{dV_{out}(t)}{dt}$$

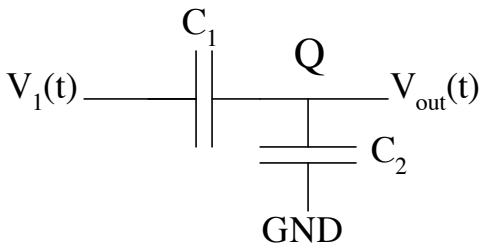
Integrating with time, we get

$$Q + C_1 V_1(t) + C_2 V_{out}(t) = C_T V_{fg}(t)$$

where Q is the constant of integration,
which equals the charge on the floating-node

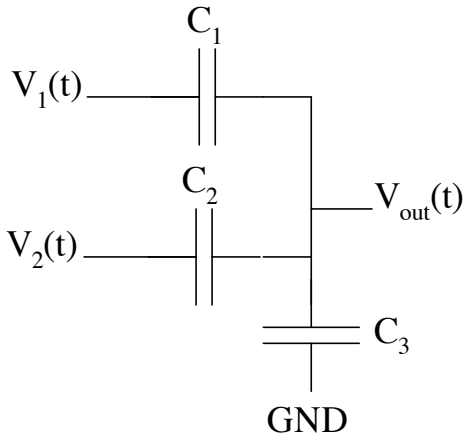
Capacitor Circuits

Capacitive Voltage Divider



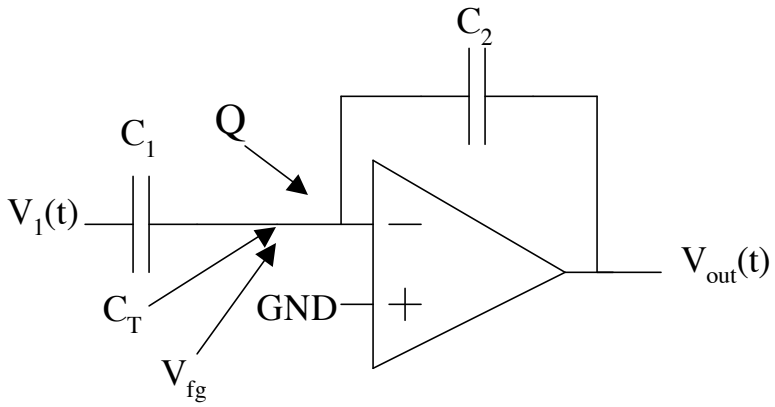
$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{Q}{C_T}$$

Multiple Input Voltage Divider



$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{C_2}{C_T} V_2(t) + \frac{Q}{C_T}$$

Capacitive Feedback



$$Q + C_1 V_1(t) + C_2 V_{out}(t) = C_T V_{fg}(t)$$

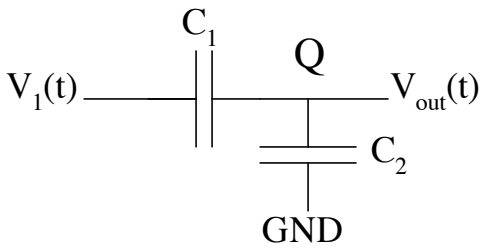
Assume the amplifier has a fixed gain, A_v.

$$Q + C_1 V_1(t) + (C_2 + (C_T / A_v)) V_{out}(t) = 0$$

$$V_{out}(t) = - \frac{C_1}{C_2 + (C_T / A_v)} V_1(t) - \frac{Q}{C_2 + (C_T / A_v)}$$

Capacitor Circuits

Capacitive Voltage Divider



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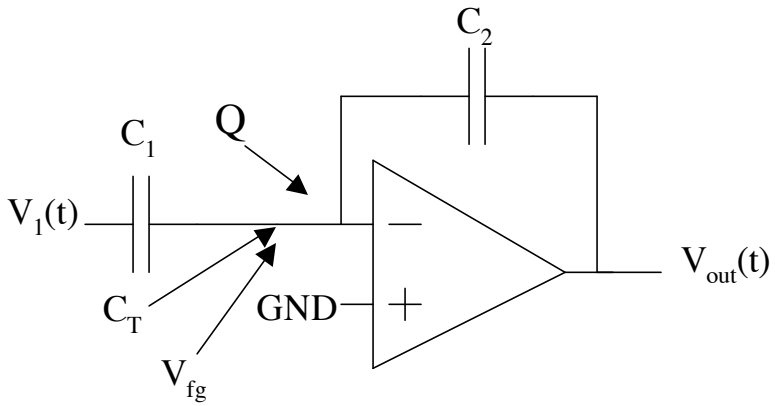
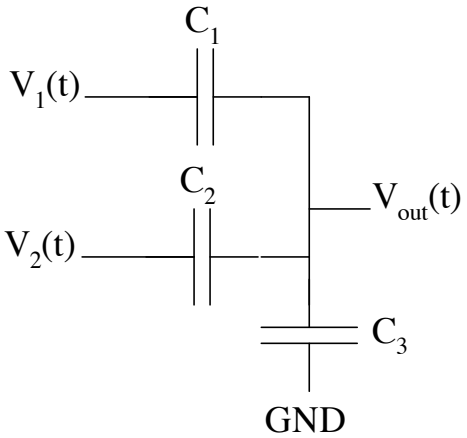
Capacitive Feedback

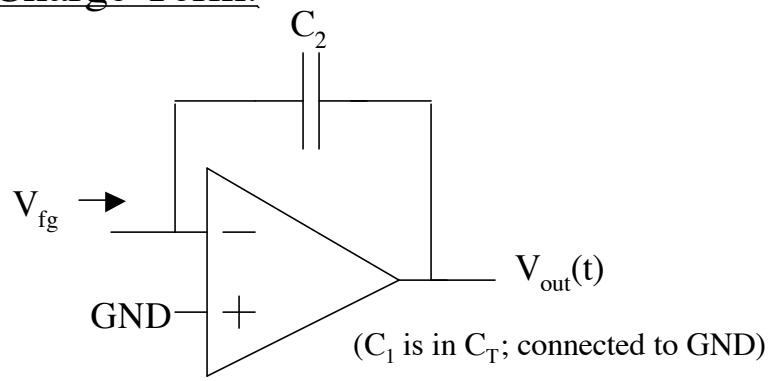


Multiple Input Voltage Divider



$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{C_2}{C_T} V_2(t) + \frac{Q}{C_T}$$

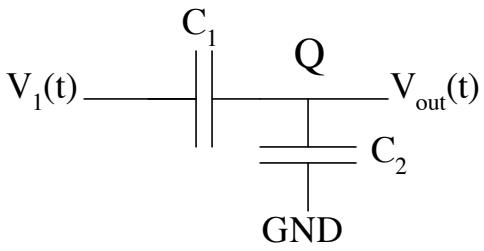
The Charge Term:



(C_1 is in C_T; connected to GND)

Capacitor Circuits

Capacitive Voltage Divider



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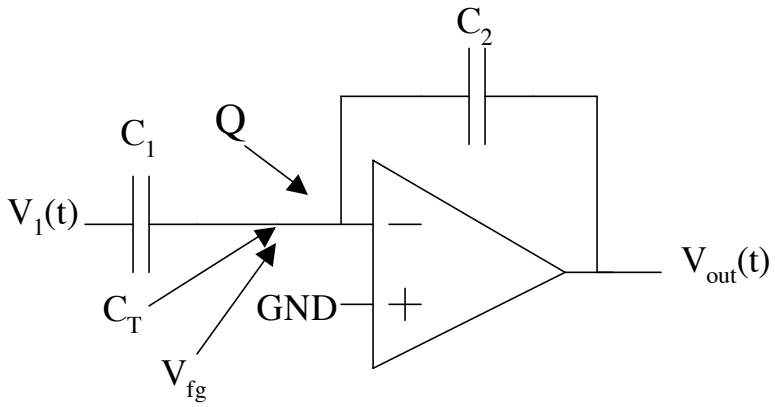
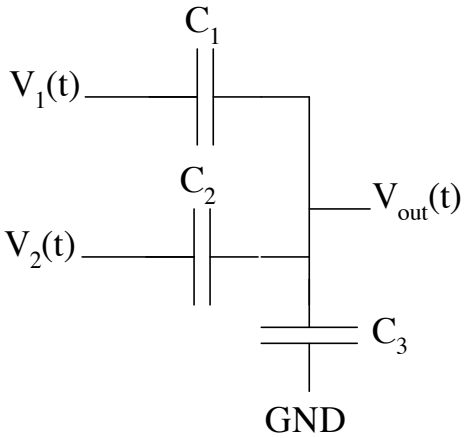


Multiple Input Voltage Divider



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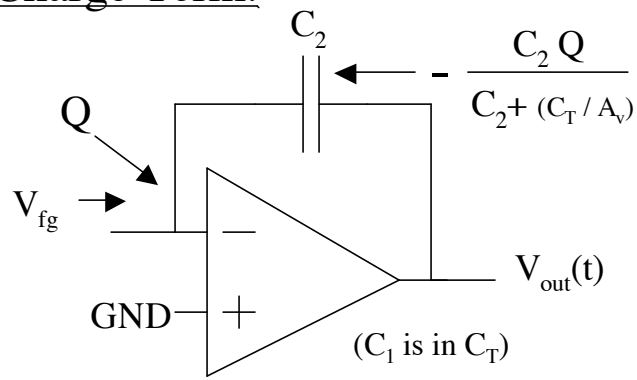
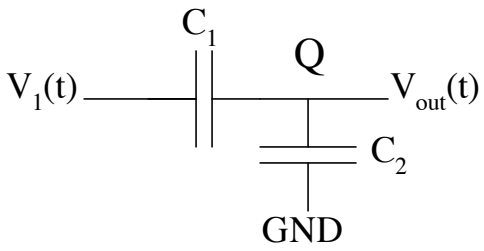


Capacitor Circuits

Capacitive Voltage Divider



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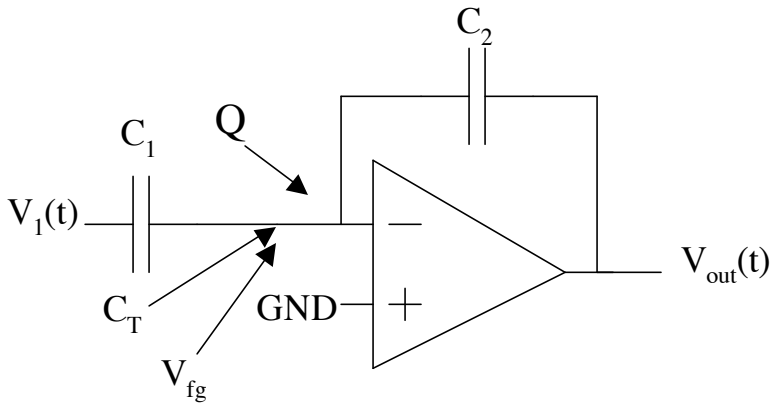
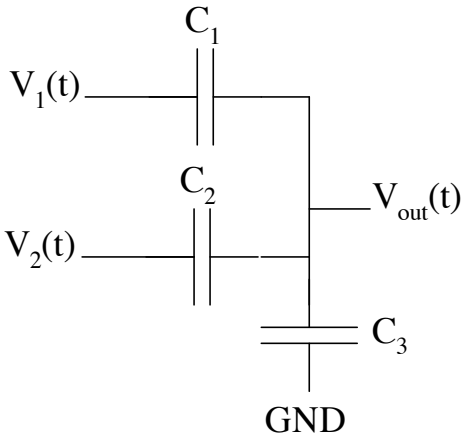
Capacitive Feedback



Multiple Input Voltage Divider



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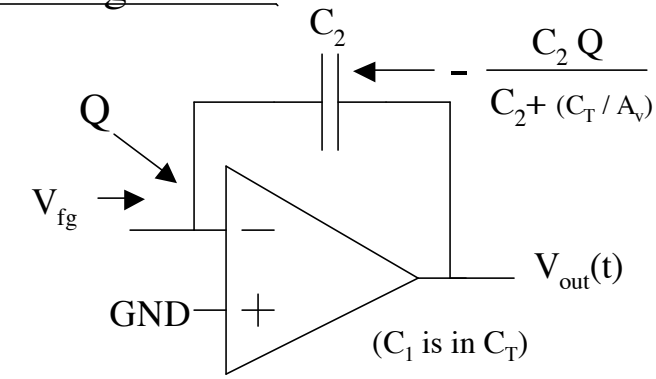
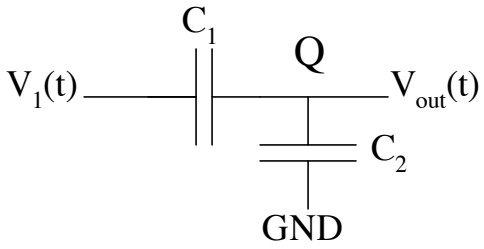


$$V_{out}(t) = - \frac{Q}{C_2 + (C_T / A_v)}$$

Capacitor Circuits

Capacitive Voltage Divider



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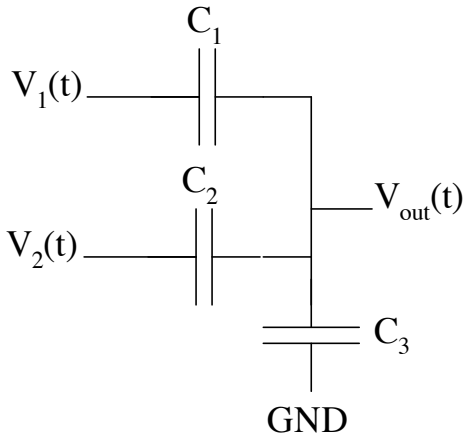

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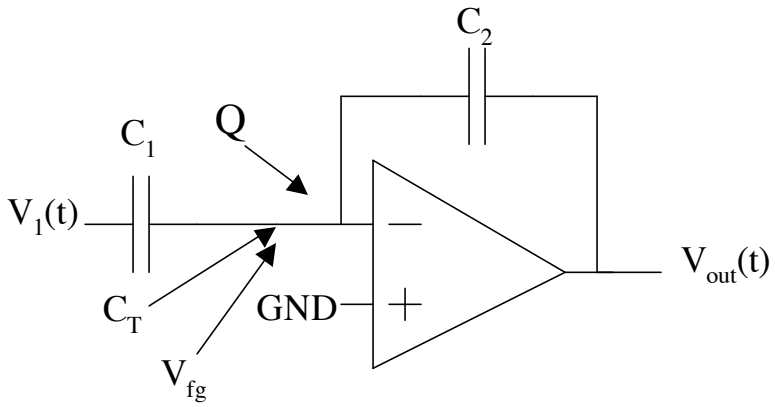
Capacitive Feedback



$$V_{out}(t) = -\frac{C_1}{C_2 + (C_T / A_v)} V_1(t) - \frac{Q}{C_2 + (C_T / A_v)}$$

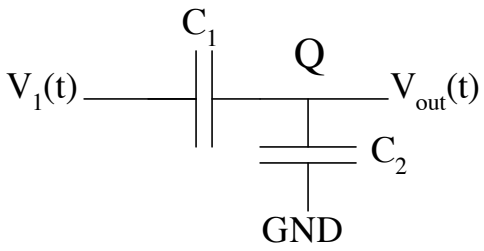
If A_v is large, then we reduce the effect of C_T

Since $A_v >> 1$, we often start with the assumption that C_T / A_v is negligible.

$$V_{out}(t) = -\frac{C_1}{C_2} V_1(t) - \frac{Q}{C_2}$$

Capacitor Circuits

Capacitive Voltage Divider



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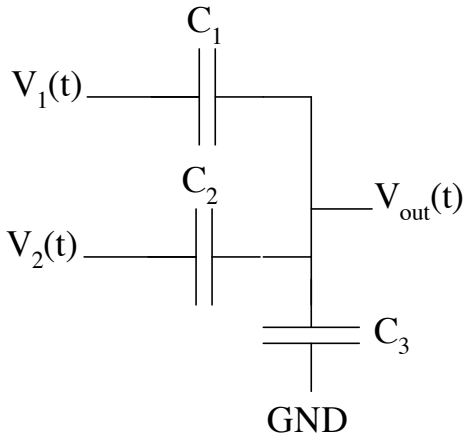
Multiple Input Voltage Divider



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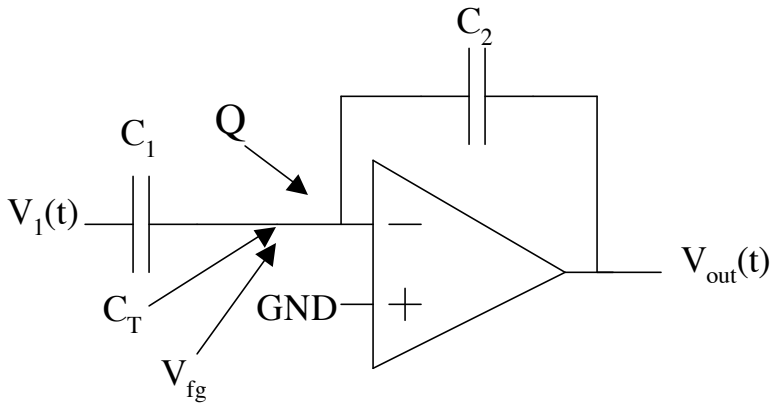
Capacitive Feedback



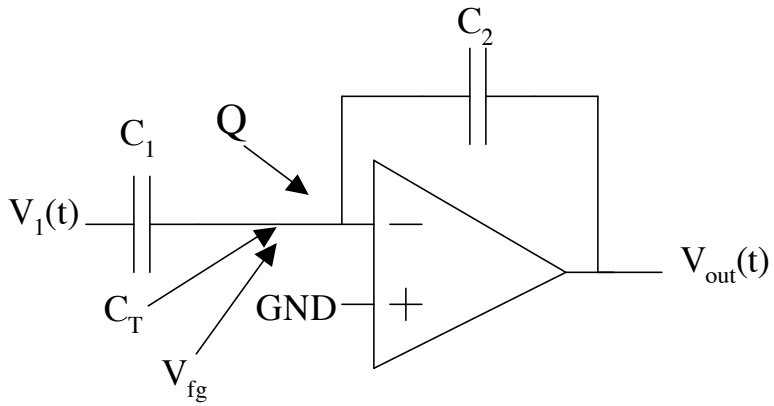
$$V_{out}(t) = -\frac{C_1}{C_2} V_1(t) - \frac{Q}{C_2}$$

We could get the same result if we say the – terminal ~ GND

$$C_1 \frac{dV_1(t)}{dt} = -C_2 \frac{dV_{out}(t)}{dt}$$

Capacitor Circuits

Capacitive Feedback



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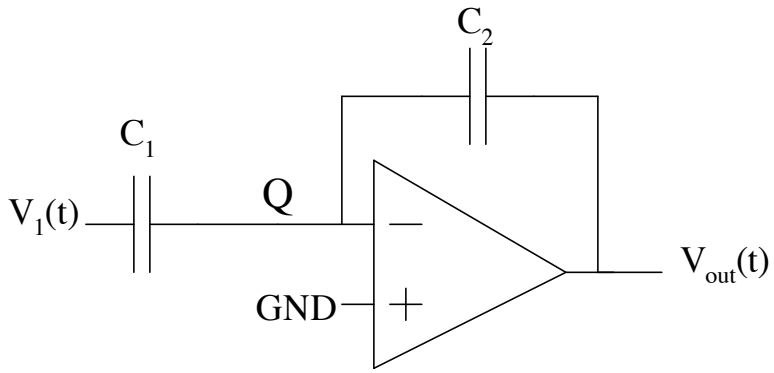
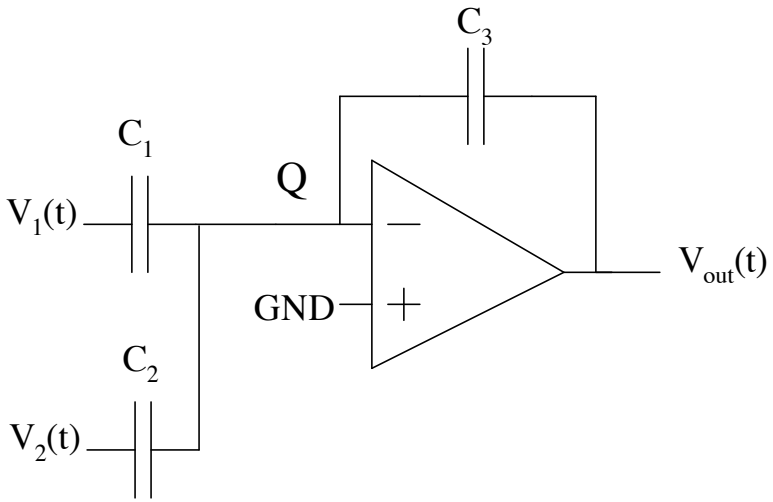
Capacitor Circuits

Capacitive Feedback



$$V_{out}(t) = -\frac{C_1}{C_2} V_1(t) - \frac{Q}{C_2}$$

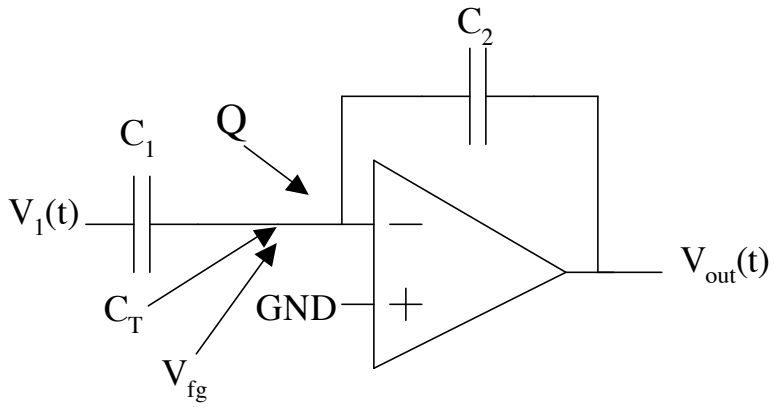


$$V_{out}(t) = -\frac{C_1}{C_3} V_1(t) - \frac{C_2}{C_3} V_2(t) - \frac{Q}{C_3}$$

We get summation with gain

Capacitor Circuits

Capacitive Feedback (Inverting)

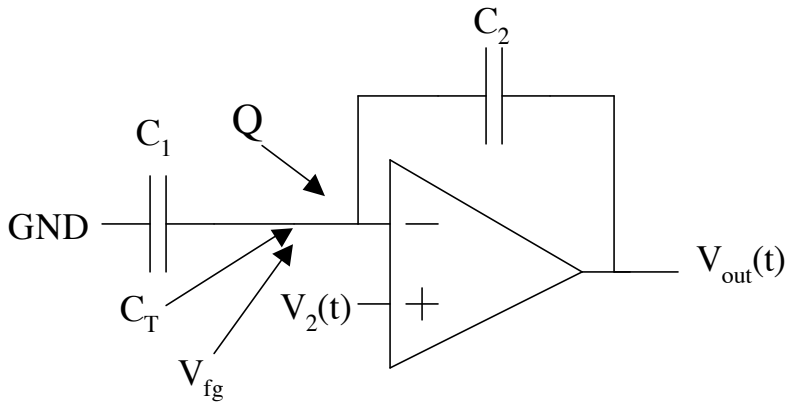


$$V_{out}(t) = -\frac{C_1}{C_2} V_1(t) - \frac{Q}{C_2}$$

We could get the same result if we say the – terminal ~ GND

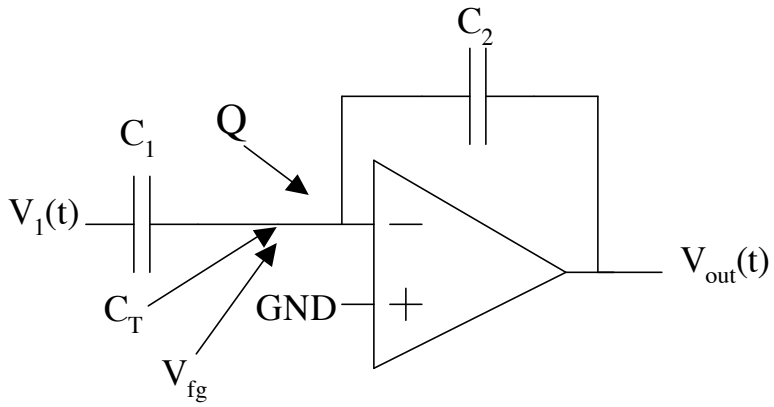
$$C_1 \frac{dV_1(t)}{dt} = -C_2 \frac{dV_{out}(t)}{dt}$$

Capacitive Feedback (Non-Inverting)



Capacitor Circuits

Capacitive Feedback (Inverting)



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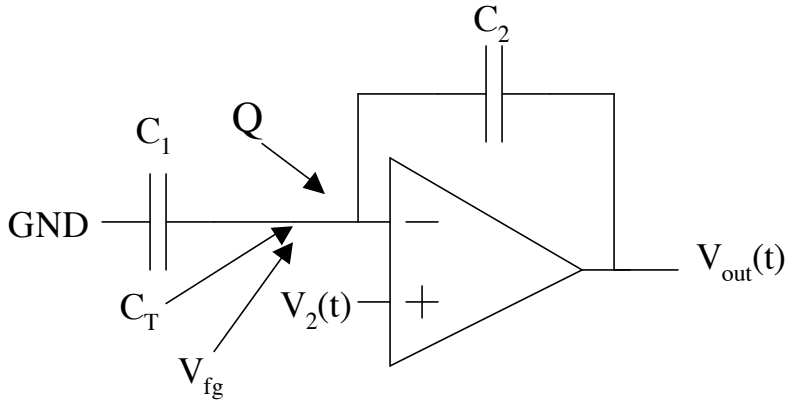
Capacitive Feedback (Non-Inverting)



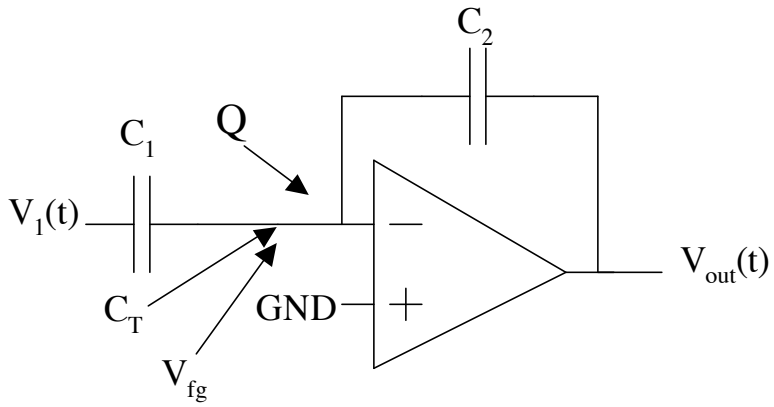
Start with C_T / A_v is negligible ($A_v >> 1$)

$$C_1 \frac{dV_2(t)}{dt} = C_2 \left(\frac{dV_{out}(t)}{dt} - \frac{dV_2(t)}{dt} \right)$$

$$(C_1 + C_2) \frac{dV_2(t)}{dt} = C_2 \frac{dV_{out}(t)}{dt}$$

Capacitor Circuits

Capacitive Feedback (Inverting)



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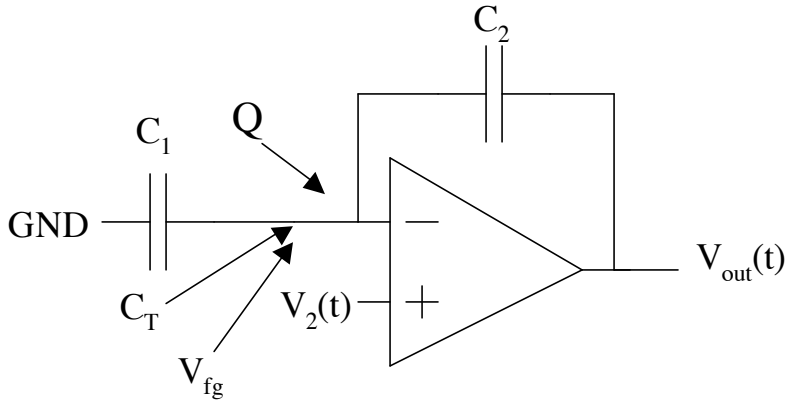
Capacitive Feedback (Non-Inverting)



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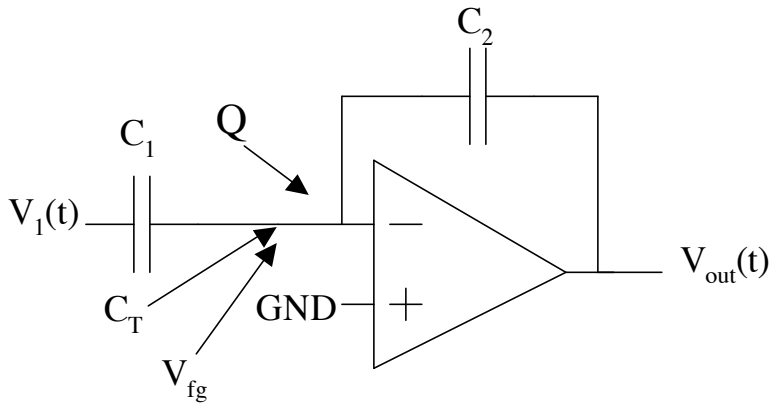
$$C_1 \frac{dV_2(t)}{dt} = C_2 \left(\frac{dV_{out}(t)}{dt} - \frac{dV_2(t)}{dt} \right)$$

$$(C_1 + C_2) \frac{dV_2(t)}{dt} = C_2 \frac{dV_{out}(t)}{dt}$$

$$V_{out}(t) = \left(1 + \frac{C_1}{C_2}\right) V_1(t) - \frac{Q}{C_2}$$

Capacitor Circuits

Capacitive Feedback (Inverting)



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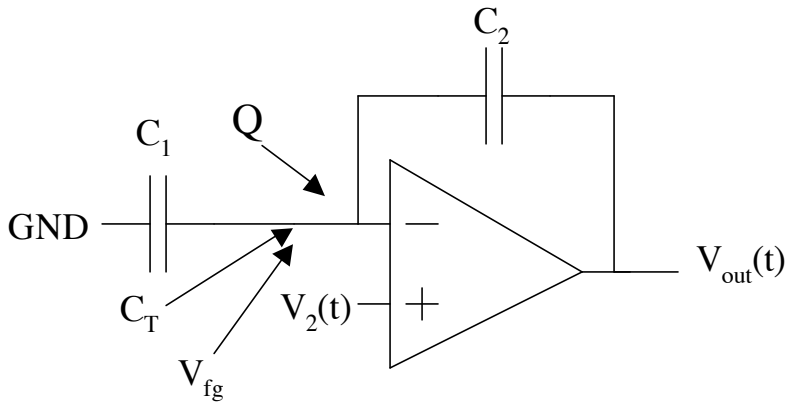
Capacitive Feedback (Non-Inverting)



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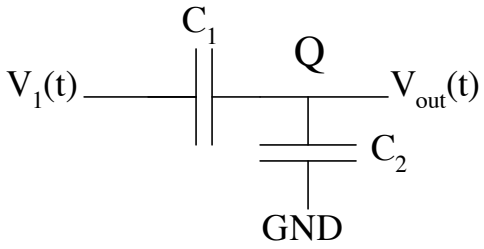
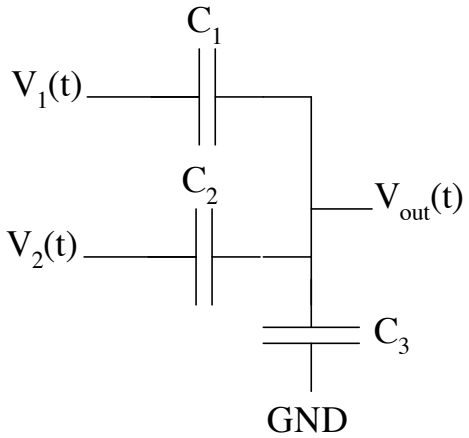
Capacitor Circuits

Capacitive Voltage Divider



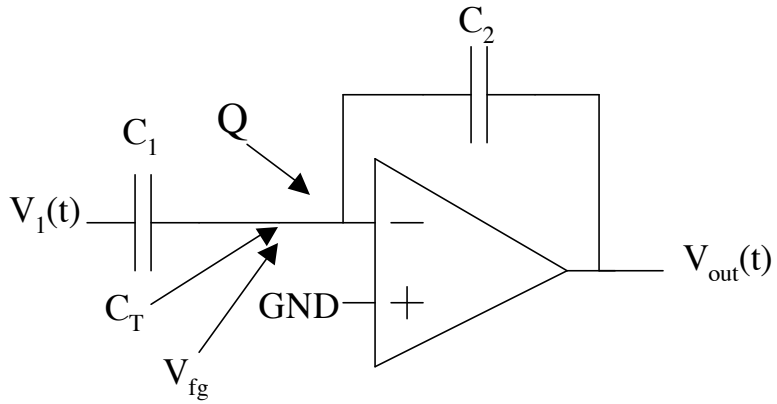
$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{Q}{C_T}$$

Multiple Input Voltage Divider

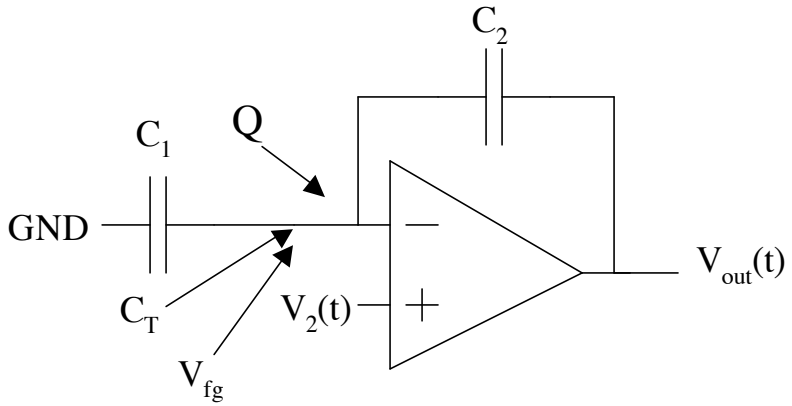


$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{C_2}{C_T} V_2(t) + \frac{Q}{C_T}$$

Capacitive Feedback



$$V_{out}(t) = -\frac{C_1}{C_2} V_1(t) - \frac{Q}{C_2}$$



$$V_{out}(t) = \left(1 + \frac{C_1}{C_2}\right) V_1(t) - \frac{Q}{C_2}$$