Analog Integrated Circuits and Signal Processing (2018) 94:65–74
https://doi.org/10.1007/s10470-017-1084-2

A compact low-power algorithmic A/D converter implemented on a large scale FPAA chip

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Received: 28 June 2017 / Revised: 25 September 2017 / Accepted: 17 November 2017 / Published online: 23 November 2017

Abstract
This paper presents an impact and low power algorithmic ADC which is implemented on a large scale field programmable analog array chip. The proposed circuit is merely composed of the elements within a single computational analog block (CAB) to minimize the area and parasitic effects. The feedback residue is amplified by a simple operational transconductance amplifier with a gain of − 2. Therefore, a new algorithm for the conversion process is proposed for this negative gain structure. Furthermore, owing to the floating-gate technique adopted in this work, the parameters and routes of the ADC achieve exceptional reconfigurability. The offset, reset, reference, threshold voltages, and gain all can be adjusted for optimizing the ADC performance. The measured results of the DNL is + 2/− 1 LSB and the INL is + 1.8/− 1.4 LSB, respectively. Under an 8-bit resolution and a 62.5 Hz sampling frequency condition, the measured effective number of bit is 7.6 bits. The total current consumption of the OTAs and FGOTAs is 1.6 μA under a 2.5 V supply voltage. Each CAB which includes all components, switches, and routings occupies an area of $400 \times 500\,mm^2$.

Keywords Algorithmic ADC · Floating-gate technique · Field programmable analog array (FPAA) · Low power

1 Introduction

For biomedical signal sensing applications, small form factor and low power consumption are two of the critical requirements to portable devices for long term operating [1, 2]. Therefore, most of the popularly developed high speed analog to digital converters (ADC) which consume large amount of power can not satisfy the specification. To achieve low power, papers presented various kinds of successive approximation register (SAR) ADCs. However, the SAR ADCs demand large circuit area for the passive components and the digital logic gates. Furthermore, the mismatch, placement and routing complexities will be increased with higher resolution designs [3]. Although these issues can be improved by using a advanced fabrication process, the capacitors and the logics still occupy a large proportion of the circuit area.

In this paper, an algorithmic ADC is employed to obtain the high efficiency of the trade-off between power consumption, resolution, and circuit area for biomedical sensing devices [4]. As shown in Fig. 1(a), the whole ADC can be considered as a circuit which only contains amplifiers and switches. The ADC of algorithmic topology doesn't require a comparator array such as that of flash or pipeline structures. Also, the feedback of the algorithmic ADC can be relized without using high resolution DAC and logic state machine such as that in SAR ADCs. Additionally, the resolution is proportional to the conversion time, the specification can be adjusted by controlling the switch clocks to achieve higher resolution or higher speed. Moreover, since the simple circuit structure, the algorithmic ADC can be implemented on the prior proposed large scale field programmable analog array (FPAA) chip [5].

The block diagram of the FPAA chip is shown in Fig. 1(b). The switches and the components are implemented with floating-gate technique. Therefore, all the connections and the compositions of circuits can be

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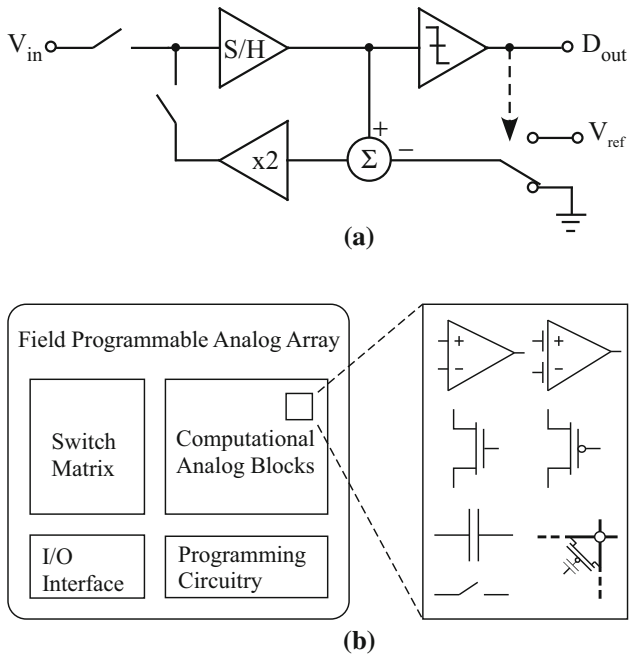

Fig. 1 **a** A basic block diagram of an algorithmic analog to digital converter. It is simplified to a structure which consists of amplifiers and switches. All the components required can be complied by using the developed field programmable analog array (FPAA) chip. **b** The block diagram of the large scale FPAA chip. The switches and the computation analog blocks (CAB) can be configured by operating the programming circuitry. Each CAB contains two FGOTAs, two OTAs, two *p*MOS transistors, two *n*MOS transistors, four capacitors, four T-gate switches and a large number of floating-gate-transistor switches for the routing

configured through controlling the programming circuitry. The high flexibilities is conducive to implement and modify the algorithmic ADC performance for different requirements of individual applications. There are totally 82 (6×14) computation analog blocks (CAB) on a chip, and each CAB includes basic analog elements such as transconductance operational amplifiers (OTA), floating-gate input OTAs (FGOTA), MOSFETs, capacitors, transmission gates (T-gate), and FG switches. To minimize the area and parasitic effects, the entire algorithmic ADC is designed and built within one single CAB with the restricted components.

By implementing the ADC on the FPAA chip, the gain, offset voltages, and reference voltages of the ADC are all adjustable. Also, the circuit can be easily integrated into a power-efficient analog system by designing and programming other circuits in the rest of the CABs [6]. For example, the ADC can be connected to amplifiers or filters programmed from other CABs for sensing applications, or can be programmed in different CABs as a multiple channel ADC array for analog signal processing. Without external input/output (I/O) pads and extra routing on PCB board, the device area and the influence from the environment can be minimized to implement a highly power-efficient device with a small form factor.

This paper is organized as follows. The design principles of the proposed algorithmic ADC and the usages of the components are presented in Sect. 2. The operational algorithm and the voltage setting analysis is described in Sect. 3. The measurement results of the sub-circuit and the ADC are shown in Sect. 4. Finally, the conclusion of proposed algorithmic ADC on the FPAA is presented in Sect. 5.

2 Architecture of algorithmic ADC

The proposed algorithmic ADC as shown in Fig. 2(a) is composed of a sample and hold (S/H), a gain of 2 amplifier (G2A), a voltage summation unit, and a comparator. All the components including amplifiers, capacitors, switches, and reference voltages are implemented in one CAB. Therefore, except the supply ground sources, no extra circuits such as regulators or I/O buffers are required for this algorithmic ADC.

The non-overlapping-clock sequences as shown in the Fig. 2(b) are generated from the mixed-signal processor (MSP430) and applied through the general purpose input/output (GPIO) which are also implemented on chip. The sampling phase (Φ_S) overlaps the first phases of resetting (Φ_R) and amplifying (Φ_A) for the maximum sampling time as well as the minimum power of S/H. In Φ_A, the comparator will generate the MSB code, and the G2A will amplify the held voltage with or without a reference-voltage (V_{ref}) summation depending on the MSB. After the amplifying, the load switch will be tuned on in the loading phase (Φ_L), and will load the residue to the input node of the S/H circuit. Thereupon, the reset switches will be closed again to reset the amplifier for the next bit-conversion step (MSB-1). All the switches on the signal paths are implemented with T-gate switches to minimize the distortion and charge injection effects.

2.1 Applications of the FGOTAs

The topology of the FGOTA is shown in Fig. 3(a). The current source is implemented with a *p*MOS floating-gate transistor for the adjustability of the FGOTA tail current and bandwidth. Since the transistors are operated in sub-threshold region, the low-pass cut-off corner is proportional to the tail current. Therefore, the current can be programmed accurately to obtain sufficient bandwidth for individual applications without wasting power on over-designing the bandwidth. The floating-gate reliability have been presented and verified in [7].

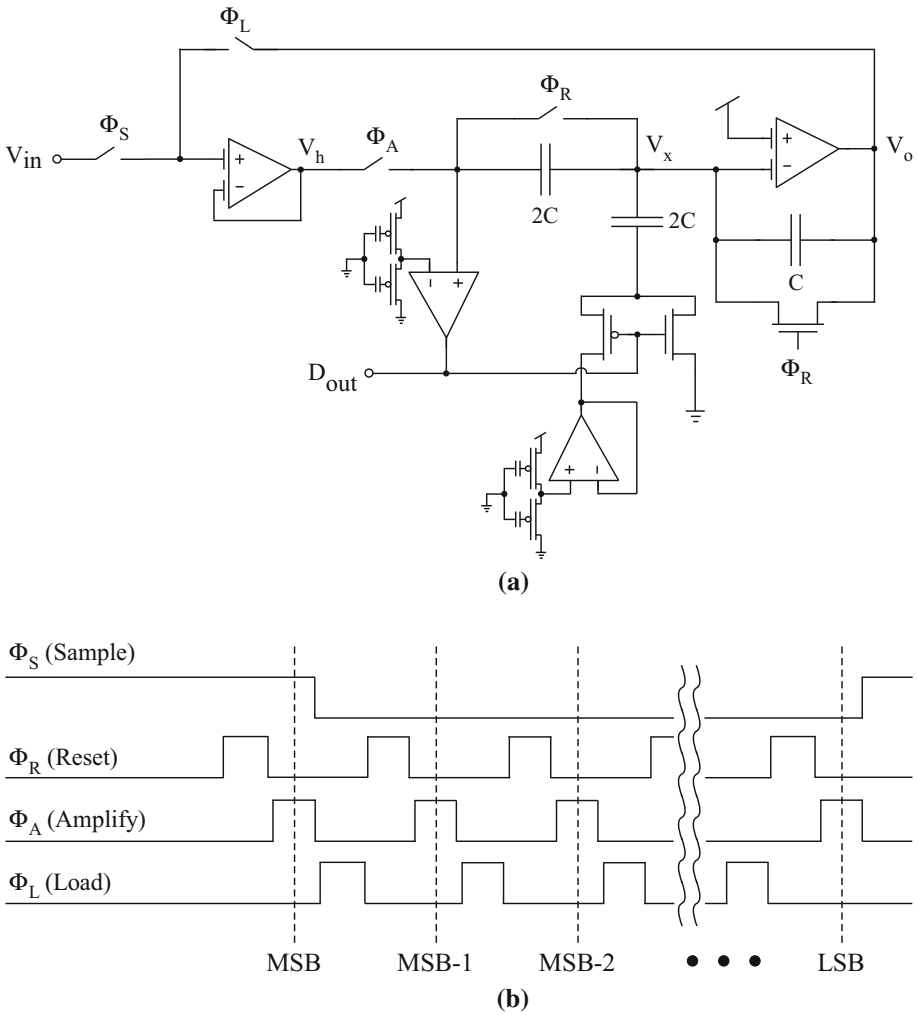

Fig. 2 **a** The architecture of the proposed algorithmic ADC. All the voltage sources are generated on chip in the same CAB of the core circuit. The floating-gate programming switches are not shown for simplicity. **b** The non-overlapping clock sequence for the ADC. The clock patterns are also generated by compiling the on chip mixed-signal processor and general purpose inputs/outputs (GPIO) as the clock generators

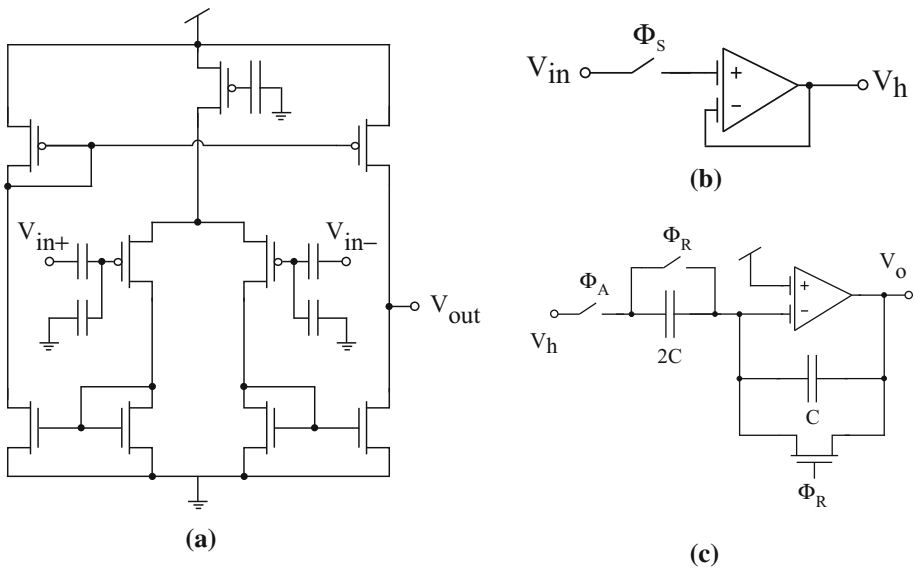

Fig. 3 **a** The architecture of the floating-gate OTA. The floating-gate technique is utilized for implementing the current source to control the tail current, and for the differential pair to adjust the input offset voltage. **b** The sample and hold circuit which is implemented by using the FGOTA. **c** The capacitive feedback charge amplifier is composed of the capacitors, the switches, and the FGOTA

Besides the current source, the input differential pair transistors are designed with floating-gate transistors in FGOTA. The input offset voltage can be trimmed out by programming different amounts of charge into the two floating gates. Moreover, because of the capacitive input attenuation (CIA) structure with the small value capacitors at inputs, the linearity of the FGOTAs is improved without cost extra current consumption. Therefore, to achieve high resolution, one of the FGOTAs is chosen to implement a highly linear S/H circuit with a unit gain feedback loop, as shown in Fig. 3(b).

Besides, since the resolution of a algorithmic ADC is directly affected by the G2A linearity, the other FGOTA is employed for the amplifier. furthermore, to achieve high power efficiency and low circuit complexity, a capacitive feedback charge amplifier structure is utilized for the G2A [8, 9], as shown in Fig. 3(c). The close-loop gain of G2A is set by the capacitance ratio $2C/C$, and can be adjusted by reconfiguring the capacitor arrays which are built in the CAB. The output and input of the amplifier are reset between each amplifying period, and the reset voltage is set by programming the floating-gate transistor at the positive-input node of the FGOTA. In addition, the linearity of the reset switch doesn't affect the performance. Hence, the reset switch is implemented by a single *n*MOS transistor.

2.2 Applications of the regular OTAs

The topology of the OTA is a conventional 9-transistor OTA with a floating-gate current source, as shown in Fig. 4(a). Without the capacitive input attenuation, the non-FG OTAs possess large transconductance (G_m) comparing to that of the FGOTAs. Therefore, the non-FG OTAs are used for the parts which require high gain or high frequency, such as a comparator and a DC voltage generator.

In the voltage summation unit which is shown in Fig. 4(b), the reference-voltage generator is implemented by using the regular OTA with a unit gain feedback loop. The high open-loop gain characteristic of the OTA is needful to obtain a stable reference voltage. The DC voltage at the positive input node is biased by a resistive voltage divider with two *p*MOS pseudo resistors. Those two *p*MOS transistors are designed to be the configurable switches for the connection to V_{DD} and gnd. However, instead of programming to be fully tuned on or tuned off, the resistance values of the transistors can be controlled through programming the charges at the floating-gate nodes. Moreover, since the leakage current at the gate node is minute, the current flowing through the *p*MOS transistors can be programmed to around 1.5 nA for saving the power consumption. On top of that, the control signal for the voltage summation unit is generate by the comparator output and connected to the gates of the *p*MOS and the *n*MOS transistors. Accordingly, the reference voltage is summed into the G2A input voltage when the comparator output is switches to low. Furthermore, The energy only dissipates if the comparator output is changed.

The other OTA with high gain is employed for the comparator to achieve short settling time. Besides, to drive the I/O pad without using any buffer from other CAB, the comparator also requires wide bandwidth. The schematic

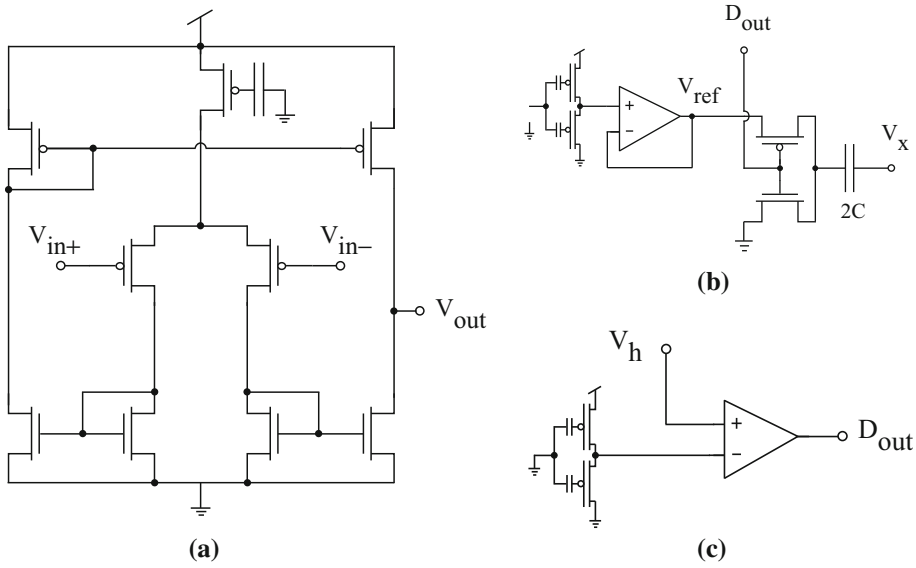

Fig. 4 **a** The architecture of the conventional 9-transistor OTA with a floating-gate current source. **b** The voltage summation unit with the two MOSFET switches, the OTA, and the configurable voltage divider. **c** The schematic of the comparator for the ADC. The threshold level can be adjusted through programming the pseudo resistors

of the comparator is shown in Fig. 4(c). The positive-input node is connected with the input of the G2A, and the negative-input node is biased by the voltage divider. The voltage divider structure is the same as the one used in the voltage summation unit.

3 Analysis

In a conventional algorithmic ADC, the basic conversion concept is shown in Fig. 5(a). If the input voltage of the G2A is within the top half of the full-scale range, the voltage will be subtracted by the half of the full scale voltage (V_{FS}). Then, extend the segment back to the full scale through multiplying the voltage by 2 for the next bit conversion. In terms of the voltage which locates within the bottom half, the input will be amplified directly without a voltage subtraction. After n cycles, a n-bit serial digital output (D_{out}) will be obtained from the comparator. The functions can be displayed as

$$V_o = 2 \cdot \left(V_h - \frac{V_{FS}}{2} \cdot D_{out} \right), \tag{1}$$

where V_o is the output of the G2A, V_h is the held output voltage of the S/H circuit as well as the input of the G2A, and D_{out} is the digital output of the ADC. A value of 1 presents high, and a 0 presents low in (1). As the calculation example shown in Fig. 5(b), the subtraction in each period is operated accordingly to obtain the correct results. The output digital code for 0.6 V input under 1 V full scale condition is 1001.

3.1 Proposed algorithm with a negative amplifier gain

However, the conventional method mentioned above only works with a positive G2A gain. In a single CAB on the developed FPAA chip, there is no extra OTA or FGOTA for a double inverting amplifier. The G2A can only be implemented by using one FGOTA with a negative gain. To resolve the issue, a new conversion method is proposed in this paper. As shown in Fig. 6(a), because of the negative amplifier gain, the voltage segments are reversed in each periods. Therefore, the digital output of even number bits have to be inverted for the correct results. Moreover, since a the circuit is supplied by 0 and 2.5 V, the amount of the subtraction voltage needs to be modified to get a positive output value without a negative value of gain, as shown in Fig. 6(b). The equations of the proposed method are

$$V_o = -2 \cdot \left[V_h - \frac{V_{FS}}{2} \cdot (D_{out} + 1) \right], \tag{2}$$

As a result, the obtained output of the proposed method is the same as that of a conventional one.

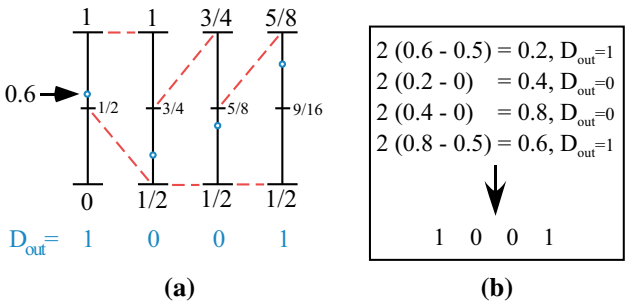

Fig. 5 **a** The conventional algorithm of the algorithmic ADC. The voltage segment which the held voltage (V_h) exists is taken and amplified by 2 for every conversion step. **b** The calculations of the algorithm. V_h is subtracted by half of the full scale voltage (V_{FS}) when D_{out} is high

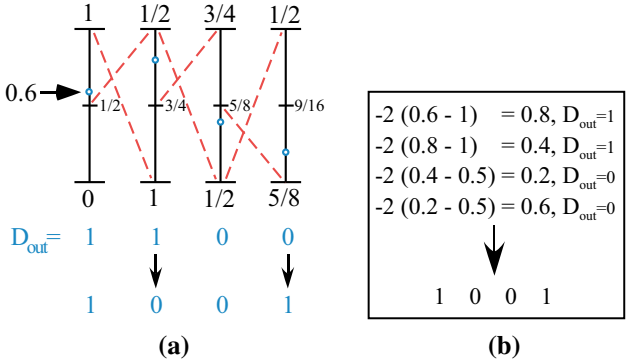

Fig. 6 **a** The proposed algorithm in this paper with a gain of -2 amplifier. **b** V_h is subtracted by V_{FS} if D_{out} is high, and subtracted by $V_{FS}/2$ if D_{out} is low. After the simple decodeing for even number bits, the digital results are the same as the conventional ADC outputs

3.2 Reset and reference voltage settings

Nevertheless, due to the bulk of the nMOS transistors are connected to ground, the negative voltage at input of G2A will cause forward current from the transistor-bulk nodes, and the negative voltages will be complemented to around 0 V. Besides, the function (2) is based on a ground-referred condition. For a single-end capacitive feedback amplifier with a 0 V source supply, the output is relative to the voltage difference between the input and the reset voltages. Also, the reset voltage is usually higher than 0 V for keeping all the transistors in saturation region during the operation. The output-voltage function of the G2A designed in this paper can be calculated by using the law of charge conservation,

$$C \cdot (V_o - V_{reset}) = 2C \cdot [V_{reset} - V_h - V_{ref} \cdot (D_{out} - 1)], \quad (3)$$

where V_{reset} is the reset voltage of the G2A, V_{ref} is the reference voltage for the summation. Both of the voltages can be adjusted in continuum because of the floating-gate technique. Hence, V_{reset} and V_{ref} are the two main programming objects for acquiring the demanded equations. After the simplification and the transposition of (3), the equation can be displayed as

$$V_o = -2 \cdot \left[\left(V_h - \frac{3}{2} V_{reset} \right) - V_{ref} \cdot (D_{out} - 1) \right]. \quad (4)$$

To obtain the exactly same terms of those in (2), V_{reset} has to be set to $2V_{FS}/3$, and V_{ref} has to be set to $V_{FS}/2$. Since the negative input of the comparator is programmed at $V_{FS}/2$, the comparator output is 1 during the resetting phase. Therefore, if V_h is lower than $V_{FS}/2$, the *p*MOS switch will be tuned on for the voltage summation. Conversely, if the D_{out} is 0, the *n*MOS switch will remain closed without consuming extra current. By using this proposed setting, all the voltages are operated in the operational range. The amplifier is implemented with only one FGOTA for minimizing the power consumption and the area.

3.3 Gain error effects

The gain error of G2A affects the ADC resolution significantly, as the measured wave forms which are recorded from the ADC output with triangle inputs, and converted by a ideal DAC shown in Fig. 7. If the absolutely value of gain is higher than 2, the output voltage of G2A will be saturated to V_{DD} or to gnd when V_h is close to $V_{FS}/2$ and both ends of operational range. Furthermore, the ADC output code will be converted to 128 since the G2A is saturated in MSB conversion. Also, the effects appear at codes of $V_{FS}/2 \pm V_{FS}/(2^{n+1})$ because of the saturation in MSB-*n*, where $n = 1, 2, ..., bit - 1$. The measured results with a -2.25 G2A gain is shown in Fig. 7(a). Conversely, if the absolutely value of the gain is less than 2, the output voltages will converge to V_{reset} gradually. Hence, noticeable missing codes occupy around code 128 and both ends of V_{FS} as shown in Fig. 7(b) which of the gain is configured to -1.75. Therefore, to optimize the output linearity, the the G2A input to feedback capacitor ratio has to be designed carefully and accurately. In the presented design, due to the floating-gate FPAA and the capacitor arrays in CAB, the gain of G2A is programmed and configured highly approximate to -2. The recorded wave form is shown in Fig. 7(c) for the verification.

4 Measurement results

The proposed algorithmic ADC can be compiled and programmed on a large scale field programmable analog array chip which is fabricated in a standard 0.35 µm CMOS process. In the testing-bench setting, the total current consumption of the OTAs and FGOTAs is 1.6 µA. The allocation of power is 12.5, 18.8, 6.2, and 62.5% for the S/H, G2A, voltage generator, and comparator, respectively. The distribution of the elements and the signal routes are shown in Fig. 8(a). All the circuit blocks are placed on the right side of the CAB. Therefore, the signal and power buses can be congregated together to realized a reconfigurable routing structure. Each intersection nodes of the lines are implemented by *p*MOS floating-gate transistors as

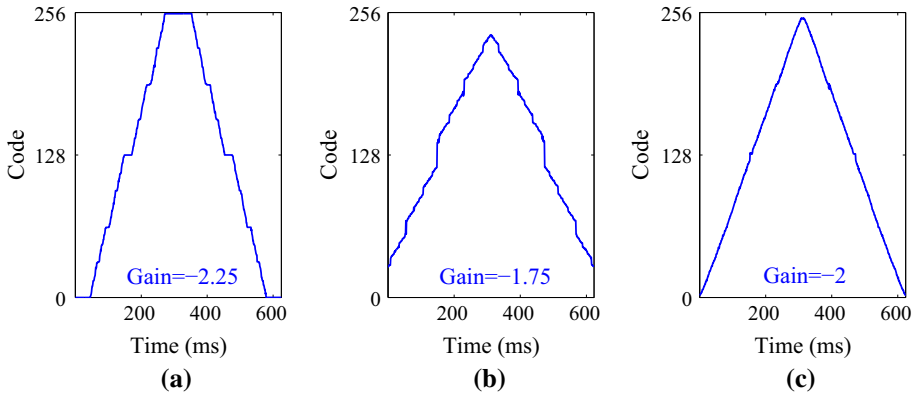

Fig. 7 The gain error effects on the output wave form. **a** With a -2.25 amplifier gain, the output codes accumulate at code 128 since the G2A was saturated when input approach to $V_{FS}/2$. **b** While the gain is configured to -1.75, the jumps appear around code 128, and the operational range is decreased. **c** The ADC performs linear output waveform when the gain of G2A is set approximately to -2

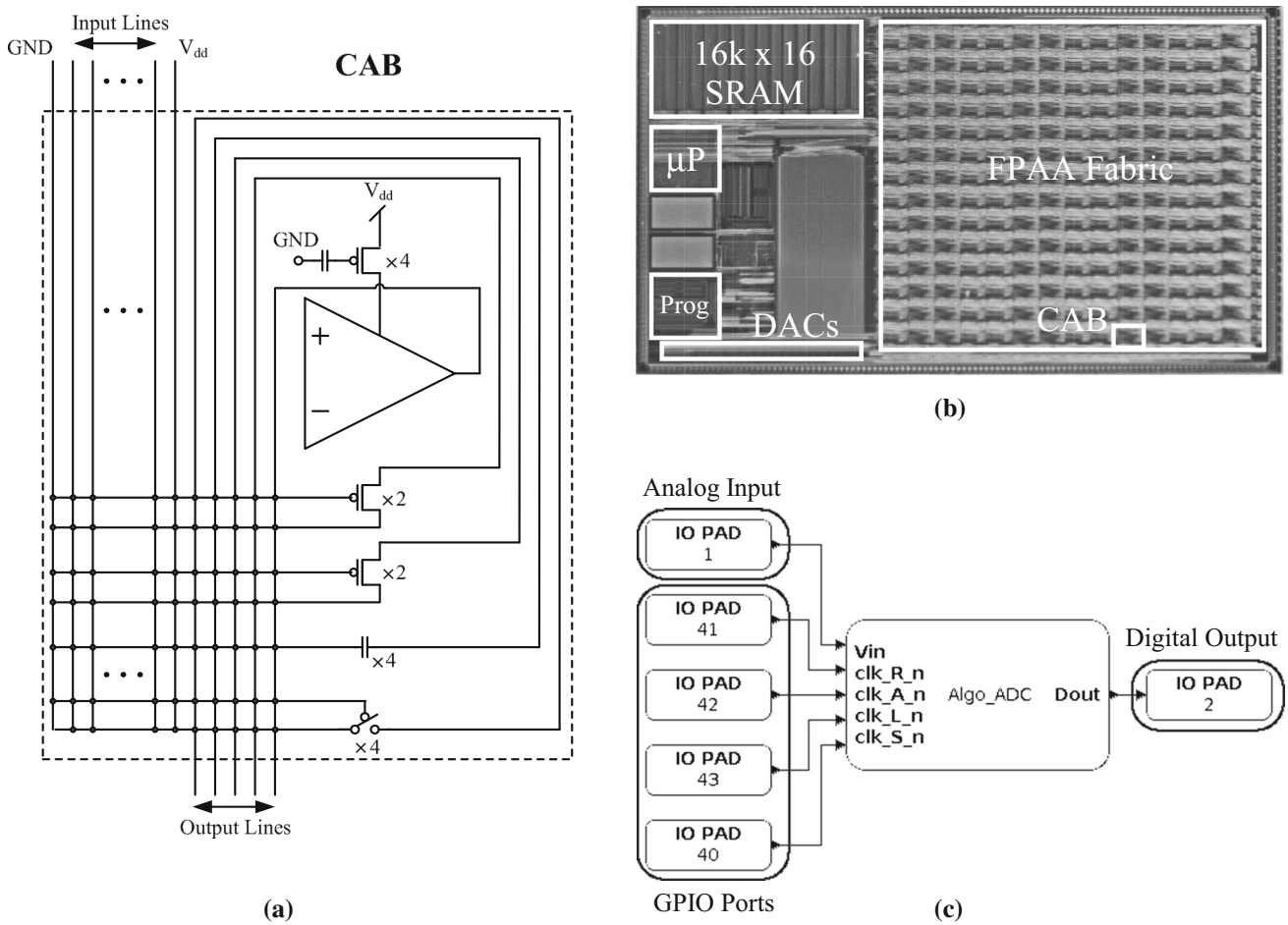

Fig. 8 **a** The layout plan of one CAB. The signal buses are arranged on the left side of the block. Each intersection nodes of the signals are realized by *p*MOS floating-gate transistors. **b** The die photo of the FPAA chip with 82 CABs. Each CAB occupies an area of $400 \times 500\,\mathrm{mm}^2$. **c** The friendly user interface with icons and the I/O connections of the developed ADC, which is created through using a compiling system

programmable switches. The connections can be easily changed in accordance with applications. The die photo is shown in Fig. 8(b), and the area of one CAB is $400 \times 500\,\mathrm{mm}^2$. An ADC block is created in the FPAA compiling system for the convenience of use and measurements, as that shown in Fig. 8(c). Furthermore, users can easily integrate the ADC with other circuits by simple connections between individual circuit blocks.

The input offset and charge injection measurement results are taken by using the S/H circuit. In Fig. 9(a), an obvious offset exits between the held voltage and the input voltage of S/H. However, by programming a opposite offset for the compensation, the held output can be highly matched to the input voltage, as shown in Fig. 9(b). Figure 9(c) shows the subtraction of the held and sampled voltages. After the smoothing to eliminate the noise, the charge injection variance is within 25 mV in a full scale input range.

The G2A measurements are taken with a 1 kHz switching frequency, and the wave form are shown in Fig. 10(a). The output is reset at 1.667 V properly in resetting phase, and the V_{ref} is set to be 1.25 V for a 2.5 V rail to rail input ramp signal. The threshold level for the voltage-summation trigger is at 1.25 V. The close loop gain of the G2A is plotted in Fig. 10(b). The gains approach to -2 within full input range.

The measured DNL is $+2/-1$ LSB, and the INL is $+1.8/-1.4$ LSB, as shown in Fig. 11(a). The sampling frequency of the ADC is set at 62.5 Hz for the FFT measurement with 2048 data points. The input frequency is set at 24.99 Hz, and the measured efficient number of bit (ENOB) is 7.6 bits under an 8-bit resolution condition. The spectrum is presented in Fig. 11(b). The 2nd harmonic distortion is eliminated because of the well-set G2A gain. Furthermore, the SNDR and SFDR measurements with different input frequencies are shown in Fig. 12 to verify

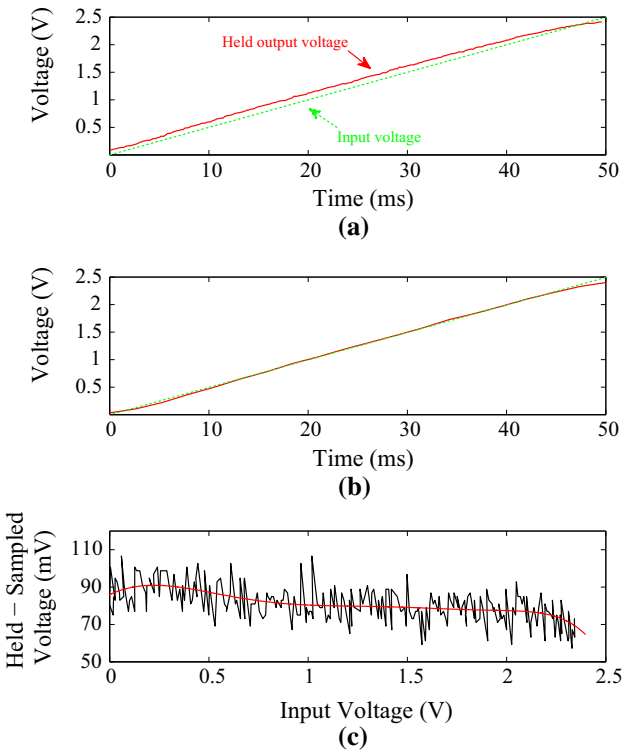

Fig. 9 **a** The comparison of the S/H input and output voltages before tuning the floating-gate inputs. **b** The curve of the S/H output approximately fits that of the input signal after trim out the offset by programming the charges at the floating-gate terminals. **c** The charge injection values versus the sensed input voltages. The definition of charge injection value is the difference between the voltages held by the S/H subtracted and the input voltages applied by the signals generator

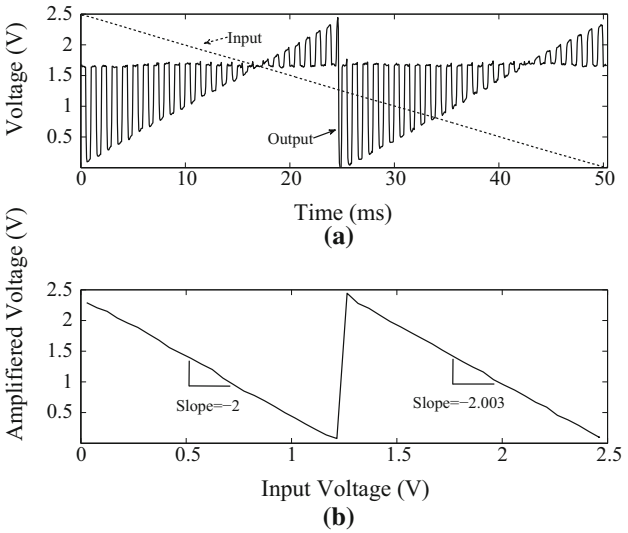

Fig. 10 **a** The measured wave form of the G2A output and input with 1 Hz switching frequency. V_{reset} is set at 1.67, and V_{ref} is 1.25 for a $2.5V_{pp}$ input swing range. The voltage summation trigger signal is generated by the comparator, and the trigger level is set at 1.25. **b** The amplifier gain is verified by taking the output voltages in amplifying phases and connecting the points. The gains are approximately -2

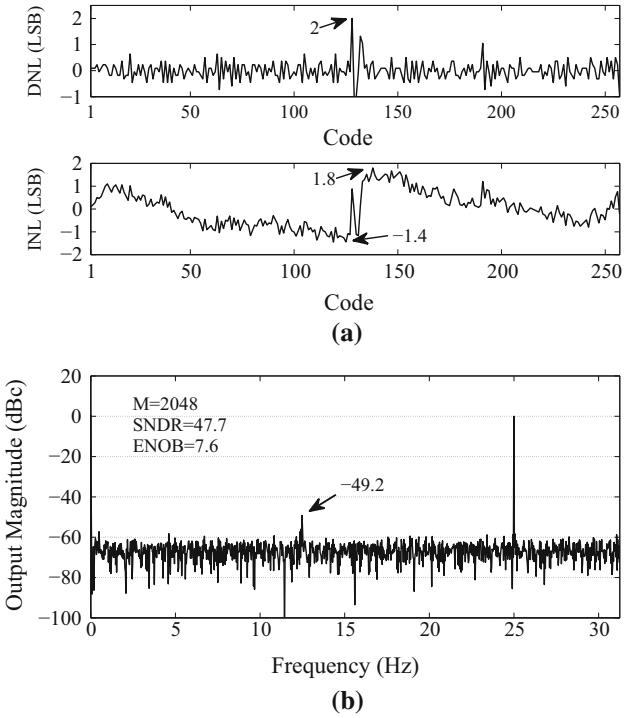

Fig. 11 **a** The DNL and the INL measurements. **b** The FFT measurement with 2048 data points. The SNDR is 47.7 dBc, and the ENOB is 7.6 under an 8-bit resolution condition. The input frequency is 24.99 Hz, and the second-high tone appears at the 3rd harmonic frequency which is around 12.5 Hz due to the frequency folding effect

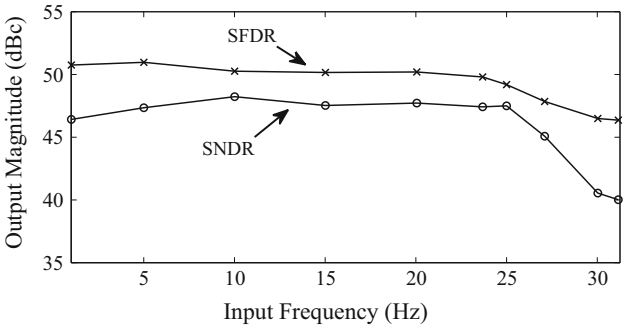

Fig. 12 The measured SNDR and SFDR versus input frequency at 62.5 Hz sampling rate

the reliability of the proposed ADC. The measured characteristics of the proposed ADC are summarized in Table 1 along with the performance comparison. The figure of merit (FoM) is given by

$$FoM = \frac{\text{Power}}{2^{\text{ENoB}} \times min\{\text{F}_s, 2 \times \text{ERBW}\}}. \quad (5)$$

where F_s is sampling frequency and F_{in} is effective resolution bandwidth [10].

Table 1 Comparasion of the measured ADC performance

Parameter	This work	[11] JSSC	[12] JSSC
Process (μm)	0.35	1.5	0.13
Supply voltage (V)	2.5	5	3
Current (μA)	1.6	3200	10,500
Sampling frequency (Hz)	62.5	125 k	10 M
Input frequency (Hz)	30	4 k	1 M
SNDR (dB)	47.7	71	56
ENoB (bit)	7.6	11.5	9
FoM (pJ/conv.-step)	329	691	29
DNL (LSB)	$+2/-1$	± 0.4	± 0.9
INL (LSB)	$1.8/-1.4$	± 0.21	± 3.5
Area (mm^2)	0.2	5.94	0.19
Reconfigurability	Speed, power, resolution	N/A	N/A

5 Conclusion

This paper presents an algorithmic ADC implemented on a large scale FPAA chip to achieve low power consumption with a small form factor. All the components are reconfigurable because of the floating-gate technique. The programmable floating-gate switches on the chip are compiled to implement and to optimize the ADC. The parameters including bandwidth, offset, reset, reference, threshold voltages, and amplifier gain can be adjusted by tuning the charge at the floating-gate nodes. The entire ADC only consists of two OTAs, two FGOTAs, four transistors, three capacitor arrays, four T-gates, and four floating-gate pseudo resistors within one CAB for the minimized power and area. The clocks are generated by the MSP430, and transmitted through the GPIO to the ADC. Owing to the CAB array, the ADC can be easily integrated into biomedical sensors or intelligent systems with the circuits compiled in other CAB. Furthermore, the circuits or systems can be tested rapidly without redoing the design and the fabrication.

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