BLOCK DIAGRAM OF A DIGITAL-ANALOG CONVERTER

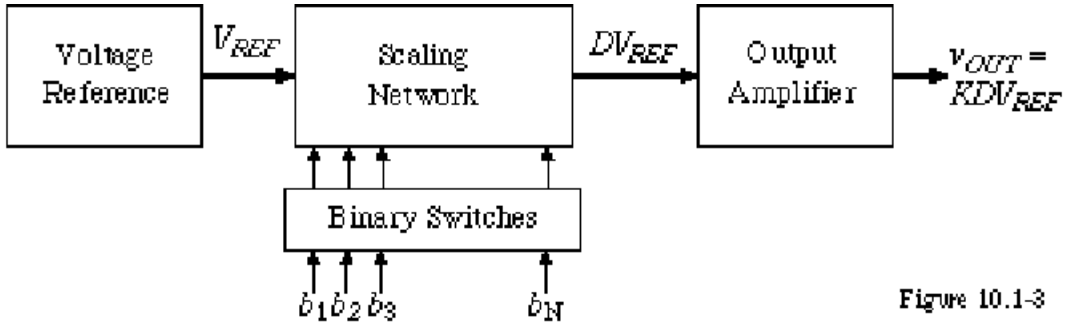

Figure 10.1-3

b_1 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

b_N is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

10.1 - CHARACTERIZATION OF DIGITAL-ANALOG CONVERTERS

STATIC CHARACTERISTICS

OUTPUT-INPUT CHARACTERISTICS

Ideal input-output characteristics of a 3-bit DAC

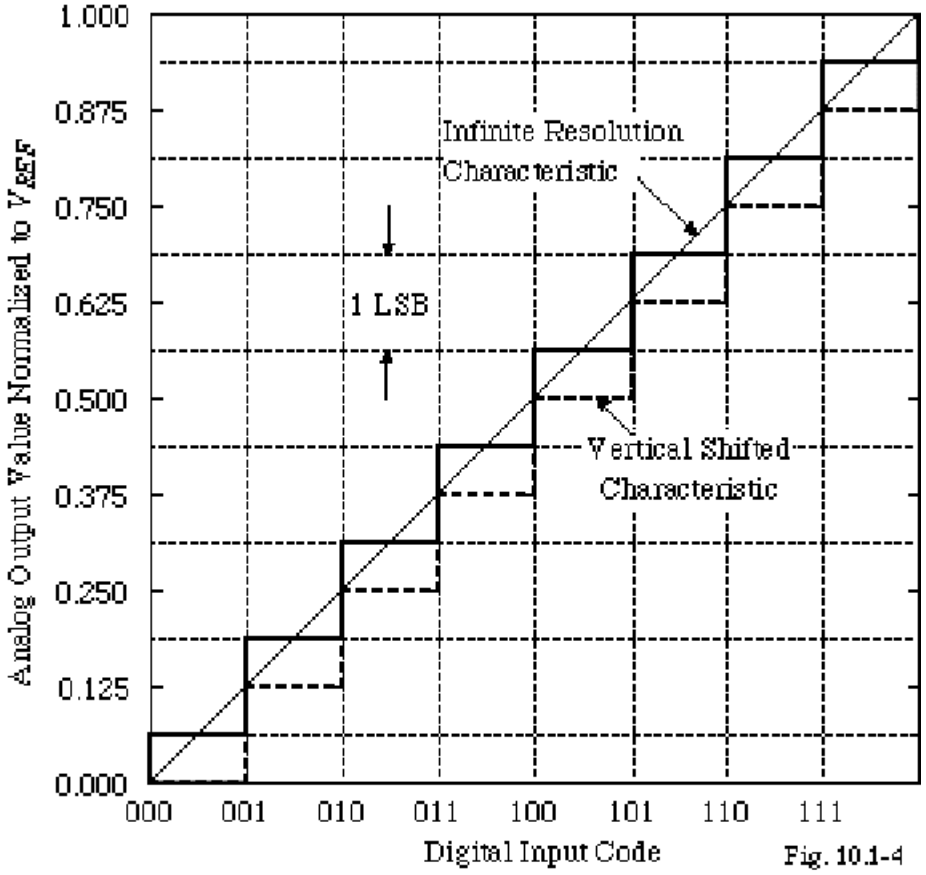

Fig. 10.1-4

DEFINITIONS

- *Resolution* of the DAC is equal to the number of bits in the applied digital input word.
- *The full scale* (FS):

  FS = Analog output when all bits are 1 - Analog output all bits are 0

  $$FS = (V_{REF} - \frac{V_{REF}}{2^N}) - 0 = V_{REF}\left(1 - \frac{1}{2^N}\right)$$

- *Full scale range* (FSR) is defined as

  $$FSR = \lim_{N\to\infty} FS = V_{REF}$$

- *Quantization Noise* is the inherent uncertainty in digitizing an analog value with a finite resolution converter.

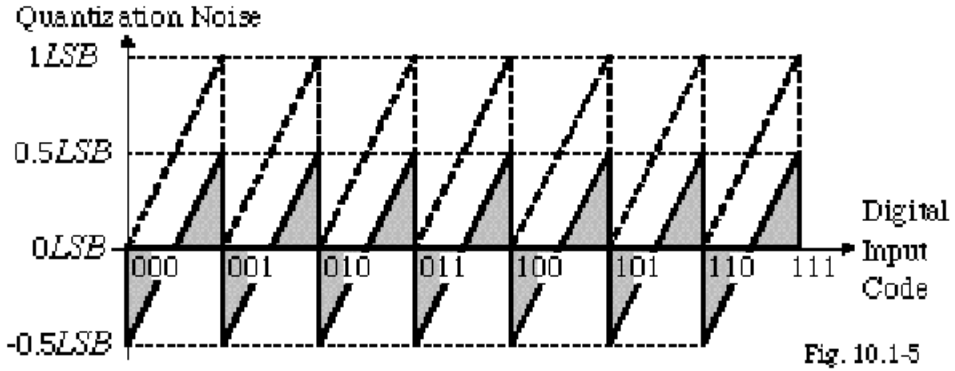

Fig. 10.1-5

MORE DEFINITIONS

- *Dynamic Range* (*DR*) of a DAC is the ratio of the *FS*R to the smallest difference that can be resolved (i.e. an *LSB*)

$$DR = \frac{FSR}{LSB \text{ change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N \text{ (dB)}$$

- *Signal-to-noise ratio* (*SNR*) for the DAC is the ratio of the full scale value to the *rms* value of the quantization noise.

$$rms(\text{quantization noise}) = \sqrt{\frac{1}{T}\int_0^T LSB^2\left(\frac{t}{T} - 0.5\right)^2 dt} = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}}$$

$$\therefore \quad SNR = \frac{v_{OUT}(rms)}{(FSR/\sqrt{12}\ 2^N)}$$

- *Maximum SNR* (SNR_{max}) is defined as

$$SNR_{max} = \frac{v_{OUT_{max}}(rms)}{(FSR/\sqrt{12}\ 2^N)} = \frac{FSR/(2\sqrt{2})}{FSR/(\sqrt{12}\ 2^N)} = \frac{\sqrt{6}\ 2^N}{2}$$

or in terms of decibels

$$SNR_{max}(dB) = 20\ log_{10}\left(\frac{\sqrt{6}\ 2^N}{2}\right) = 10\ log_{10}(6) + 20\ log_{10}\ (2^N) - 20\ log_{10}(2)$$

$$= 7.78\ dB - 6.02\ dB + 6.02N\ dB = 1.76\ dB + 6.02N\ dB$$

EVEN MORE DEFINITIONS

- *Effective number of bits (ENOB)* can be defined from the above as

$$ENOB = \frac{SNR_{Actual} - 1.76}{6.02}$$

where SNR_{Actual} is the actual *SNR* of the converter.

Comment:

The *DR* is the amplitude range necessary to resolve *N* bits regardless of the amplitude of the output voltage.

However, when referenced to a given output analog signal amplitude, the *DR* required must include 1.76 dB more to acount for the presence of quantization noise.

Thus, for a 10-bit DAC, the *DR* is 60.2dB and for a full-scale, *rms* output voltage, the signal must be approximately 62dB above whatever noise floor is present in the output of the DAC.

OFFSET AND GAIN ERRORS

An *offset error* is a constant difference between the actual finite resolution characteristic and the infinite resolution characteristic measured at any vertical jump.

A *gain error* is the difference between the slope of an actual finite resolution and an infinite resolution characteristic measured at the right-most vertical jump.

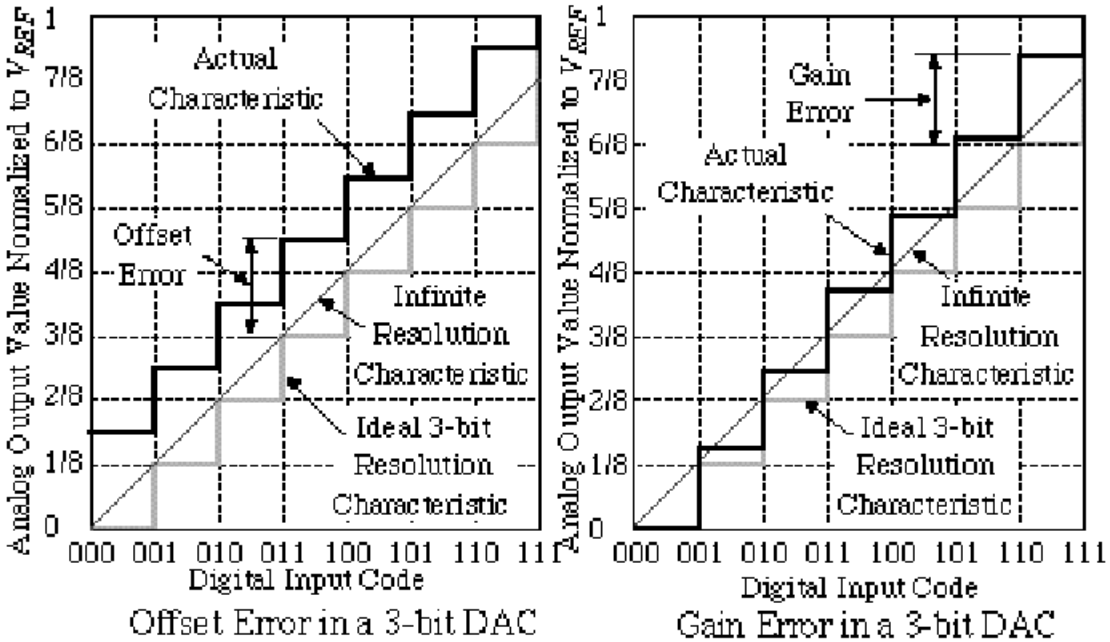

Fig. 10.1-6

INTEGRAL AND DIFFERENTIAL NONLINEARITY

- *Integral Nonlinearity* (*INL*) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*).
- *Differential Nonlinearity* (*DNL*) is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*).

$$DNL = \left(\frac{V_{cx} - V_s}{V_s}\right) \text{x } 100\% = \left(\frac{V_{cx}}{V_s} - 1\right) LSBs$$

where V_{cx} is the actual voltage change on a bit-to-bit basis and V_s is the ideal change ($V_{FSR}/2^N$)

Example of a 3-bit DAC:

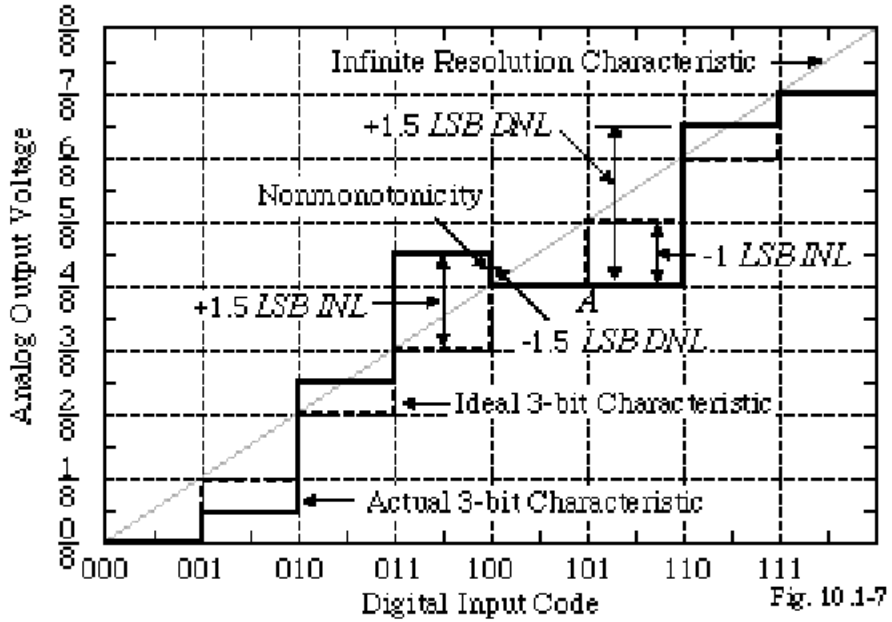

Fig. 10.1-7

EXAMPLE OF INL AND DNL OF A NONIDEAL 4-BIT DAC

Find the ±*INL* and ±*DNL* for the 4-bit DAC shown.

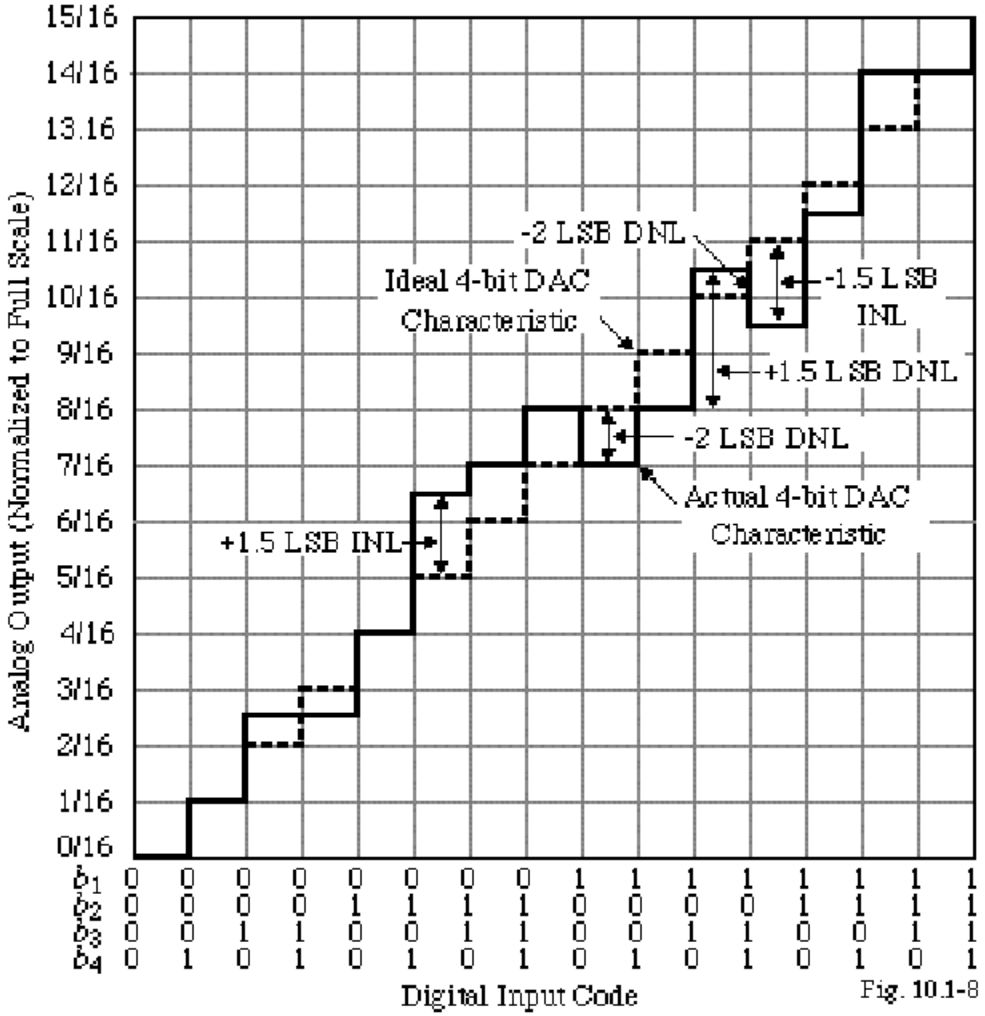

Fig. 10.1-8

DYNAMIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

Dynamic characteristics include the influence of time.

DEFINITIONS

- *Conversion speed* is the time it takes for the DAC to provide an analog output when the digital input word is changed.

  Factor that influence the conversion speed:

  Parasitic capacitors (would like all nodes to be low impedance)

  Op amp gainbandwidth

  Op amp slew rate

- *Gain error* of an op amp is the difference between the desired and actual output voltage of the op amp (can have both a static and dynamic influence)

$$\text{Actual Gain} = \text{Ideal Gain} \times \left(\frac{\text{Loop Gain}}{1 + \text{Loop Gain}} \right)$$

$$\text{Gain error} = \text{Ideal Output} - \text{Actual Output} = \frac{\text{Ideal Gain} - \text{Actual Gain}}{\text{Ideal Gain}} = \frac{1}{1 + \text{Loop Gain}}$$

EXAMPLE OF INFLUENCE OF OP AMP GAIN ERROR ON DAC PERFORMANCE

Assume that a DAC using an op amp in the inverting configuration with $C_1 = C_2$ and $A_{vd}(0) = 1000$. Find the largest resolution of the DAC if V_{REF} is 1V and assuming worst case conditions.

Solution

The loop gain of the inverting configuration is $LG = \frac{C_2}{C_1+C_2} A_{vd}(0) = 0.5 \cdot 1000 = 500$. The gain error is therefore $1/501 \approx 0.002$. The gain error should be less than the quantization noise of $\pm 0.5LSB$ which is expressed as

$$Gain\ error = \frac{1}{501} \approx 0.002 = \frac{V_{REF}}{2^{N+1}}$$

Therefore the largest value of N that satisfies this equation is $N = 7$.

INFLUENCE OF THE OP AMP GAINBANDWIDTH

Single-pole response:

$$v_{out}(t) = A_{CL}[1 - e^{-w_H t}]v_{in}(t)$$

where

A_{CL} = closed-loop gain

$$w_H = GB\left(\frac{R_1}{R_1+R_2}\right) \text{ or } GB\left(\frac{C_2}{C_1+C_2}\right)$$

To avoid errors in DACs (and ADCs), $v_{out}(t)$ must be within $\pm 0.5LSB$ of the final value by the end of the conversion time.

Multiple-pole response:

Typically the response is underdamped like the following (see Appendix C of text).

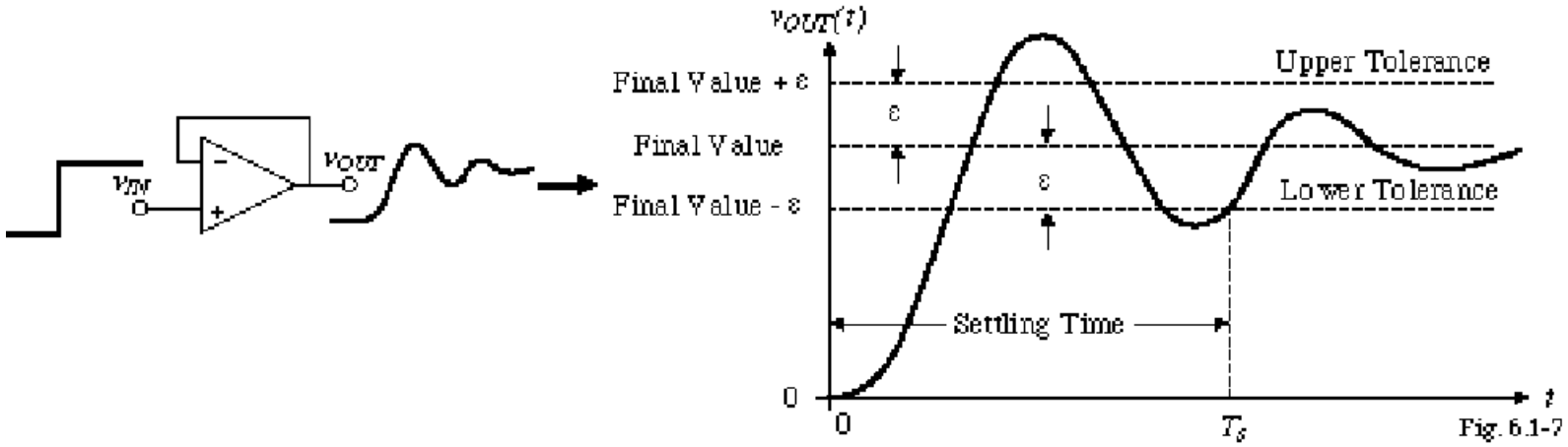

Fig. 6.1-7

EXAMPLE OF THE INFLUENCE OF *GB* AND SETTLING TIME ON DAC PERFORMANCE

Assume that a DAC uses a switched capacitor noninverting amplifier with $C_1 = C_2$ and GB = 1MHz. Find the conversion time of an 8-bit DAC if V_{REF} is 1V.

Solution

From the analysis in Secs. 9.2 and 9.3, we know that

$$w_H = \left(\frac{C_2}{C_1+C_2}\right) GB = (2\pi)(0.5)(10^6) = 3.141\text{x}10^6$$

and $A_{CL} = 1$. Assume that the ideal output is equal to V_{REF}. Therefore the value of the output voltage which is 0.5LSB of V_{REF} is

$$1 - \frac{1}{2^{N+1}} = 1 - e^{-w_H T}$$

or

$$2^{N+1} = e^{w_H T}$$

Solving for T gives

$$T = \left(\frac{N+1}{w_H}\right) ln(2) = 0.693 \left(\frac{N+1}{w_H}\right) = \left(\frac{9}{3.141}\right) 0.693 = 1.986ms$$

TESTING OF DACs

INPUT-OUTPUT TEST

Test setup:

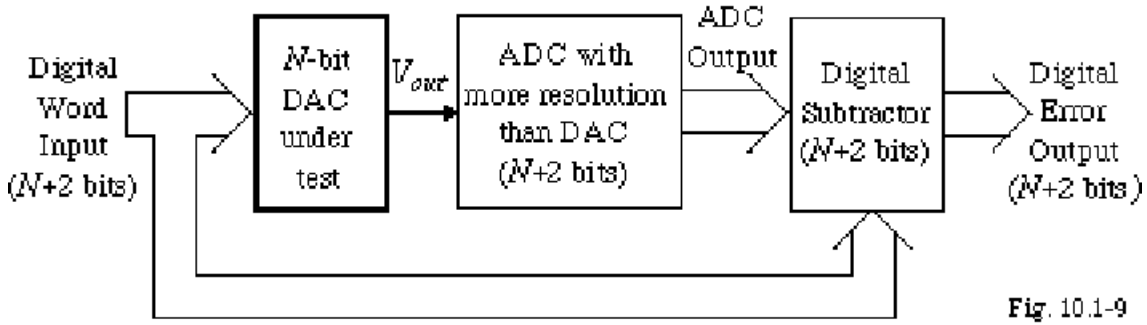

Fig. 10.1-9

Comments:

Sweep the digital input word from 000...0 to 111...1.

The ADC should have more resolution by at least 2 bits and be more accurate than the errors of the DAC

INL will show up in the output as the presence of 1's in any bit.

If there is a 1 in the Nth bit, the *INL* is greater than ±0.5*LSB*

DNL will show up as a change between each successive digital error output.

The bits which are greater than *N* in the digital error output can be used to resolve the errors to less than ±0.5*LSB*

SPECTRAL TEST

Test setup:

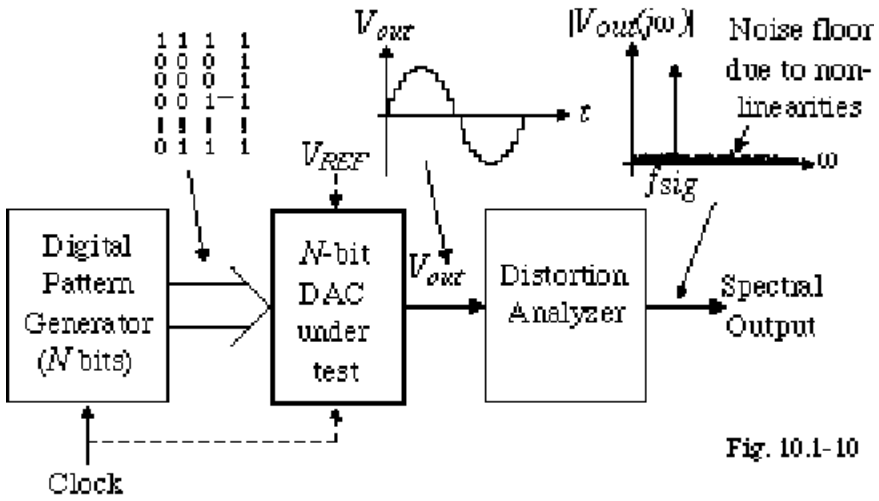

Fig. 10.1-10

Comments:

Digital input pattern is selected to have a fundamental frequency which has a magnitude of at least 6*N* dB above its harmonics.

Length of the digital sequence determines the spectral purity of the fundamental frequency.

All nonlinearities of the DAC (i.e. *INL* and *DNL*) will cause harmonics of the fundamental frequency

The THD can be used to determine the SNR dB range between the magnitude of the fundamental and the THD. This SNR should be at least 6*N* dB to have an *INL* of less than ±0.5*LSB* for an ENOB of *N*-bits.

Note that the noise contribution of V_{REF} must be less than the noise floor due to nonlinearities.

If the period of the digital pattern is increased, the frequency dependence of *INL* can be measured.