as they are maintained well below $-50$ dB up to 900 mV$_{\text{pp}}$ of the output voltage. As far as the odd components are concerned, the third one dominates up to 600 mV$_{\text{pp}}$, but their overall contribution is held to well below $-20$ dB, thus substantiating the high linearity of the proposed output stage which, of course, is greatly improved, embedding the circuit in a feedback operational amplifier.

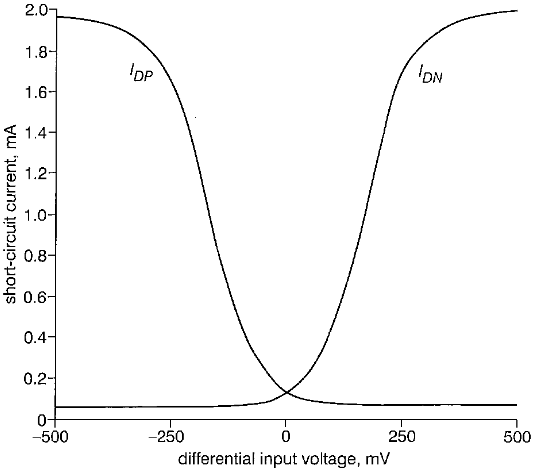

**Fig. 2** *Class AB behaviour: short circuit $I_{OP}$ and $I_{DN}$ against $v_d$*

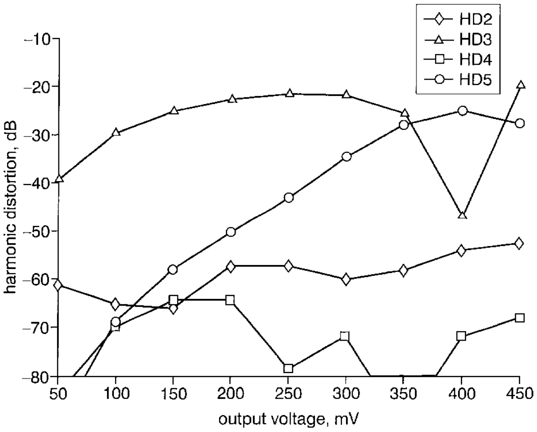

**Fig. 3** *Harmonic distortion components against output voltage amplitude*

© IEE 2002 *11 June 2002*
*Electronics Letters Online No: 20020927*
*DOI: 10.1049/el:20020927*

W. Aloisi, G. Giustolisi and G. Palumbo (*Dipartimento Elettrico Elettronico e Sistemistico, Università degli Studi di Catania, Viale Andrea Doria, 6, 95125 Catania, Italy*)

E-mail: ggiustolisi@dees.unict.it

## References

1 PALMISANO, G., PALUMBO, G., and SALERNO, R.: 'CMOS output stages for low-voltage power supplies', *IEEE Trans. Circuits Syst. II*, 2000, **47**, (2), pp. 96–104

2 PALMISANO, G., PALUMBO, G., and SALERNO, R.: 'A 1.5-V high drive capability CMOS op-amp', *IEEE J. Solid-State Circuits*, 1999, **34**, (2), pp. 248–252

3 PALUMBO, G.: '1.2 V CMOS output stage with improved drive capability', *Electron. Lett.*, 1999, **35**, (5), pp. 358–359

4 YOU, F., EMBABI, S.H.K., and SÁNCHEZ-SINENCIO, E.: 'Low-voltage class AB buffers with quiescent current control', *IEEE J. Solid-State Circuits*, 1998, **33**, (6), pp. 915–920

5 CAIULO, G., MALOBERTI, F., PALMISANO, G., and PORTALURI, S.: 'Video CMOS power buffer with extended linearity', *IEEE J. Solid-State Circuits*, 1993, **28**, (7), pp. 845–848

---

# Cancellation of load regulation in low drop-out regulators

R.K. Dokania and G.A. Rincón-Mora

A method for cancelling load regulation, based on level shifting the reference, is proposed. In this architecture, the load current is monitored, sensed, and used to dynamically adapt the effective value of the reference voltage. The proposed architecture reduced a 2.5% load regulation droop to a mere 0.2%, without compromising system stability.

*Introduction:* Modern state-of-the-art technologies require higher accuracy performance from voltage regulators. With load regulation performance being a significant factor, special attention is warranted in reducing its negative effects. In typical low drop-out (LDO) topologies, DC open-loop gain is severely restricted because of stringent stability requirements. Process variations in the output and the vast load current range of the circuit impose severe challenges on frequency compensation, thereby allowing only low-gain circuits to be reliably stable [1].

Load regulation is defined as the output voltage variation resulting from a unit load current change, which is equivalent to describing the output resistance of the regulator, as is clear from (1), given a simple feedback circuit as shown in Fig. 1:

$$R_{\text{load-reg}} = \frac{\Delta V_{\text{out}}}{\Delta I_{\text{load}}} = \frac{R_{\text{O-pass}}}{1 + A_{\text{OL}}\beta} \qquad (1)$$

or, equivalently,

$$V_{\text{out}} = V_{\text{ideal}} - I_{\text{load}} \cdot R_{\text{load-reg}} \qquad (2)$$

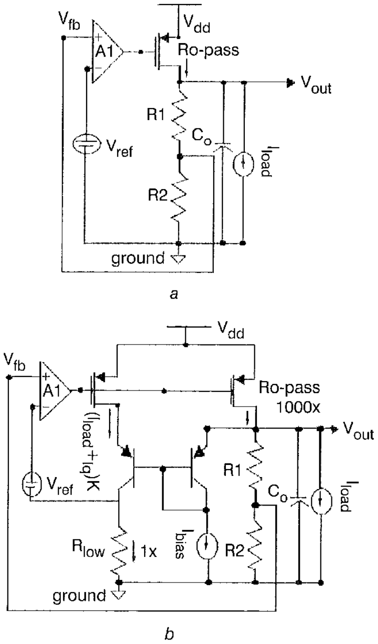

**Fig. 1** *Basic and proposed architecture*
*a* Basic
*b* Proposed

where resistor $R_{\text{O-pass}}$ is the output resistance of the pass device, $A_{\text{OL}}$ is the open-loop gain of the control circuit, and $\beta$ is the feedback factor. As shown, load regulation is inversely proportional to open-loop gain; but, as stated earlier, the gain cannot be high. The unity-gain frequency (UGF) is limited by the parasitic poles of the system and correspondingly restricts the bandwidth of the circuit. Load regulation performance, as a result, is fundamentally poor.

*Background:* A couple of techniques have been proposed to tackle the load regulation issue without excessively compromising stability.

The first technique directly alters the Bode-plot performance of the circuit, while the later two adaptively optimise either the open-loop gain or the pole placement in the buffer stage.

*Pole-zero generation:* In this technique, the DC open-loop gain is augmented by adding a pole-zero pair in the transfer function. For a given UGF, DC open-loop gain is increased by increasing the gain-drop rate in the frequency response, as is shown in trace (ii) of Fig. 2. In essence, the gain drops faster with increasing frequencies, thereby allowing larger DC gains with equal bandwidths. Consequently, regulation performance is improved while maintaining a stable condition. The design location of the added pole and zero determine the maximum DC open-loop gain possible, given output filter requirements. The circuit can be realised, generally, in one of several ways, two of which are by the use of parallel amplifiers [2] and by a feed-forward capacitor [3], as shown in Figs. 3*a* and *b*. The basic idea is to feed-forward the AC signal through a bypass path, constituted by either a low-gain amplifier or by a capacitor. The amplifier is unaffected by the feed-forward capacitor at low frequencies, and thus gives a high overall DC gain. At higher frequencies, the capacitor provides a parallel short circuit path, thereby giving rise to a lower high-frequency gain [3].

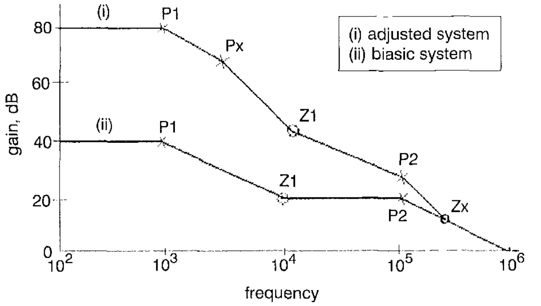

**Fig. 2** *Bode plot*

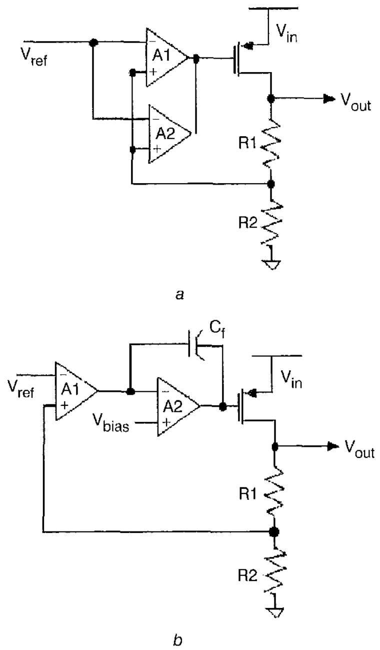

**Fig. 3** *Parallel amplifier and feed-forward capacitor*
*a* Parallel amplifier
*b* Feed-forward capacitor

*Load-adaptive techniques:* In typical LDO architectures, the frequency response itself varies with load current; thus, to have good phase-margin, even in worst-case conditions, some trade-offs between gain and stability are necessary. Dynamically adapting the open-loop gain with load current helps in having a better phase-margin and a higher overall open-loop DC gain. To ensure this, in this architecture the regulator uses a non-inverting, variable gain amplifier stage. In specific terms, the load current is sensed and used to modulate the output impedance of the second gain stage to keep the output pole beyond the UGF [4]. Thus, phase-margin performance is maximised, keeping the open-loop DC gain high and consequently load regulation effects low.

To similarly optimise the buffer, a load-dependent feedback signal may be used to modulate its conductance [5, 6]. As with the previous topology, the load current is sensed but a fraction of it is now fed back to a source-follower buffer stage. A positive feedback loop results but its gain is low and its signal is further attenuated with an RC filter, thereby not interfering with the negative feedback of the overall circuit [6].

*Proposed technique–floating reference LDO:* The techniques described above either alter the frequency response or directly change the circuit, thereby compromising system stability. Ideally, an enhancing technique should cancel any load regulation effects without altering the frequency response, or any other aspect, of the circuit, including parametric performance. The proposed circuit architecture does just that while enjoying the luxury of simplicity.

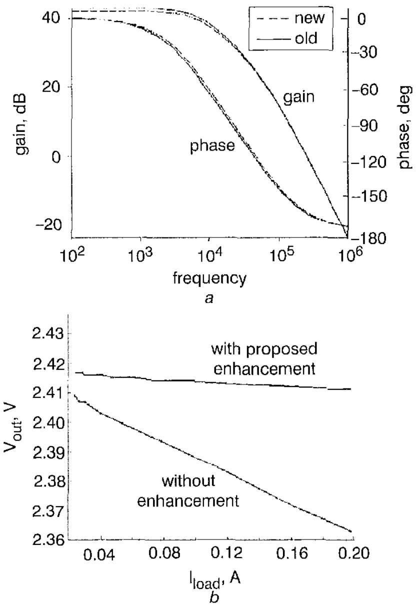

**Fig. 4** *Bode plot and load regulation*
*a* Bode plot
*b* Load regulation

As with the other techniques, the load current is sensed and fed back but it is only used to level-shift the reference in a benign fashion, as it relates to stability and circuit operation. Only the effective ground current of the control circuit is affected, (it increases), but that too at a significantly reduced rate. Simply inserting a resistor in its path, between ground and the reference, produces a voltage drop that increases linearly with the load current, exactly the opposite effect of load regulation. The mirroring of the current does not deteriorate current efficiency, as at zero-load current the mirrored current is also zero. Further, there is no change in the DC open-loop gain and hence the UGF is kept constant, thereby not compromising stability in the least. Overall, this topology is capable of completely cancelling all load regulation effects by appropriately choosing a resistor, as is clear from (3):

$$V_{out} = V_{ideal} - \left(\frac{R_{O\text{-pass}}}{1 + A_{OL}\beta} - \frac{R_{low}}{C}\right) \cdot I_{load} \qquad (3)$$

where $R_{low}$ is the resistance, through which, the mirrored current is passed to level shift the reference and $C$ is the factor by which the load current is reduced in the mirror (e.g. for $A_{OL} = 100$, $\beta = 1$, $R_{O\text{-pass}} = 10$, and $C = 1000$, $R_{low} = 100$ yields zero load regulation effects).

*Results:* The design was fabricated and tested with provisions to adjust resistor $R_{low}$. Near zero load regulation effects were observed; higher resolution of $R_{low}$ could have given still better results. As is obvious from the test results, shown in Fig. 4*b*, the proposed architecture reduced a 60 mV load regulation droop, which is prevalent in most widely stable LDO regulators, to a mere 5 mV, without sacrificing stability or affecting any other aspect of the circuit. That stability is intact is shown through simulations by the open-loop frequency response (Fig. 4*a*), phase and gain margin are unaffected by adding the resistor. With frequency response unchanged, the method is relatively easy to apply to most LDO topologies and, consequently, nearly cancels all load regulation effects.

*Conclusion:* From a design perspective, the proposed architecture is simple and benign, and effectively cancels all load regulation effects. Other topologies directly alter either the circuit and/or the gain and hence the frequency response, more than likely compromising stability. For optimal performance (complete cancellation), the value of $R_{low}$ can be easily trimmed during wafer testing, requiring only a few bits (e.g. three bits for roughly 3 to 4 mV resolution) [7].

*12 July 2002*
*Electronics Letters Online No: 20020909*
*DOI: 10.1049/el:20020909*

R.K. Dokania and G.A. Rincón-Mora (*Georgia Tech Analog Consortium, School of Computer and Electrical Engineering, Georgia Institute of Technology, 777 Atlantic Drive, Atlanta, Georgia 30332-0250, USA*)

E-mail: r_dokania@yahoo.com

**References**

1 GOODENOUGH, F.: 'Low dropout linear regulators', *Electron. Des.*, 1996, pp. 65–77
2 RINCÓN-MORA, G.A.: 'Optimized frequency shaping circuit topologies for LDOs', US Patent 5,982,226, November 1999
3 RINCÓN-MORA, G.A., and ALLEN, P.E.: 'Optimized frequency shaping circuit topologies for LDOs', *IEEE Trans. Circuits Syst II*, 1998, **45**, (6), pp. 703–708
4 XI, X.: 'PMOS low drop-out voltage regulator using non-inverting variable gain stage', US Patent 6,246,221, September 2000
5 RINCÓN-MORA, G.A., and ALLEN, P.E.: 'A low voltage, low quiescent current, low drop-out regulator', *IEEE J. Solid-State Circuits*, 1998, **33**, (1), pp. 36–44
6 RINCÓN-MORA, G.A.: 'Low-dropout voltage regulator incorporating a current efficient transient response boost circuit', US Patent 6,046,577, April 2000
7 RINCÓN-MORA, G.A.: 'Voltage reference – from diodes to precision high-order bandgap circuits', (IEEE Press, Wiley Interscience, 2002), pp. 126–130

---

# Class D audio power amplifier with fine hysteresis control

Sang-Hwa Jung, Nam-In Kim and Gyu-Hyeong Cho

A new simple and efficient control method for a class D audio power amplifier is presented. The new fine hysteresis control method can control the switching frequency freely and guarantees stability for any load condition without having any outside compensation circuit at all.

*Introduction:* In recent years, digital switching power amplifiers have gained growing attention in the field of audio applications. The switching power technology provides a high-efficiency and low-volume alternative for audio power amplifications but suffers from low signal-to-noise ratio due to inherent nonlinearity and crossover distortion. Efforts have been made to overcome these problems [1–3]. A novel solution is presented in this Letter based on a new simple and practically useful fine hysteresis control method.

Hysteresis control (Bang-Bang) is one of the well-known techniques used in DC-DC converters. It is popular and widely used because of its simplicity and absolute stability. Conventional hysteresis control converters, however, produce rough output voltages due to high ripple current in the inductor caused by low switching frequency and sub-harmonic oscillation [4]. The response time from the drain voltage ($V_{drain}$) of the main switch to the converter output voltage ($V_{out}$) is also very slow because the voltage information is used only to regulate the output voltage. As a result, the switching frequency is low and consequently the ripple current and conduction loss are high in the conventional hysteresis control converters. Conversely, in the pulse-width modulation (PWM) control method, the switching frequency is easily adjustable and thus the ripple voltage at the output as well as the ripple current in the inductor can be made to be low by increasing the switching frequency [2]. However, a complex compensation circuit around the error amplifier depending on the load and filter conditions is a serious shortcoming in the PWM converters.

In this Letter, a new control method called fine hysteresis control (FHC) is presented for a high performance class D audio power amplifier. FHC is capable of maintaining excellent stability for any load and/or filter conditions. It allows the switching frequency to be set at a high value. All these are possible using a very simple structure.

*Inductor current sensing method:* To increase the switching frequency in the hysteresis control, the inductor current information needs to be included in the feedback loop. For this purpose, the output voltage $V_{out}$ and a switching ripple current of the inductor are added together at the $V_{sense}$ node as shown in Fig. 1.

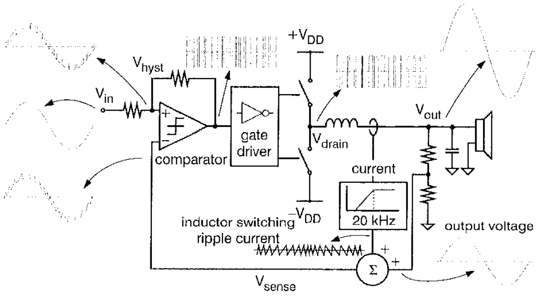

**Fig. 1** *Basic block diagram of FHC class D audio amplifier*

If it is only the ripple current information caused by switching that is important, it is possible to obtain it by integrating the voltage across the inductor using an RC integrator ($R_{S1}$, $R_{S2}$ and $C_{int}$) as shown in Fig. 2. This method is useful only when the information about the switching ripple current shape is required instead of its exact value. As a result, the node voltage $V_{sense}$ becomes the sum of the output voltage divided by $R_{S1}$ and $R_{S2}$ and the switching ripple current component ($V_C$) of the inductor.

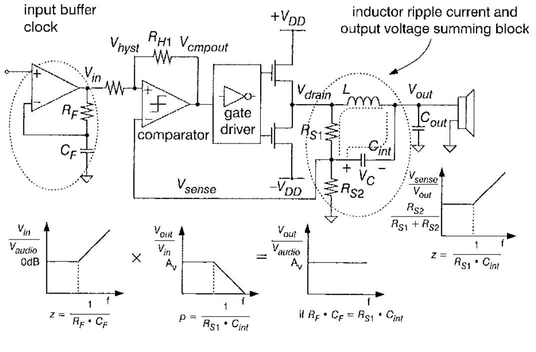

**Fig. 2** *Implemented circuit*

*Overall operation and switching frequency:* The node voltage $V_{sense}$ is applied to the negative input of the comparator having a hysteresis by $R_{H1}$ and $R_{H2}$ to the plus input as shown in Fig. 2. By comparison,