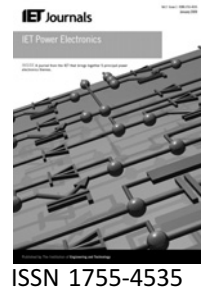


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# Limits of predictive current-ripple suppression in switching power-supply ICs

L.A. Milner G.A. Rincón-Mora

Georgia Tech Analog, Power, and Energy IC Research, School of Electrical and Computer Engineering, Georgia Institute of Technology, 777 Atlantic Drive, Atlanta, GA 30332-0250, USA  
 E-mail: lamilner@ece.gatech.edu

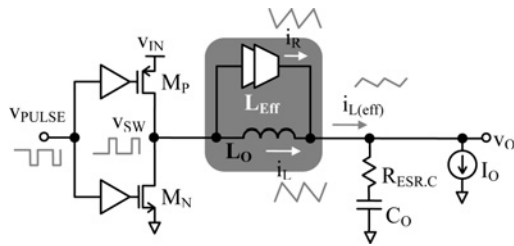
**Abstract:** Large inductance requirements (for accuracy) in switching power supplies for portable applications impede system-on-chip (SoC) integration and therefore form-factor reduction because on-chip inductances are invariably low and off-chip inductors intolerably obtrusive. Cancelling the current ripple of innately small on-chip inductors, however, keeps the effective output current ripple and its resulting output voltage variation (i.e. accuracy) within acceptable window limits (e.g. 50–200 mA and 20–50 mV), effectively multiplying the on-chip inductance and circumventing the need for bulky off-chip inductors. To this end, while gyrators and other voltage-mode inductor multiplier circuitry simulate relatively high inductances, they cannot supply the 250–750 mW loads typically attached to battery-powered switching regulators, which the predictive current-mode multipliers discussed in this paper can. The basic objective is to cancel the ac inductor current ripple with an inverting ac replica and allow the on-chip inductor to source the full dc load. Ac mismatches in the form of amplitude, delay and non-linearity, however, limit the extent to which the original ac ripple is cancelled, constraining the inductor multiplication factor to finite values. The foregoing paper describes, illustrates and derives the effects of these mismatches on the multiplication factor and shows how realistic non-idealities (e.g. up to 10% gain error and less than 10 ns of delay) can yield inductance multiplication factors of 125 H/H at 100 kHz and 11.5 H/H at 10 MHz in a practical switching dc–dc power-supply integrated circuit (IC).

## 1 Inductor multiplication

Switching dc–dc supplies are bulky, yet essential fixtures in portable and stationary microelectronic applications. The fact is state-of-the-art dc–dc converters used to drive processors, backlights, power amplifiers (PAs) and the like, require discrete off-chip power inductors. The magnetic-based buck converter shown in Fig. 1, for example, converts a 2.7–4.2 V Li-ion voltage (i.e.  $V_{IN}$ ) into a steady 1.2 V supply (i.e.  $v_O$ ) by modulating how often transistor  $M_P$  connects switching node  $v_{SW}$  to  $V_{IN}$ ; in other words, because inductor  $L$  is a short circuit at dc, the average value of  $v_{SW}$  equates to the average value of  $v_O$

$$v_{O(\text{avg})} \equiv V_O = v_{SW(\text{avg})} = V_{IN}d_{MP} \quad (1)$$

where  $V_O$  is the average value of  $v_O$  and  $d_{MP}$  the duty cycle of  $M_P$ . The switching action of  $v_{SW}$ , however, causes the voltage across the inductor to alternate between  $V_{IN}-v_O$  and  $-v_O$  and its current  $i_L$  to rise and fall as a result. The rippling current (ac component) ultimately flows into output capacitor  $C_O$  and produces an ac voltage at the output. This ac ripple voltage, which constitutes accuracy degradation, is inversely proportional to inductance  $L_O$ , which is why large off-chip inductors are typically used. Although on-chip inductors with plated ferromagnetic layers are promising [1–4], state-of-the-art on-chip inductances are prohibitively low, on the order of 20–100 nH, and increasing the number of turns increases the ohmic losses across its increased equivalent series resistance (ESR) while using cores with higher permeability decreases the onset of saturation conditions. Note  $M_N$  conducts



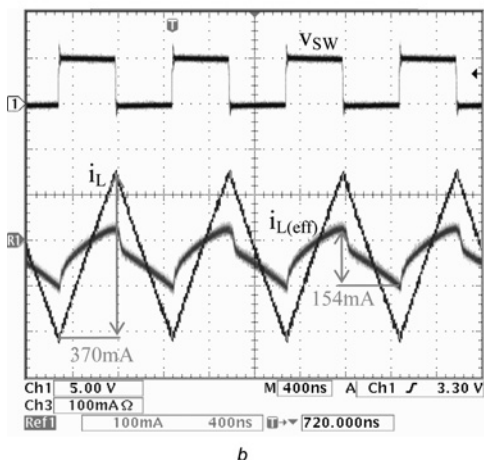
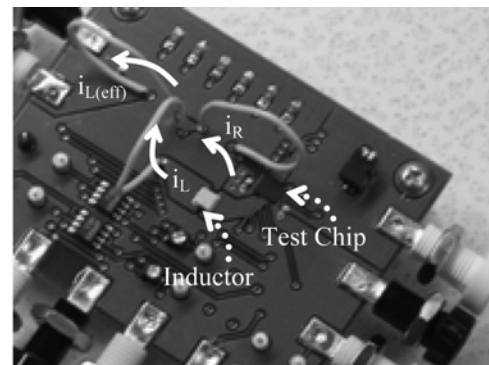
**Figure 1** Current-mode inductor multiplication in a buck switching dc–dc supply circuit

whenever  $M_P$  does not, which means  $M_N$ 's duty cycle complements  $d_{MP}$  and is equal to  $1 - d_{MP}$ , or by convention,  $d'_{MP}$ .

The ‘linear-assisted converters’ in [5, 6], ‘gyrators’ in [7, 8], ‘active filters’ in [9–11] and ‘inductor multipliers’ in [12, 13] attenuate the ac ripple current driven into  $C_O$  by subtracting a circuit-derived complementary ripple replica current  $i_R$  from on-chip inductor current  $i_L$  (Fig. 1), the difference of which constitutes a smaller effective ripple current (i.e.  $i_{L(eff)}$ ) that produces less voltage variations in  $v_O$  (i.e. across  $C_O$ ). If  $i_R$  were an exact inverting replica of the ac component of  $i_L$ ,  $i_{L(eff)}$  would carry no ac component to drive into  $C_O$  and  $v_O$  would consequently be free of ripple. Because a larger inductor induces lower ripple currents, the circuit generating  $i_R$  is said to be an inductor multiplier, and since an infinitely large inductor produces no ripple, an exact inverting copy yields infinite inductor gain (i.e. infinitely high inductor multiplication factor). Note increasing switching frequency also reduces the ripple current, but additional passives and burst-mode operation are required to implement the resonant topologies that mitigate the increased switching losses, and so reductions in the physical area and voltage ripple are never fully realised. The fact is increasing the switching frequency enough for on-chip inductors to be viable can be impractical in some applications (e.g. when restricted to low-voltage process technology) and might negate the efficiency advantage switching regulators have over their linear counterparts [14, 15], which are considerably easier and less costly to integrate. Inductor multipliers present their own challenges and also heavily impact converter efficiency, but an integrated prototype has been developed that demonstrates current-ripple suppression of more than an order of magnitude and also compares favourably with other strategies in terms of efficiency.

Given the systematic nature of inductor current  $i_L$  – it rises and falls on cue and in proportion to  $V_{IN}$  and  $V_O$  – both [10, 13] predict (rather than sense) and reproduce the ac component of  $i_L$  via inverting replica  $i_R$ . The basic idea is that integrating the voltage across  $L_O$  with a capacitor produces an ac triangular voltage that is analogous to  $i_L$  so converting this ripple voltage into a current with an inverting transconductor yields  $i_R$ . Unfortunately, neither the transconductance nor the capacitance track  $L_O$  so  $i_R$  is

not entirely accurate, plus  $i_R$  lags  $i_L$  (in time) and finite resistances across the integrating capacitor distort the otherwise triangular voltage. Irrespective of the scheme, however, errors in amplitude, delay and linearity such as these change the ultimate amplitude and shape of the current driven into  $C_O$  (i.e.  $i_{L(eff)}$ ), limiting the efficacy of the multiplying circuit in switching regulator applications (i.e. the amount by which the effective inductance appears larger). For example, the amplitude of  $i_{L(eff)}$  is still almost half of  $i_L$  in one experiment with the integrated prototype inductor multiplier shown in Fig. 2a, and as shown in Fig. 2b, its waveform is not triangular. (Although the copper wires added to capture these waveforms with a current probe introduced several nanohenries to the circuit,  $L_O$  was 4.7  $\mu$ H so the parasitic effects of the wires were negligible, and considering the wires were only included for the sake of the measurement, their effects do not apply to practical applications, even when using small on-chip inductors.) The ripple suppression in this example is limited because  $i_R$  (which is not shown) is only 260 mA<sub>pp</sub> and delayed by 35 ns relative to  $i_L$ . While literature of multiphase converters, such as [16, 17], analyse the cancellation effect of complementary current ripples with respect to amplitude errors, delay and non-linearity effects because of finite time constants, either of which can



**Figure 2** Prototyped inductor multiplier IC

- a Assembled test board
- b Experimental waveforms

dominate the cancellation factor and both of which are inherent in any active-circuit technique, remain largely unexplored. This paper describes, illustrates and derives the individual (Section 2) and combined (Section 3) effects of non-idealities such as these on a switching power supply circuit (Section 4), drawing and discussing relevant conclusions (Section 5).

*Note 1:* Since analysing these errors by comparing the ac portions of  $i_R$  to  $i_L$  only (and ignoring their dc components) is easier, to help delineate one from the other, the following sections use all lowercase variables (e.g.  $i_r$  and  $i_l$ ) for ac signals only, all uppercase variables (e.g.,  $I_R$  and  $I_L$ ) for dc and lowercase–uppercase combinations (e.g.,  $i_R$  and  $i_L$ ) for both ac and dc. Notice, nevertheless, that removing the dc component does not affect the peak-to-peak magnitude of a signal, which means, for example,  $\Delta i_{l(\text{eff})}$  equals (by definition)  $\Delta i_{L(\text{eff})}$  even if  $i_{l(\text{eff})}$  differs from  $i_{L(\text{eff})}$  by a dc value.

*Note 2:* A ripple in  $v_O$  constitutes a ripple voltage across  $L_O$ , which causes variations in  $i_L$ . The extent to which the ripple in  $v_O$  affects  $i_L$ 's large-signal response depends on its percent variation, which in the case of state-of-the-art dc–dc converters is on the order of 5–10 mV/V, in other words, at most 1% of  $V_{O\text{UT}}$ . In deriving  $i_L$ , as a result, assuming  $v_O$  reduces to its dc value of  $V_O$  produces errors well below 1%. Neglecting this error in the foregoing analysis is therefore reasonable (and practical) because other errors, as results will show, swamp its effects, ultimately yielding sufficiently accurate and insightful expressions from which to draw meaningful design-oriented conclusions. Incidentally, lower ripples, which result from higher multiplication factors, reduce the impact of this error. Nevertheless, for validation and accuracy, all simulation results in this paper include this error (i.e. the effects of a ripple in  $v_O$ ) so the graphs and tables shown are accurate, proving the validity of this assumption.

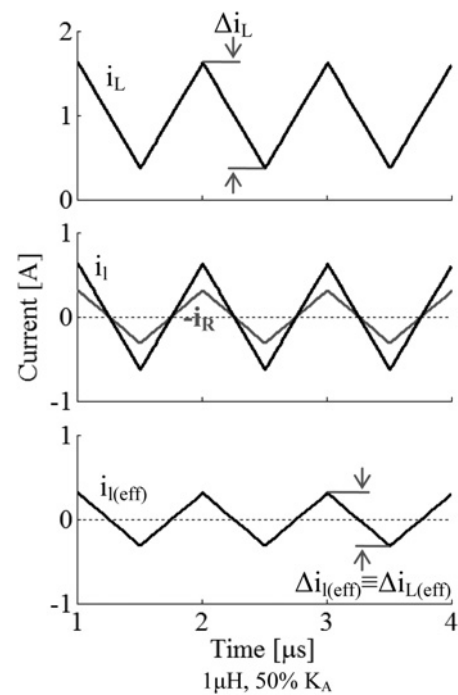
## 2 Individual errors

### 2.1 Linear (amplitude) error

The first error to consider is a variation in amplitude when the peak-to-peak value of inverting replica current  $i_R$  differs from that of the ac component in inductor current  $i_L$  (i.e.  $i_l$ ), as depicted in Fig. 3. This error has been acknowledged before in the context of multiphase converters [16], in which the ripple currents through two or more inductors are meant to cancel each other. With a linear error of this sort, the effective ripple current driven into  $C_O$  (i.e.  $i_{l(\text{eff})}$ ), which is the sum of  $i_l$  and  $i_R$ , retains a triangular shape but with smaller amplitude

$$\Delta i_{L(\text{eff})} = \Delta i_L + \Delta i_R = \Delta i_L - \Delta i_L(1 - K_A) = K_A \Delta i_L \quad (2)$$

where  $K_A$  is the fractional amplitude-error coefficient, which can be positive or negative. Because the ultimate metric in a



**Figure 3** Spice simulation results showing the effect of amplitude error  $K_A$  in replica current  $i_R$  on output ripple current  $i_{l(\text{eff})}$

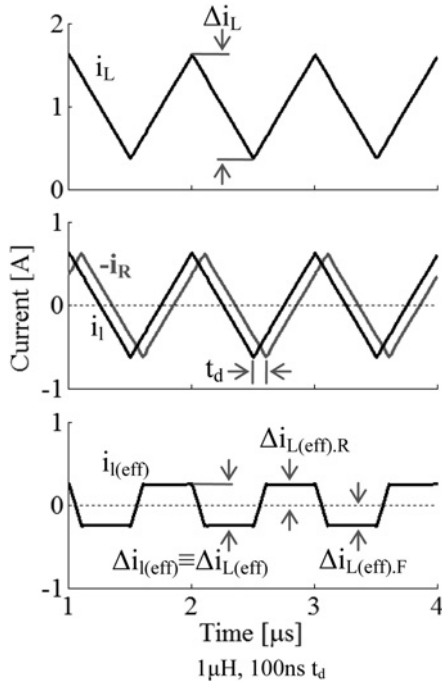
switching power supply is its peak-to-peak output ripple voltage, the inductor multiplication factor amounts to the peak-to-peak ratio of  $\Delta i_L$  to  $\Delta i_{L(\text{eff})}$ , which in this case is the reciprocal of  $K_A$

$$M_{L,A} \equiv \frac{L_{\text{Eff}}}{L_O} \equiv \frac{\Delta i_L}{\Delta i_{L(\text{eff})}} = \frac{1}{K_A} \quad (3)$$

or equivalently, by definition, the ratio of equivalent inductance  $L_{\text{Eff}}$  that would have produced  $i_{L(\text{eff})}$  and on-chip inductance  $L_O$ , where  $M_{L,A}$  is the multiplication factor when only an error in amplitude exists.

### 2.2 Delay (timing) error

A delay error in inverting replica current  $i_R$  with respect to  $i_L$  is more problematic because its effect on effective output current  $\Delta i_{L(\text{eff})}$  is to substantially increase its ac ripple, especially under high  $di_L/dt$  conditions, when the voltage across the inductor is relatively large, and with increasing switching frequencies, as delay  $t_d$  becomes a larger fraction of switching period  $T_{\text{SW}}$ . Fig. 4 illustrates a replica current  $i_R$  that, other than being delayed by  $t_d$ , is perfectly matched to the ac portion of  $i_L$ . The effect of the delay on  $i_{L(\text{eff})}$  when  $i_L$  and  $-i_R$  both rise (or fall) is a constant difference  $\Delta i_{L(\text{eff})\text{.R}}$  (or  $\Delta i_{L(\text{eff})\text{.F}}$ ). During the times  $i_L$  rises and  $-i_R$  falls, and vice versa,  $i_{L(\text{eff})}$  rises and falls linearly to and from peak values  $\Delta i_{L(\text{eff})\text{.R}}$  and  $-\Delta i_{L(\text{eff})\text{.F}}$ , the net result of which is a trapezoidal ac current into output capacitor  $C_O$ , as shown in Fig. 4. The trapezoidal shape is an unfortunate result in so far as it complicates control of a switching



**Figure 4** Spice simulation results showing the effect of delay error  $t_d$  in replica current  $i_R$  on output ripple current  $i_{L(eff)}$

regulator. Since this shape is a result of delay, which cannot be completely eliminated in any active filter, it will always be a feature of  $i_{L(eff)}$  that may in some cases dominate other errors, so it must be characterised.

Rising difference  $\Delta i_{L(eff).R}$  is the product of rising rate  $di_L^+/dt$  and delay  $t_d$ , which is inversely proportional to  $L_O$  and directly proportional to the voltage across  $L_O$  when switch  $M_P$  conducts, that is,  $V_{IN} - v_O$ , or equivalently,  $V_{IN}(1 - d_{MP})$  or  $V_{IN}d'_{MP}$

$$\begin{aligned} \Delta i_{L(eff).R} &= \left(\frac{di_L^+}{dt}\right)t_d = \left(\frac{V_{IN} - v_O}{L_O}\right)t_d \\ &= \left[\frac{V_{IN}(1 - d_{MP})}{L_O}\right]t_d = \left(\frac{V_{IN}d'_{MP}}{L_O}\right)t_d \end{aligned} \quad (4)$$

Similarly, falling difference  $\Delta i_{L(eff).F}$  is the product of  $di_L^-/dt$  and  $t_d$  and inversely proportional to  $L_O$  and directly proportional to  $v_O$ , or  $V_{IN}d_{MP}$

$$\Delta i_{L(eff).F} = \left(\frac{di_L^-}{dt}\right)t_d = \left(\frac{v_O}{L_O}\right)t_d = \left[\frac{V_{IN}d_{MP}}{L_O}\right]t_d \quad (5)$$

The total ac peak-to-peak current in  $i_{L(eff)}$  is the sum of the aforementioned rising and falling difference currents (i.e.  $\Delta i_{L(eff)} = \Delta i_{L(eff).R} + \Delta i_{L(eff).F}$ ) whereas the peak-to-peak current in  $i_L$  (i.e.  $\Delta i_L$ ) is the product of rising rate  $di_L^+/dt$  and  $M_P$ 's on time, the latter of which is the product of

switching period  $T_{SW}$  and  $d_{MP}$  (i.e.  $t_{on}/T_{SW}$ )

$$\begin{aligned} \Delta i_L &= \left(\frac{di_L^+}{dt}\right)d_{MP}T_{SW} = \left(\frac{V_{IN} - v_O}{L_O}\right)\frac{d_{MP}}{f_{SW}} \\ &= \left[\frac{Ve(1 - d_{MP})}{L_O}\right]\frac{d_{MP}}{f_{SW}} = \frac{V_{IN}d'_{MP}d_{MP}}{L_O f_{SW}} \end{aligned} \quad (6)$$

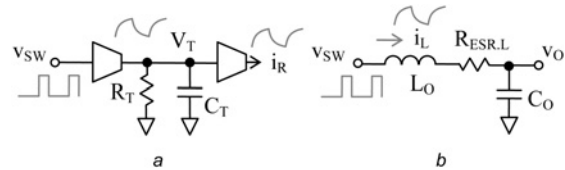
where  $f_{SW}$  is the switching frequency  $1/T_{SW}$ . As before, within the context of switching power supplies, the effective inductor multiplication factor is the ratio of  $\Delta i_{L(eff)}$  and  $\Delta i_L$ , which in the presence of a delay yields a factor that is directly proportional to  $d_{MP}d'_{MP}$  and inversely proportional to  $t_d$  and  $f_{SW}$ , or inversely proportional to the percentage of time  $t_d$  is with respect to  $T_{SW}$

$$\begin{aligned} M_{I.D} &\equiv \frac{L_{eff}}{L_O} \equiv \frac{\Delta i_L}{\Delta i_{L(eff)}} = \frac{\Delta i_L}{\Delta i_{L(eff).R} + \Delta i_{L(eff).F}} \\ &= \frac{d_{MP}d'_{MP}}{t_d f_{SW}} = d_{MP}d'_{MP} \left(\frac{T_{SW}}{t_d}\right) \end{aligned} \quad (7)$$

where  $M_{I.D}$  is the effective inductor multiplication factor in the presence of a delay. Note that, unlike an amplitude mismatch, a delay error changes the shape of  $\Delta i_{L(eff)}$  to trapezoidal and its impact is worse under higher switching frequencies.

### 2.3 Non-linear error

Non-linearities in replica current  $i_R$  constitute another error source (as amplitude and delay errors are linear effects). These non-linear errors result from non-idealities in the circuit, such as the exponential response of RC poles in the signal path. For instance, driving and sinking a constant square current into and from a capacitor produces a triangular voltage, which when multiplied by a transconductor generates the triangular current desired in  $i_R$ . However, considering current levels are low to decrease quiescent power losses and therefore extend battery life, the presence of a parasitic resistance across the aforementioned filter capacitor, as shown in Fig. 5a, distorts the otherwise linear response with higher order components (i.e. the exponential RC time-constant response produces non-linearities in  $i_R$ ). Note the equivalent series resistance ( $R_{ESRL}$ ) of  $L_O$  in the power stage of a switching supply (Fig. 5b) also produces similar effects in  $i_L$ , except  $L_O$  and



**Figure 5** The non-linear effects

a Parasitic filter resistor in the replica-current circuit on replica current  $i_R$   
b Inductor's equivalent series resistance  $R_{ESRL}$  in the power stage of a switching buck regulator on inductor current  $i_L$

$R_{ESR,L}$  are typically large and small enough, respectively, to produce unobservable non-linear effects in  $i_L$ .

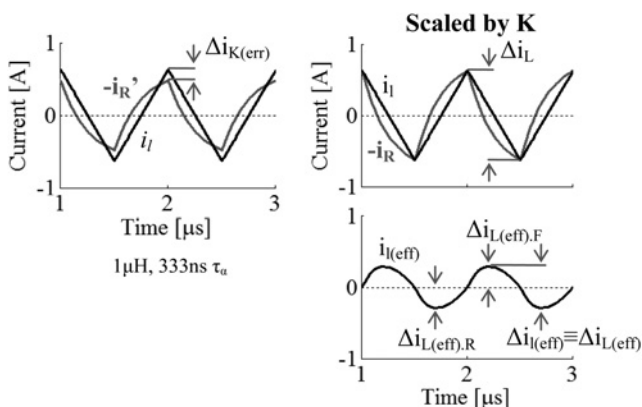
A second-order polynomial with respect to time approximates the effects of the exponential relationship in  $i_R$  and  $i_L$  reasonably well while simultaneously simplifying the math. The fact is the coefficient of the second-order term of an exponential is considerably larger than those of higher order components, as seen from its Taylor-series expansion

$$e^{At} = e^{At}|_{t=0} + \left(\frac{1}{1!}\frac{d^1(e^{At})}{dt^1}\right)|_{t=0} \times t + \dots + \left(\frac{1}{n!}\frac{d^n(e^{At})}{dt^n}\right)|_{t=0} t^n$$

$$= 1 + At + \left(\frac{A^2}{2}\right)t^2 + \left(\frac{A^3}{6}\right)t^3 + \dots + \left(\frac{A^n}{n!}\right)t^n \quad (8)$$

where second-order coefficient  $A^2/2$  is greater than the third and all others. (Amplitude and delay errors already account for errors in linear term  $At$ .) Fig. 6 shows how this simplifying assumption preserves the general characteristics of the nonlinearity shown in Fig. 5. Adding the second-order term, however, also affects the amplitude of the signal, which was already addressed in the analysis of fractional amplitude-error coefficient  $K_A$ . As a result, scaling factor  $K$  is used to normalise the otherwise amplitude-affected replica current  $i'_R$  (shown as its inverse  $-i'_R$  in Fig. 6 to appreciate how it relates to  $i_L$ ) into  $-i_R$  to decouple non-linear effects from amplitude and delay errors.

To understand the impact of non-linearity on  $i_{l(eff)}$ , it is helpful to first recall that the rising and falling inductor current is a function of the rising and falling rates of  $i_L$  when subjecting  $L_O$  to on- and off-time voltages of



**Figure 6** Spice simulations showing the effect of non-linearity in replica current  $i_R$  on output ripple current  $i_{L(eff)}$

$V_{IN}-v_O$  and  $-v_O$ , respectively, as  $M_P$  switches on and off

$$i_{l,R} = \left(\frac{di_L^+}{dt}\right)t = \left(\frac{V_{IN} - v_O}{L_O}\right)t = \left(\frac{V_{IN}d'_{MP}}{L_O}\right)t \equiv m_R t \quad (9)$$

and

$$i_{l,F} = \left(\frac{di_L^-}{dt}\right)t = \left(\frac{-v_O}{L_O}\right)t = \left(\frac{-V_{IN}d'_{MP}}{L_O}\right)t$$

$$= \left(\frac{-m_R d'_{MP}}{d'_{MP}}\right)t \equiv -m_F t \quad (10)$$

where the effects of parasitic resistor  $R_{ESR,L}$  are negligible and  $m_R$  and  $m_F$  are the linear rising and falling coefficients of  $i_l$ . Inverting replica current  $-i_R$  must therefore include scaling factor  $K$  and the aforementioned linear rising and falling coefficients to retain the amplitude and first-order term of  $i_L$  while succumbing to the effects of rising and falling non-linear terms  $\alpha_R$  and  $\alpha_F$

$$-i_{R,R} = K(m_R t - \alpha_R t^2) \quad (11)$$

and

$$-i_{R,F} = K(-m_F t + \alpha_F t^2) \quad (12)$$

where  $K$ , by definition, is the constant that equates the amplitudes of  $i_l$  and  $-i_R$  (i.e.  $i_{l,R}$  and  $-i_{R,R}$  at time  $t_{on}$  and  $i_{l,F}$  and  $-i_{R,F}$  at  $t_{off}$ )

$$i_{l,R}|_{t_{on}} = m_R t_{on} \equiv -i_{R,R}|_{t_{on}} = K(m_R t_{on} - \alpha_R t_{on}^2) \quad (13)$$

or

$$K = \frac{m_R}{m_R - \alpha_R t_{on}} \quad (14)$$

which, for the purpose of this discussion, is a constant. The sign of non-linear terms  $\alpha_R$  and  $\alpha_F$  is consistent with exponential distortion in  $i_R$  (Fig. 6).

As before, the effective inductor multiplication factor, as it relates to switching converters, is the ratio of the peak-to-peak values of  $i_L$  and  $i_{L(eff)}$ . Effective output ripple ac current  $i_{l(eff)}$  is the sum of  $i_l$  and  $i_R$  (or the difference between  $i_l$  and  $-i_R$ ) so rising and falling  $i_{l(eff)}$  with a non-linear error amount to

$$i_{l(eff),R} = i_{l,R} + i_{R,R} = m_R t - K(m_R t - \alpha_R t^2)$$

$$= m_R(1 - K)t + K\alpha_R t^2 \quad (15)$$

and

$$\begin{aligned} i_{l(\text{eff})\text{.F}} &= i_{l\text{.F}} + i_{r\text{.F}} = -m_{\text{F}}t - K(-m_{\text{F}}t + \alpha_{\text{F}}t^2) \\ &= -m_{\text{F}}(1 - K)t - K\alpha_{\text{F}}t^2 \end{aligned} \quad (16)$$

The polarity of the second-order (i.e. squared) term indicates  $i_{l(\text{eff})}$  is concave and larger than  $i_{l\text{.R}}$  during  $M_{\text{P}}$ 's on time (i.e. rising portion of  $i_{l\text{.L}}$ ) and convex and smaller than  $i_{l\text{.F}}$  during  $M_{\text{P}}$ 's off time (i.e. falling part of  $i_{l\text{.L}}$ ), as seen in Fig. 6. Unlike the amplitude and delay errors, however, the maximum error (i.e.  $\Delta i_{l(\text{eff})}$ ) does not occur at transitional points  $t_{\text{on}}$  or  $t_{\text{off}}$ . Differentiating  $i_{l(\text{eff})\text{.R}}$  and  $i_{l(\text{eff})\text{.F}}$  and equating to zero reveals the maximum error occurs half-way through  $t_{\text{on}}$  and  $t_{\text{off}}$

$$\left. \frac{di_{l(\text{eff})\text{.R}}}{dt} \right|_{t=0.5t_{\text{on}}} = 0 \quad (17)$$

and

$$\left. \frac{di_{l(\text{eff})\text{.F}}}{dt} \right|_{t=0.5t_{\text{off}}} = 0 \quad (18)$$

which means the amplitude of  $i_{l(\text{eff})}$  is

$$\begin{aligned} \Delta i_{l(\text{eff})} &\equiv \Delta i_{l(\text{eff})\text{.R}} + \Delta i_{l(\text{eff})\text{.F}} = -i_{l(\text{eff})\text{.R}|0.5t_{\text{on}}} + i_{l(\text{eff})\text{.F}|0.5t_{\text{off}}} \\ &= -m_{\text{R}}(1 - K)\left(\frac{t_{\text{on}}}{2}\right) - K\alpha_{\text{R}}\left(\frac{t_{\text{on}}}{2}\right)^2 \\ &\quad - m_{\text{F}}(1 - K)\left(\frac{t_{\text{off}}}{2}\right) - K\alpha_{\text{F}}\left(\frac{t_{\text{off}}}{2}\right)^2 \end{aligned} \quad (19)$$

Similar to how  $d_{\text{MP}}/d'_{\text{MP}}$  relates  $m_{\text{R}}$  and  $m_{\text{F}}$  (i.e.  $m_{\text{F}}$  is  $m_{\text{R}}d_{\text{MP}}/d'_{\text{MP}}$ ),  $t_{\text{on}}$  and  $t_{\text{off}}$  correlate (with respect to switching period  $T_{\text{SW}}$ )

$$\begin{aligned} t_{\text{on}} &= d_{\text{MP}}T_{\text{SW}} = d_{\text{MP}}T_{\text{SW}}\left(\frac{d'_{\text{MP}}}{d_{\text{MP}}}\right) = d'_{\text{MP}}T_{\text{SW}}\left(\frac{d_{\text{MP}}}{d'_{\text{MP}}}\right) \\ &= t_{\text{off}}\left(\frac{d_{\text{MP}}}{d'_{\text{MP}}}\right) \end{aligned} \quad (20)$$

Additionally, for equilibrium and steady-state conditions, the ripple must rise as much as it falls every period, which means  $i_{r\text{.R}}$  at  $t_{\text{on}}$  must equate to  $-i_{r\text{.F}}$  at  $t_{\text{off}}$  and second-order coefficients  $\alpha_{\text{R}}$  and  $\alpha_{\text{F}}$  consequently also relate through the ratio of  $d'_{\text{MP}}$  and  $d_{\text{MP}}$

$$\begin{aligned} i_{r\text{.R}}|_{t_{\text{on}}} &= K(m_{\text{R}}t_{\text{on}} - \alpha_{\text{R}}t_{\text{on}}^2) \equiv -i_{r\text{.F}}|_{t_{\text{off}}} \\ &= -K(-m_{\text{F}}t_{\text{off}} + \alpha_{\text{F}}t_{\text{off}}^2) \\ &= K\left(m_{\text{R}}\left(\frac{d_{\text{MP}}}{d'_{\text{MP}}}\right)t_{\text{on}}\left(\frac{d'_{\text{MP}}}{d_{\text{MP}}}\right) - \alpha_{\text{F}}t_{\text{on}}^2\left(\frac{d'_{\text{MP}}}{d_{\text{MP}}}\right)^2\right) \end{aligned} \quad (21)$$

or

$$\alpha_{\text{R}} = \alpha_{\text{F}}\left(\frac{d'_{\text{MP}}}{d_{\text{MP}}}\right)^2 \quad (22)$$

where  $m_{\text{R}}d_{\text{MP}}/d'_{\text{MP}}$  and  $t_{\text{on}}d'_{\text{MP}}/d_{\text{MP}}$  replace  $m_{\text{F}}$  and  $t_{\text{off}}$ , respectively. Using these simplifying relations reduces  $\Delta i_{l(\text{eff})}$  to

$$\begin{aligned} \Delta i_{l(\text{eff})} &= -2K\alpha_{\text{R}}\left(\frac{t_{\text{on}}}{2}\right)^2 - 2m_{\text{R}}(1 - K)\left(\frac{t_{\text{on}}}{2}\right) \\ &= 2\left|i_{l(\text{eff})\text{.R}}|_{0.5t_{\text{on}}}\right| = 2\left|i_{l(\text{eff})\text{.F}}|_{0.5t_{\text{off}}}\right| \end{aligned} \quad (23)$$

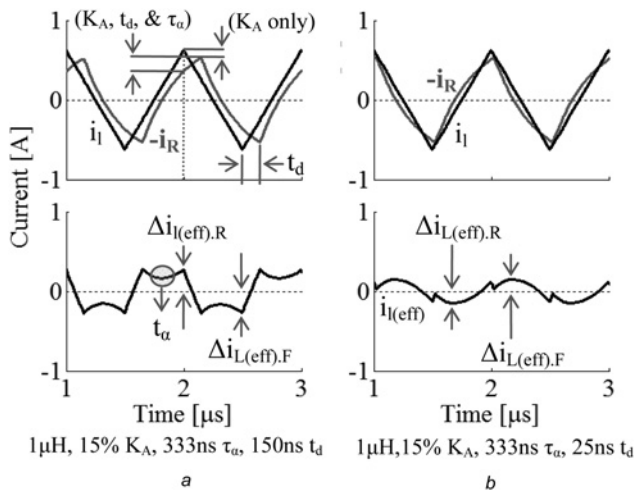
which means the worst-case variation during a rising  $i_{l\text{.L}}$  event equals that of its falling counterpart. Recalling  $\Delta i_{l\text{.L}}$  is the product of rising rate  $m_{\text{R}}$  and  $t_{\text{on}}$  and the current-based inductor multiplication factor is the ratio of  $\Delta i_{l\text{.L}}$  and  $\Delta i_{l(\text{eff})}$

$$\begin{aligned} M_{\text{I.N}} &\equiv \frac{L_{\text{Eff}}}{L_{\text{O}}} \equiv \frac{\Delta i_{l\text{.L}}}{\Delta i_{l(\text{eff})}} \\ &= \frac{m_{\text{R}}t_{\text{on}}}{-2K\alpha_{\text{R}}(t_{\text{on}}/2)^2 - 2m_{\text{R}}(1 - K)(t_{\text{on}}/2)} \\ &= \frac{m_{\text{R}}}{-K(0.5\alpha_{\text{R}}t_{\text{on}} - m_{\text{R}}) - m_{\text{R}}} = 2\left(\frac{m_{\text{R}}}{\alpha_{\text{R}}t_{\text{on}}} - 1\right) \end{aligned} \quad (24)$$

where  $M_{\text{I.N}}$  is the multiplication factor in the presence of non-linear error  $\alpha$ , reveals that the decreasing effect of a non-linearity in  $i_{r\text{.R}}$  on  $M_{\text{I.N}}$  is more pronounced with slower rise and fall times because the mid on- and off-time (i.e. worst case) differences between a linear and an exponential (or second-order) response is worse (i.e. greater) as more time elapses (i.e. slower  $di_{l\text{.L}}/dt$  rates). Given the true nature of non-linearity effects in RC circuits, it is useful to consider the time constant that produced  $\alpha$  in the first place with respect to switching period  $T_{\text{SW}}$ , in other words,  $R_{\text{T}}C_{\text{T}}$  or  $L_{\text{O}}/R_{\text{ES.R.L}}$  time-constant  $\tau_{\alpha}$ . In this sense,  $\alpha$  is inversely proportional to  $\tau_{\alpha}$  (i.e. a small  $\alpha$  value corresponds to a large  $\tau_{\alpha}$ ), which means an infinitely large  $\tau_{\alpha}$  produces no discernable non-linear effects in  $i_{r\text{.R}}$  within finite switching period  $T_{\text{SW}}$  (i.e. the multiplier circuit integrates its square input current perfectly and therefore produces a nearly flawless triangular current) and yields a substantially high inductor multiplication factor.

### 3 Combined effects

Although replica current  $i_{r\text{.R}}$  contains amplitude, delay and non-linearity errors, one of these often dominates and determines the nature of the resulting response. The inductor multiplier, by design, should balance and trade-off the dominant error for another to minimise the total variation in effective output inductor current  $i_{l(\text{eff})}$ , producing in the process a combined effect. In the case where amplitude (i.e.  $K_{\text{A}}$ ) and delay (i.e.  $t_{\text{d}}$ ) errors overwhelm non-linearity (i.e.  $\tau_{\alpha}$ ), the ac component of  $i_{l(\text{eff})}$  mostly conforms to the triangular and trapezoidal shapes  $K_{\text{A}}$  and  $t_{\text{d}}$  induce on  $i_{l(\text{eff})}$ , as illustrated in Fig. 7a,



**Figure 7** Spice simulation results showing the effect of non-linearity time-constant error  $\tau_\alpha$  in the presence of amplitude and delay errors  $K_A$  and  $t_d$  in replica current  $i_R$  on output ripple current  $i_{L(eff)}$  when  $K_A$  and  $t_d$

a Are dominant  
b Are not dominant

yielding a worst-case peak-to-peak ripple at  $M_P$ 's switching transitions  $t_{on}$  and  $t_{off}$ . On the other hand, as shown in Fig. 7b, in the event  $\tau_\alpha$  effects dominate over those of  $K_A$  and  $t_d$ , the peak ripple occurs closer to half-way through  $M_P$ 's on and off conduction times (i.e. at  $0.5t_{on}$  and  $0.5t_{off}$ ).

In the first case, when amplitude and delay errors dominate (Fig. 7a), the total peak-peak error can be divided into two parts: the portion impacted by all  $K_A$ ,  $t_d$  and  $\tau_\alpha$  and the one only due to  $K_A$ . The sums of the two parts at the end of the on time and at the end of the off time are, respectively

$$\begin{aligned} \Delta i_{L(eff).R} &= \Delta i_{K_A} + \Delta i_{K_A, t_d, \tau_\alpha} \\ &= \left( \frac{K_A}{2} \right) \Delta i_L + K(1 - K_A)(m_R t - \alpha_R t^2) \Big|_{t_{on} - t_d}^{t_{on}} \\ &= \frac{K_A}{2} (\Delta i_L) + K(1 - K_A)(m_R t_d + \alpha_R t_{on}^2 - 2\alpha_R t_{on} t_d) \end{aligned} \quad (25)$$

and

$$\begin{aligned} \Delta i_{L(eff).F} &= \Delta i_{K_A} + \Delta i_{K_A, t_d, \tau_\alpha} \\ &= \left( \frac{K_A}{2} \right) \Delta i_L + K(1 - K_A)(m_F t - \alpha_F t^2) \Big|_{t_{off} - t_d}^{t_{off}} \\ &= \left( \frac{K_A}{2} \right) \Delta i_L + K(1 - K_A)(m_F t_d + \alpha_F t_{off}^2 - 2\alpha_F t_{off} t_d) \\ &= \left( \frac{K_A}{2} \right) \Delta i_L + K(1 - K_A) \\ &\quad \times \left( m_R \left( \frac{d_{MP}}{d'_{MP}} \right) t_d + \alpha_R t_{on}^2 - 2\alpha_R t_{on} \left( \frac{d_{MP}}{d'_{MP}} \right) t_d \right) \end{aligned} \quad (26)$$

Therefore the combination of  $K_A$ ,  $t_d$  and  $\tau_\alpha$ , when dominated by  $K_A$  and  $t_d$ , yields effective ripple current  $\Delta i_{L(eff)}$

$$\begin{aligned} \Delta i_{L(eff)} &= \Delta i_{L(eff).R} + \Delta i_{L(eff).F} = K_A (\Delta i_L) + K(1 - K_A) \\ &\quad \times \left( \frac{m_R t_d}{d'_{MP}} + 2\alpha_R t_{on}^2 - \frac{\alpha_R t_{on} t_d}{d'_{MP}} \right) \end{aligned} \quad (27)$$

The multiplication factor, again defined in terms of current, is a ratio with  $\Delta i_L$  in the numerator and the above expression in the denominator. In the case where  $\alpha$  is substantially small (or  $\tau_\alpha$  practically infinite and scaling factor  $K$  nearly one), the multiplication factor simplifies to

$$\begin{aligned} M_{I.A.D.N} \Big|_{\alpha \rightarrow 0, K \rightarrow 1} &\equiv \frac{\Delta i_L}{\Delta i_{L(eff)}} \\ &= \frac{d_{MP} d'_{MP} T_{SW}}{t_d (1 - K_A) + d_{MP} d'_{MP} T_{SW} K_A} \end{aligned} \quad (28)$$

The likelihood  $\tau_\alpha$  effects dominate over those of  $K_A$  and  $t_d$  (Fig. 7b), however, is low because the degree of non-linearity required to overwhelm amplitude error and delay errors (given practical  $K_A$  and  $t_d$  values of 5–10% and 50–100 ns) is unrealistically high (e.g.  $\tau_\alpha$  must be below 5–20% of  $T_{SW}$ ). Even if non-linearity is introduced intentionally, there is no reason to make it dominant.

From a design perspective, it helps to reduce the combined effects of all errors (i.e.  $M_{I.A.D.N}$ ) into a compact, easy-to-discern format. Intuitively, and as shown, a dominant error prevails over the others (i.e.  $M_{I.A.D.N}$  is approximately the worse of  $M_{I.A}$ ,  $M_{I.D}$  and  $M_{I.N}$ ), and the impact of non-dominant errors is to reduce  $M_{I.A.D.N}$  slightly. Interestingly, resistors in parallel behave in a similar fashion, that is, higher resistances (e.g.  $R_{HI}$ ) pull the combined resistance (e.g.  $R_{TOT}$ ) below the lowest resistance in the network (e.g.  $R_{LOW}$ ), where the combined resistance is closest to the lowest (e.g.  $R_{TOT} \approx R_{LOW}$ ) when the lowest is substantially lower than the rest (e.g.  $R_{LOW} < 0.1R_{HI}$ ). As such,  $M_{I.A.D.N}$  may be empirically expressed as the (resistive) parallel combination of its constituent factors, where the lowest individual factor dominates  $M_{I.A.D.N}$  and other factors have a tendency to decrease  $M_{I.A.D.N}$  below the lowest factor

$$\begin{aligned} M_{I.A.D.N} &\approx M_{I.A} \parallel M_{I.D} \parallel M_{I.N} \\ &= \frac{M_{I.A} M_{I.D} M_{I.N}}{M_{I.A} M_{I.D} + M_{I.D} M_{I.N} + M_{I.N} M_{I.A}} \end{aligned} \quad (29)$$

Note, for example, that when non-linearity is negligible (i.e.  $M_{I.N}$  is infinitely high), (29) reduces to

$$\begin{aligned} M_{I.A.D.N} \Big|_{M_{I.N} \rightarrow \infty} &\approx \frac{M_{I.D} M_{I.A}}{M_{I.D} + M_{I.A}} \\ &= \frac{d_{MP} d'_{MP} T_{SW}}{t_d + d_{MP} d'_{MP} T_{SW} K_A} \end{aligned} \quad (30)$$

which is almost identical to (28). To further qualify the foregoing approximation, consider the practical case where delay and amplitude errors dominate, such as when  $t_d$  is 20 ns,  $K_A$  is 0.05,  $\alpha_R$  is  $0.001 \text{ A}/\mu\text{s}^2$ ,  $d_{MP}$  is 0.3,  $T_{SW}$  is 500 ns,  $V_{IN}$  is 3 V and  $L_O$  is  $0.5 \mu\text{H}$ .  $M_{I.A.D.N}$  in this scenario is 10.21 (from simulation results) and the simplified expression of (29) predicts 10.17, which represents a 0.4% error. If on the other hand, error dominance is less prevalent (i.e. all three errors have similar impact), such as in the case where  $t_d$  is 10 ns,  $K_A$  is 0.1,  $\alpha_R$  is  $0.01 \text{ A}/\mu\text{s}^2$ ,  $d_{MP}$  is 0.5,  $T_{SW}$  is  $1 \mu\text{s}$ ,  $V_{IN}$  is 4 V and  $L_O$  is  $1 \mu\text{H}$ ,  $M_{I.A.D.N}$  is 4.58 and (29) predicts 5.19, a value that is 13% off its target. Simulation results of several cases, in fact, show the error is usually within 10% and less often up to 20%. The accuracy ultimately improves when one factor is considerably larger (i.e. its corresponding error is negligible) or smaller (i.e. its corresponding error is dominant) than the others, which is more likely to occur in a practical application.

#### 4 Realistic inductor multipliers in switching regulators

Thus far, inductor multiplication factor  $M_I$  has been defined as the ratio of inductor ripple current  $\Delta i_L$  to effective ripple current  $\Delta i_{L(\text{eff})}$ . However, because the overriding objective of a switching regulator (Fig. 1) is to suppress variations in output voltage  $v_O$ , and increasing (or multiplying)  $L_O$  is only a means to reducing steady-state voltage ripple  $\Delta v_O$ , a current-based definition is not always as meaningful as a voltage-based one. The fact is output capacitor  $C_O$  integrates  $\Delta i_{L(\text{eff})}$  and the shape and frequency content of  $\Delta i_{L(\text{eff})}$  (not just the amplitude) determine  $\Delta v_O$ . For example, while the same  $\Delta i_{L(\text{eff})}$  ripple could result from gain error (as shown with triangular  $\Delta i_{L(\text{eff})}$  in Fig. 8a) or delay (as with trapezoidal  $\Delta i_{L(\text{eff})}$  in Fig. 8b) alone or a combination of both, the same peak-to-peak output ripple voltage (i.e.  $\Delta v_O$ ) does not necessarily result. Therefore the efficacy of the multiplier (i.e. the amount by which the effective inductance appears larger) should also be characterised by the ratio of  $\Delta v_O$  with and without the benefit of  $i_R$  (as denoted by  $M_V$ ). If the voltage across  $R_{ESR,C}$  (i.e.  $\Delta v_{ESR}$ ) overwhelms that of  $C_O$  (i.e.  $\Delta v_C$ ), however, output ripple voltage  $\Delta v_O$  is only a linear translation of  $i_{L(\text{eff})}$  (i.e.  $\Delta v_O = \Delta v_C + \Delta v_{ESR} \simeq \Delta v_{ESR} = R_{ESR,C} \dot{i}_{L(\text{eff})}$ ), which means current-based multiplication factor  $M_I$ , when applied to high-ESR capacitors, is equivalent to its voltage-based counterpart, that is,  $M_I$  equals  $M_V$ . In general,  $M_I$  does not account for the shape of  $i_{L(\text{eff})}$ , and  $M_V$  accounts for it in the manner most relevant to switching regulators: output ripple voltage accuracy.

Voltage-based inductor multiplication factor  $M_V$  for low-ESR output capacitors is the ratio of  $\Delta i_L$  to  $\Delta i_{L(\text{eff})}$ , but integrated by  $C_O$ . Deriving the output voltage ripple effects of  $i_L$  alone without the multiplier amounts to integrating half the ac inductor current ripple into  $C_O$  from time  $t_a$  to  $t_b$  (i.e. half period  $T_{SW}$ ) in Fig. 8a, which is the area under

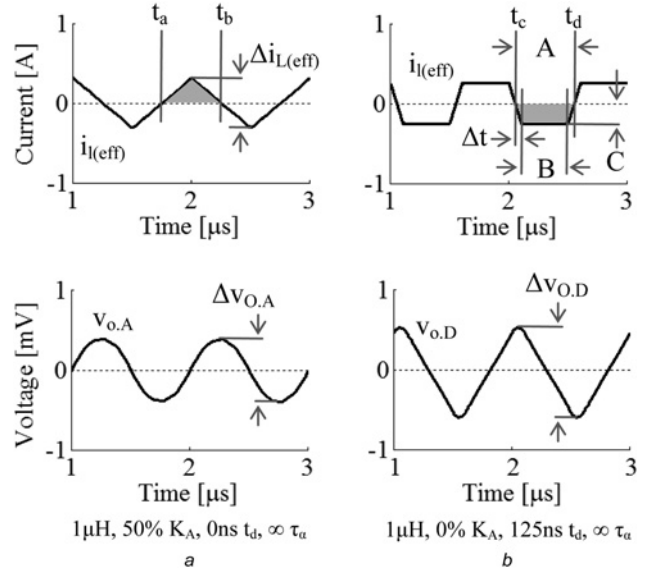


Figure 8 Spice simulation results showing the effects of  
 a Gain  $K_A$   
 b Delay  $t_d$  errors on output voltage ripple  $\Delta v_O$

the specified triangle

$$\Delta v_{O,L} = \frac{\Delta Q}{C_O} = \frac{1}{C_O} \left( \int_{t_a}^{t_b} i_L dt \right) = \frac{(0.5 \Delta i_L)(0.5 T_{SW})}{2 C_O} = \frac{V_{IN} d_{MP} d'_{MP} T_{SW}^2}{8 L_O C_O} \quad (31)$$

where  $\Delta v_{O,L}$  is the output ripple without the multiplier and  $t_a$  and  $t_b$  mark the points when ac current  $i_L$  crosses zero, which coincide with the points when ac current  $i_{L(\text{eff})}$  crosses zero, but only if amplitude is the dominant error (Fig. 8a). In general, the boundaries for the integral of  $i_{L(\text{eff})}$  are not straightforward because the different combinations of errors affect the shape of the waveform drastically. However, in a simple case, such as when delay is the only error, integrating  $i_{L(\text{eff})}$  into  $C_O$  from  $t_c$  to  $t_d$  in Fig. 8b yields multiplied output ripple  $\Delta v_{O,L(\text{eff})}$ , which is proportional to the area of the highlighted trapezoid (i.e. the average of the parallel sides times the distance between them)

$$\Delta v_{O,L(\text{eff})} = \frac{1}{C_O} \left( \int_{t_c}^{t_d} i_{L(\text{eff})} dt \right) = \frac{1}{C_O} \left[ \frac{(A+B)}{2} C \right] = \frac{1}{C_O} (A - \Delta t) C = \frac{1}{C_O} \left[ A - \frac{C}{(di_{L(\text{eff})}/dt)} \right] C = \left( \frac{d'_{MP} d_{MP} T_{SW} - d_{MP} t_d}{C_O} \right) \left( \frac{d_{MP} V_{IN} t_d}{L_O} \right) \quad (32)$$

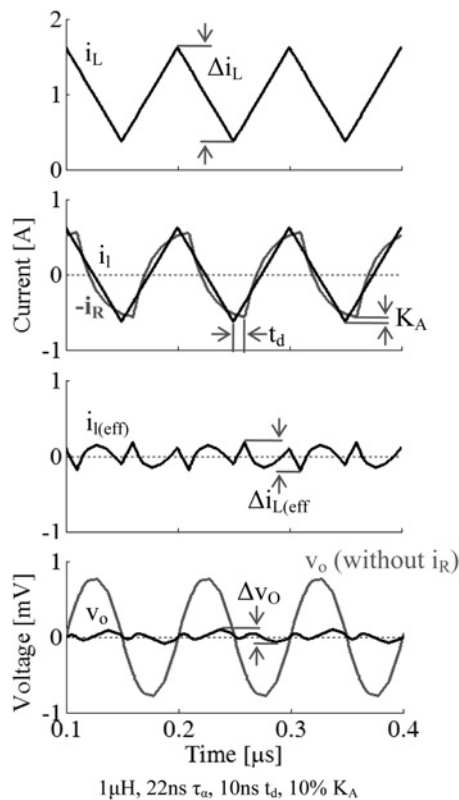
where  $A$ ,  $B$ ,  $C$  and  $\Delta t$  are the current levels and time intervals labelled in Fig. 8b. Voltage-based inductor multiplication

factor  $M_V$  for the simplified case of  $t_d$  therefore becomes

$$M_{V,D} \equiv \frac{\Delta v_{O,L}}{\Delta v_{O,L(\text{eff})}} = \frac{1}{8} \left[ \frac{d'_{MP}}{d'_{MP}(t_d/T_{SW}) - d_{MP}(t_d/T_{SW})^2} \right] \approx \frac{1}{8} \left( \frac{T_{SW}}{t_d} \right) \quad (33)$$

which means  $M_{V,D}$  is less sensitive to  $d'_{MP}$  (and  $d_{MP}$ ) than  $M_{I,D}$  in the presence of delay errors only. In fact, for a gain of 10 H/H in terms of  $M_{V,D}$ ,  $t_d$  can be no more than 1.25% of  $T_{SW}$  (e.g. less than 12.5 ns for a 1 MHz converter and less than 1.25 ns for a 10 MHz converter), unless duty cycles are at their extremes (e.g. 1 or 99%). In feedback schemes, where  $i_L$  is sensed and then replicated, sensing and applying  $i_R$  to  $v_O$  in less than 1.25–12.5 ns is considerably difficult under low-quiescent current conditions. Although feed-forward techniques [13] partially decrease this delay by deriving  $\Delta i_L$  information from further back in the ac path, matching and tracking delays down to 1.25–12.5 ns remains a substantial challenge.

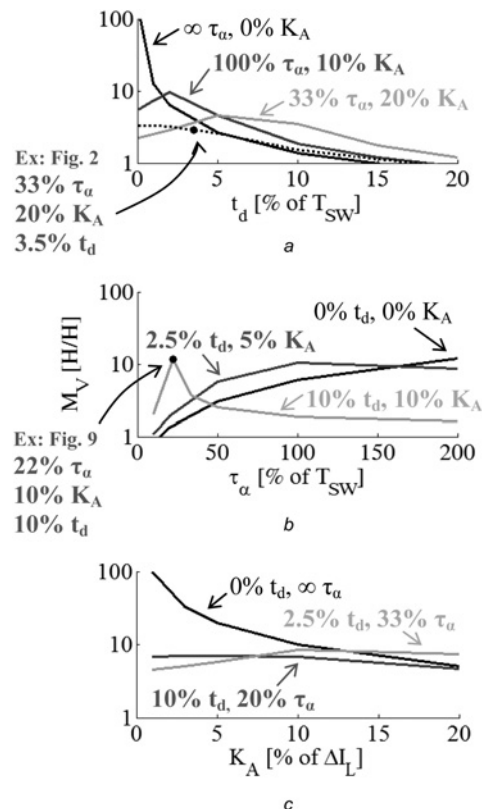
Simplifying the case to only delay errors, however, does not account for the possible cancelling effects of gain error and non-linearity. Non-linearity errors, in fact, accelerate the rising rate of  $-i_R$  (Fig. 6) and therefore offset the effects of delay errors. Fig. 9 illustrates an optimal case where time



**Figure 9** Spice simulation results showing how using the non-linearity ( $\tau_\alpha$ ) in replica current  $i_R$  to compensate for delay error  $t_d$  generates a ripple current  $\Delta i_{L(\text{eff})}$  that crosses zero more often and produces a smaller supply output ripple voltage  $\Delta v_O$

constant  $\tau_\alpha$  is sufficiently small to offset  $t_d$  and allow  $-i_R$  to lead  $i_L$  for part of the period, even when  $t_d$  is 10% of  $T_{SW}$ . Even though the impact on  $\Delta i_{L(\text{eff})}$  is not as significant,  $\Delta i_{L(\text{eff})}$  now crosses zero more often, as  $i_R$  shifts from leading to lagging  $i_i$ , which means  $\Delta v_O$  rises and falls more frequently and charges and discharges  $C_O$  less (i.e.  $\Delta v_O$  is smaller). (Fig. 9 also shows how  $v_O$ , without the benefit of  $i_R$ , exceeds its counterpart substantially because the unabated inductor current ripple  $\Delta i_L$  now charges and discharges  $C_O$ .) For comparison,  $M_V$  is 1.25 H/H when  $t_d$  is 10% of  $T_{SW}$  and other errors are negligibly small and 11.5 H/H when  $t_d$  is 10%,  $K_A$  is 10%, and  $\tau_\alpha$  is 22% of  $T_{SW}$ , and for the simulation in Fig. 9  $T_{SW}$  is 10 MHz.

In practice, delay  $t_d$  and gain  $K_A$  errors are unavoidable, and offsetting their effects with non-linearity  $\tau_\alpha$  is better but not perfect. With respect to  $t_d$ , the effects on inductor multiplication factor  $M_V$  are worse at high frequencies, when a small delay of 10 ns constitutes 10% of a 100 ns period  $T_{SW}$ , which barring  $K_A$  and  $\tau_\alpha$  errors, constrains  $M_V$  to less than 2 H/H, as shown by the black trace in Fig. 10a. The same delay would only be 0.1% of a 10  $\mu$ s period, and so at 100 kHz,  $M_V$  could be as high as 125 H/H. Similarly, neglecting other errors, a time constant less than 200% of  $T_{SW}$  or a gain error more than 10% would



**Figure 10** Spice simulation results showing the combined effects of delay  $t_d$ , non-linearity  $\tau_\alpha$ , and gain error  $K_A$  on inductor multiplication factor  $M_V$  with respect to

- a  $t_d$
- b  $\tau_\alpha$
- c  $K_A$

limit  $M_V$  to 10 H/H (as shown with the black traces in Figs. 10b and 10c, respectively). Furthermore, without non-linearity (i.e.  $\tau_\alpha$  is infinite) a 10% delay and 10% gain error would limit  $M_V$  to less than 2 H/H (as denoted by the light gray trace in Fig. 10b), negating almost entirely the cancellation purpose of  $i_R$ . However, intentionally reducing time constant  $\tau_\alpha$  to 20% of  $T_{SW}$  in the presence of these errors increases  $M_V$  to 10 H/H. A similar adjustment of  $\tau_\alpha$  is just as effective when  $t_d$  is 2.5% and  $K_A$  is 5% (Fig. 10b). Note Fig. 10 includes the combined effects of amplitude, delay and non-linearity errors and illustrates how various relative combinations of these errors alter the resulting multiplication factor of the circuit. Also note that even though the expressions derived earlier neglected the effects of a ripple in  $v_O$ , the simulation results shown do not, for they include the effects of  $C_O$  and  $R_{ESRC}$  both of which produce this ripple. Nevertheless, the derived expressions for the most part predict the results well because the ripple in the output of a switching supply, by design, is small.

Two of the examples discussed above were simulated, and the results are summarised in Table 1. In the first, just as in the experimental results shown in Fig. 2,  $K_A$  is 30%,  $t_d$  is 3.5% and  $\tau_\alpha$  is practically infinite. The simulated multiplication factors in this case are modest, but they agree with the experimental result and are predicted by (28), which is applicable because of the negligible non-linearity. In the second case,  $K_A$  is 10%,  $t_d$  is 10% and  $\tau_\alpha$  is 22%, which are the conditions chosen to demonstrate an optimal combination of delay and non-linearity, as depicted in Fig. 9; by itself,  $t_d$  would prohibit a worthwhile multiplication factor. Note that even though  $t_d$  is only

**Table 1** Simulation results for comparison with experimental example

	Example 1 (Fig. 2)	Example 2 (Fig. 9)
$\Delta i_L$ (mA <sub>pp</sub> )	378 <sup>a</sup>	1250
$\Delta i_R$ (mA <sub>pp</sub> )	265	1125
$K_A$ (%)	30	10
$T_{SW}$ ( $\mu$ s)	1	0.1
$t_d$ (ns)	35	10
$t_d$ (% of $T_{SW}$ )	3.5	10
$L$ ( $\mu$ H)	3.3	1
$R_{ESR}$ ( $\Omega$ )	0.335	45
$\tau_\alpha$ (% of $T_{SW}$ )	980 ( $\sim\infty$ )	22
$\Delta i_{L(\text{eff})}$ (mA <sub>pp</sub> )	151 <sup>a</sup>	375
$M_I$	2.5 <sup>a</sup>	3.3
$M_V$	2.9	11.5

<sup>a</sup>Compare to experiment in Fig. 2

10 ns (and it would be difficult to achieve a lower  $t_d$ ),  $t_d$  remains a considerable fraction of  $T_{SW}$ , which is only 100 ns. Nevertheless, due to the cancellation effect of non-linearity,  $M_V$  is 11.5 so the multiplier circuit suppresses the output voltage ripple by more than an order of magnitude.

Generally, in increasing inductor multiplication factor  $M_V$ , partially cancelling the effects of one dominant error requires making one or two of the remaining errors equally significant. Additionally, the sensitivity of  $M_V$  to  $K_A$  in light of moderate-to-large delay and non-linearity is lower (i.e. dark and light grey traces are relatively flat in Fig. 10c) when compared to  $t_d$  and  $\tau_\alpha$  under similar conditions (as shown with the dark and light grey traces in Figs. 10a and 10b), which means the effects of  $t_d$  overwhelm those of  $K_A$ , and  $\tau_\alpha$  is more effective in compensating for  $t_d$ . Given delays in the signal path of  $i_L$  and  $i_R$  and that output inductance  $L_O$  can vary by as much as 40% or more with process corners and temperature, a post-processing tuning or trimming scheme with at least first-order temperature-tracking features is necessary, and performing this calibration cycle in situ and periodically is ideal, but maybe not essential.

## 5 Conclusions

Current-mode inductor multipliers for switching power-supply applications suffer from sensitivity to delay (i.e.  $t_d$ ), gain error (i.e.  $K_A$ ) and non-linearity (i.e. time constant  $\tau_\alpha$ ) in the replica current (i.e.  $i_R$ ) supposed to cancel the ac component of inductor current  $i_L$ . While a gain error in  $i_R$  retains the triangular shape desired in switching power supplies, delay and non-linearity induce trapezoidal and sinusoidal current signals. Ultimately, however, their effects on regulator accuracy (i.e. output ripple voltage  $\Delta v_O$ ) depend on output capacitor  $C_O$  and its equivalent series resistance  $R_{ESRC}$ , given low  $R_{ESRC}$  values integrate effective output current  $i_{L(\text{eff})}$  and large  $R_{ESRC}$  values only linearly translate  $i_{L(\text{eff})}$ , which is why inductor multiplication factor  $M_V$  is best based on voltage ripple  $\Delta v_O$  and not on current ripple  $\Delta i_{L(\text{eff})}$ . Ultimately, given typical circuit delays of 50–100 ns and practical state-of-the-art switching frequencies of 5–10 MHz,  $M_V$  is particularly sensitive to delay, but tuning or trimming non-linearity can offset those effects and yield an  $M_V$  on the order of 10 H/H. Non-linearity aside, in maximising  $M_V$ , sensing  $i_L$  to generate  $i_R$ , as presented in [5, 6, 9, 11], is more challenging than predicting  $i_R$  with feed-forward techniques, as in [10, 13], because the latter offsets delay by tapping further back in the ac-signal chain. Matching and tracking the feed-forward delay in  $i_R$  to the delay in  $i_L$  remains a practical challenge, but in this way, the total delay between  $i_R$  and  $i_L$  might realistically stay within 5–10 ns so that a factor of roughly 10 H/H may be achieved at 5–10 MHz, where 50–100 nH on-chip inductors start becoming viable. The possibility of fully integrating the switching power supply on chip (i.e. system-on-chip – solution) while producing state-of-the-art performance

appeals to the portable electronics market, especially the promising wireless micro-sensors space.

## 6 References

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