

# Harvesting Circuits for Miniaturized Photovoltaic Cells

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**Abstract**—Miniaturized systems like wireless microsensors suffer from short operational lifetimes because they lack space to store the energy that wireless transmission, signal conditioning, and monitoring require to operate across time. Harvesting ambient energy circumvents this limitation because the environment is a virtually boundless reservoir of energy. Of available sources, solar light produces the highest power density, and although artificial lighting is not as rich, thermal and magnetic sources produce even lower power densities and mechanical and chemical transducers are difficult to integrate. The problem is microscale photovoltaic (PV) cells only produce 1 and 100  $\mu\text{W}/\text{mm}^2$  for artificial and solar lighting, so the act of conditioning and transferring power can dissipate most, if not all, of the power available. The focus of this paper is to introduce and discuss the design challenges associated with harvesting circuits when harnessing, conditioning, and transferring power from tiny PV cells that only generate 1 – 100  $\mu\text{W}$ .

## I. HARVESTING MICROSYSTEMS

Although recent advances in the semiconductor industry suggest that integrating sensors, processors, memory, and radio transceivers into a wireless microsensor node is possible [1]–[2], powering these devices across extended periods remains an issue. The problem is limited space, because small batteries store little energy and replacing or recharging them periodically presents prohibitive personnel costs. Fortunately, because power-hungry functions like telemetry (TX in Fig. 1) seldom engage in a sensor node, drawing energy from the environment to continually charge a small battery is a viable and appealing alternative [1], [3].

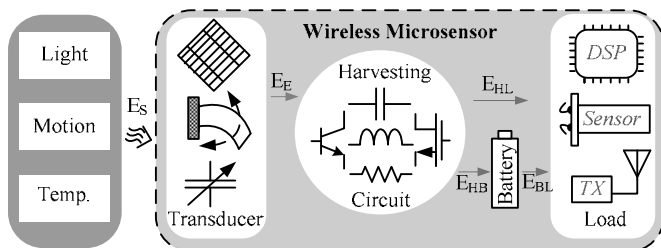


Fig. 1. Harvester-powered wireless microsensor.

Of available ambient sources, solar light offers the highest power density at more than 15  $\text{mW}/\text{cm}^2$  [4]. Artificial lighting generates considerably lower power at 10 – 100  $\mu\text{W}/\text{cm}^2$ , but thermal and magnetic sources produce even less at 1 – 15  $\mu\text{W}/\text{cm}^3$ . The challenge with piezoelectric and chemical transducers is integration. Kinetic energy in motion may produce moderate power at 1 – 300  $\mu\text{W}/\text{cm}^3$ , but not all

applications vibrate. Ultimately, because solar energy generates so much power, as Table I shows, light remains an alluring source for many practical applications. Still, harnessing light energy from tiny photovoltaic (PV) cells constrains power to below 100  $\mu\text{W}/\text{mm}^2$ , which parasitic components in the cell and the harvester circuit can exhaust.

TABLE I. POWER DENSITIES FROM AMBIENT ENERGY SOURCES.

Sources		Transduction Mechanism	Estimated Power Density
Light	Solar	Photovoltaic (PV)	< 15 $\text{mW}/\text{cm}^2$
	Artificial		10 – 100 $\mu\text{W}/\text{cm}^2$
Motion		Electrostatic	50 – 100 $\mu\text{W}/\text{cm}^3$
		Electromagnetic	< 1 $\mu\text{W}/\text{cm}^3$
		Piezoelectric	50 – 300 $\mu\text{W}/\text{cm}^3$
$\Delta\text{Temp. (10}^\circ\text{C)}$		Seebeck	5 – 15 $\mu\text{W}/\text{cm}^3$

The aim of this paper is to introduce and discuss the challenges involved in harnessing light energy from miniaturized PV cells that generate less than 100  $\mu\text{W}$ . To that end, Section II describes the electrical characteristics of PV cells that dictate (in Section III) the operating boundaries of a harvesting microsystem. Section IV then discusses and compares the design and efficiency performance of two basic harvesting approaches: switched-inductor and switched-capacitor circuits and Section V draws relevant conclusions.

## II. MINIATURIZED PHOTOVOLTAIC CELLS

Photons in incident light strike and break apart electron-hole (E-H) pairs in photovoltaic (PV) cells to generate current  $i_{\text{PH}}$ . Because PV cells are, at their core, pn-junction diodes,  $D_{\text{PV}}$  in the model of Fig. 2 [7] shunts and forward-biases with  $i_{\text{PH}}$ , if not steered elsewhere.  $D_{\text{PV}}$ 's junction capacitance  $C_{\text{PV}}$  also shunts  $i_{\text{PH}}$ , as does the parasitic peripheral shunt resistance across the structure  $R_{\text{PV}}$ . In conducting the fraction of  $i_{\text{PH}}$  that flows out of the cell as  $i_{\text{PV}}$ , equivalent series (contact) resistances (ESR)  $R_{\text{ESR}}$  raise  $D_{\text{PV}}$ 's voltage  $v_{\text{D}}$  to boost  $D_{\text{PV}}$ 's shunting effect on  $i_{\text{PH}}$ .  $R_{\text{PV}}$  and  $R_{\text{ESR}}$ 's combined impact on  $i_{\text{PV}}$ , however, is normally negligible in these tiny devices because  $R_{\text{ESR}}$  is small at a few  $\Omega$ 's and  $R_{\text{PV}}$  large at  $\text{M}\Omega$ 's:

$$i_{\text{PV}} = i_{\text{PH}} - I_{\text{S}} \exp\left(\frac{v_{\text{PV}} + i_{\text{PV}} R_{\text{ESR}}}{V_{\text{t}}}\right) - \left(\frac{v_{\text{PV}} + i_{\text{PV}} R_{\text{ESR}}}{R_{\text{PV}} \parallel \frac{1}{sC_{\text{PV}}}}\right)$$

$$\approx i_{PH} - I_S \exp\left(\frac{V_{PV}}{V_t}\right) - sC_{PV}V_{PV}, \quad (1)$$

where  $V_t$  is the thermal voltage and  $C_{PV}$  depends on  $v_{PV}$ .

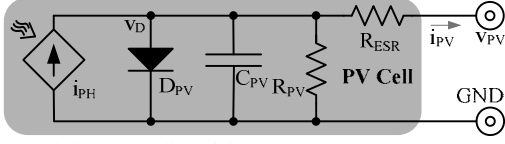


Fig. 2. Photovoltaic (PV) cell model.

Given a particular light intensity and corresponding  $i_{PH}$ ,  $D_{PV}$ 's shunting current  $i_D$  increases with  $v_{PV}$ . Accordingly, output power  $P_{PV}$ , or  $i_{PV}V_{PV}$ , grows with  $v_{PV}$  as long as the rise in  $P_{PV}$  exceeds that of diode power  $P_D$ , which is why  $P_{PV}$  peaks (at  $P_{PV(MAX)}$  in Fig. 3) when  $\Delta P_D$  begins to exceed  $\Delta P_{PV}$  (at optimum diode voltage  $V_{PV(OPT)}$ ). Increasing light intensity raises  $i_{PH}$  (and  $P_{PV}$ ), so  $i_D$  (and its corresponding  $V_{PV(OPT)}$ ) can rise before offsetting  $\Delta P_{PV}$ . Therefore, tracking maximum power-point  $V_{PV(OPT)}$  with respect to light intensity ensures the PV cell generates  $P_{PV(MAX)}$ .

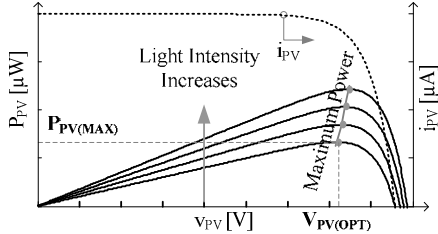


Fig. 3. Typical photovoltaic (PV) cell's power-current-voltage (P-I-V) curves.

### III. HARVESTING EFFICIENCY

The acts of converting, transferring, and conditioning energy dissipate power, which is why a harvesting system ultimately supplies a fraction of the energy it receives. A PV cell, for example, converts a fraction of photon source energy  $E_S$  (from Fig. 1) into the electrical domain  $E_E$  as  $i_{PH}$ . Then, depending on how well the system tracks  $V_{PV(OPT)}$ ,  $D_{PV}$ ,  $R_{PV}$ , and  $R_{ESR}$  in the cell dissipate a fraction of  $E_E$  to output  $E_{PV}$  in  $i_{PV}$ . The harvesting circuit, which transfers and conditions  $E_{PV}$  to charge a battery and supply a load, also consumes power, reducing  $E_{PV}$  to usable harvested energy  $E_H$  (i.e.,  $E_{HB}$  and  $E_{HL}$  in Fig. 1). As a result, the system efficiency of the harvester ( $\eta_S$ ) is the product of photon- $i_{PH}$ ,  $i_{PH}$ - $i_{PV}$ , and conversion efficiencies  $E_E/E_S$  or  $\eta_{PH}$ ,  $E_{PV}/E_E$  or  $\eta_{PV}$ , and  $E_H/E_{PV}$  or  $\eta_{CONV}$ :

$$\eta_S = \eta_{PH} \eta_{PV} \eta_{CONV}. \quad (2)$$

#### A. Light-Current Conversion

Of the photons available in incoming light, only those with energies exceeding the band-gap energy of the semiconductor used to build the PV cell can break apart E-H pairs to generate  $i_{PH}$ ; the material loses excess photon energy as heat. Light-conversion efficiency  $\eta_{PH}$  is therefore highest when the spectral energy of the incident light peaks at the band-gap energy of the material. Given this, when exposed to solar light, crystalline silicon outperforms other low-cost semiconductor technologies with efficiencies of 15% to 20% [5]. Amorphous silicon is slightly better under artificial lights and 10% to 20% cheaper, but the absence of a dedicated process and the

conversion efficiency of its crystalline counterpart (under variable lighting conditions and limited area) outweigh this small positive offset.

#### B. Tracking Performance

The act of tracking  $V_{PV(OPT)}$  also consumes energy, so balancing tracking accuracy with processing power is important. Predicting (rather than measuring)  $V_{PV(OPT)}$ 's optimum open-circuit point from empirical information typically offers the best tradeoff [6]–[7], because processing power is low. Monitoring the cell's open-circuit voltage is a weakness, however, because sensing a small open-circuit replica of the cell is wasteful of silicon area (i.e., cost) just as disconnecting the cell is of power (i.e., efficiency).

## IV. HARVESTER CIRCUIT

The application space this research targets is light-powered chip-sized sensors that operate continuously, even under cloud cover and artificial lights. Accordingly, this section describes the design constraints such an application places on a harvester circuit. Since the fundamental aim of the system is to generate output power, understanding where and how these circuits dissipate energy is vital, which is why, after operation and design, the focus here shifts to efficiency.

#### A. System Requirements

Tiny  $2 \times 2\text{-mm}^2$  PV cells typically generate less than  $100 \mu\text{W}$ , even under direct sunlight.  $C_{PV}$  for these devices is roughly  $1 \text{ nF}$  and, since  $D_{PV}$ 's current increases exponentially with  $v_{PV}$ ,  $V_{PV(OPT)}$  falls slightly below  $0.6 - 0.7 \text{ V}$  to around  $0.55 \text{ V}$ . Therefore, to charge a super capacitor at  $1 \text{ V}$  (i.e.,  $V_O$ ), for example, the harvester circuit must boost the cell's  $0.55 \text{ V}$  to  $1 \text{ V}$  with a switched-inductor (SI) or -capacitor (SC) circuit (because unswitched circuits cannot boost voltages). The switching action, unfortunately, produces a ripple at  $v_{PV}$  that deviates it from  $V_{PV(OPT)}$ , so variation  $\Delta v_{PV}$  must remain small (e.g.,  $50 \text{ mV}$ ) for  $P_{PV}$  to stay near  $P_{PV(MAX)}$ . Regulating  $v_{PV}$  about  $V_{PV(OPT)}$ , whether it be an SI or SC circuit, requires a feedback controller that must, by design, operate in sub-threshold (with nA's) to consume a diminutive fraction of  $P_{PV}$ . In all, SI and SC implementations must condition the PV cell according to these requirements, which Table II summarizes.

TABLE II. SYSTEM REQUIREMENTS.

Parameter	Value	Design Target	Value
$P_{PV}$	$\leq 100 \mu\text{W}$	$V_{PV(OPT)}$	$0.55 \text{ V}$
$C_{PV}$	$\approx 1 \text{ nF}$	$V_O$	$1 \text{ V}$
		$\Delta v_{PV}$	$\leq 50 \text{ mV}$

#### B. Switched-Inductor (SI) Boost Converter

**Operation:** SI circuits transfer energy by energizing (closing switch  $M_N$  in Fig. 4a) and de-energizing (closing  $M_P$ ) an inductor  $L_H$  from an input source  $i_{PV}$  into an output  $C_O$  in alternate switching cycles. When  $P_{PV}$  rises,  $L_H$  transfers energy packets more often, so switching frequency  $f_{SW}$  increases. While  $L_H$ 's ESR  $R_{L,ESR}$ ,  $M_N$ , and  $M_P$  dissipate Ohmic power,  $M_N$  and  $M_P$ 's drivers consume energy to charge and discharge  $M_N$  and  $M_P$ 's parasitic gate capacitances. However, because  $i_{PV}$  is low and transferring small packets of energy requires a high  $f_{SW}$ , Ohmic losses are not as significant as gate-drive losses. Fortunately, operating  $L_H$  discontinuously, which is to say  $L_H$ 's current  $i_L$  rises and falls back to zero in a fraction of the

switching period  $T_{SW}$ , as Fig. 4b shows, decreases the number of switching events (i.e., energy losses) per period.

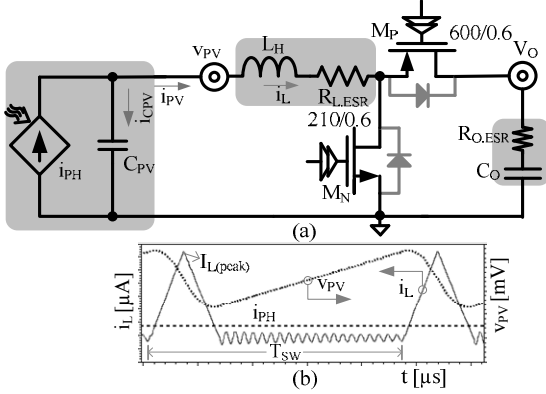


Fig. 4 (a) Switched-inductor circuit and (b) its simulated waveforms.

**Design:** To keep conduction losses (i.e.,  $\Delta i_L$ ) and system-in-package (SiP) dimensions low, a  $220\text{-}\mu\text{H}$ ,  $2 \times 2 \times 1\text{-mm}^3$  inductor implements  $L_H$ . With this  $L_H$ ,  $M_N$  and  $M_P$ 's respective aspect ratios should (at  $210\mu\text{m}/0.6\mu\text{m}$  and  $600\mu\text{m}/0.6\mu\text{m}$ ) balance conduction, switching, and control losses to minimize their net sum. Since  $i_L$  is discontinuous and  $i_{PH}$  is, for all practical purposes constant through  $T_{SW}$ , current difference  $i_L - i_{PH}$  discharges and charges  $C_{PV}$ , producing ripple  $\Delta v_{PV}$ . However, because  $L_H$  must energize to and de-energize from  $i_{L(PEAK)}$  (through conduction time  $t_c$ ) to store and transfer  $i_{PH}$ 's maximum energy as charge  $q_L$ , worst-case ripple  $\Delta v_{PV(MAX)}$  occurs when  $i_{PH}$  is so small that  $C_{PV}$  supplies all of  $q_L$ :

$$\Delta v_{PV(MAX)} = \frac{q_L}{C_{PV}} = \frac{0.5t_c i_{L(PEAK)}}{C_{PV}} \leq 50 \text{ mV}, \quad (3)$$

where  $V_{PV(OPT)}$ ,  $V_O$ , and the converter's minimum delay across the loop set  $t_c$  and  $P_{PV(MAX)}$  and  $L_H$  set  $i_{L(PEAK)}$  [10].

**Losses:**  $L_H$ 's  $R_{L,ESR}$  and  $M_P$  and  $M_N$ 's combined resistance  $R_{SW,EQ}$  conduct  $i_L$ , so they dissipate root-mean-square (RMS) Ohmic loss  $P_R$ :

$$P_R = i_{L(RMS)}^2 (R_{L,ESR} + R_{SW,EQ}). \quad (4)$$

$M_N$  also consumes power  $P_{IV}$  while conducting  $i_{L(PEAK)}$  and transitioning from zero to  $V_O + V_D$  across overlap time  $t_{OV}$ :

$$P_{IV} = \left[ \frac{i_{L(PEAK)} (V_O + V_D)}{2} \right] \left( \frac{t_{OV}}{T_{SW}} \right), \quad (5)$$

where  $V_D$  is  $M_P$ 's body's diode voltage. Plus,  $M_N$  and  $M_P$ 's drivers dissipate energy every cycle to charge and discharge  $M_N$  and  $M_P$ 's combined gate capacitance  $C_{G,EQ}$  across  $V_O$ :

$$P_G = \frac{C_{G,EQ} V_O^2}{T_{SW}} = C_{G,EQ} V_O^2 f_{SW}. \quad (6)$$

Because  $L_H$  transfer pockets of energy more often when  $P_{PV}$  increases,  $i_{L(RMS)}$  increases with  $f_{SW}$ , as do  $P_{IV}$  and  $P_G$ , although not to the same extent, as Fig. 5 shows, assuming feedback controller losses  $P_Q$  is constant at  $1 \mu\text{W}$ .

### C. Boosting Switched-Capacitor (SC) Charge Pump

**Design:** SC circuits boost and transfer energy by first paralleling (i.e., charging) flying capacitors ( $C_{FLY}$  in Fig. 6a) and then connecting (and discharging) them in series with the source ( $v_{PV}$ ) to output  $V_O$ . In the parallel phase,  $v_{PV}$  first drops

to  $V_{PV(MIN)}$  because  $C_{PV}$  de-energizes quickly into partially discharged  $C_{FLY}$ , as Fig. 6b shows, and then rises to  $V_{PV(MAX)}$  as  $i_{PH}$  charges  $C_{PV}$  and  $C_{FLY}$  through the phase. In the series phase,  $v_{PV}$  again drops to  $V_{PV(MIN)}$  because  $C_{PV}$  and  $C_{FLY}$  discharge into  $C_O$  and then rises because  $i_{PH}$  charges  $C_{PV}$  and  $C_O$  and discharges  $C_{FLY}$ . As before, the circuit transfers energy packets more often (i.e.,  $f_{SW}$  increases) when  $i_{PH}$  rises.

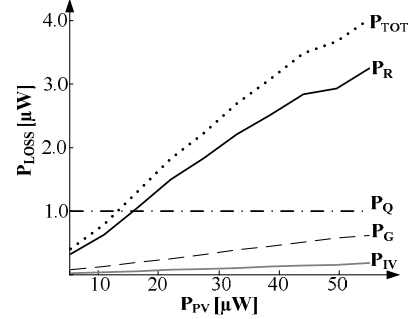


Fig. 5. Simulated switched-Inductor losses across  $P_{PV}$ .

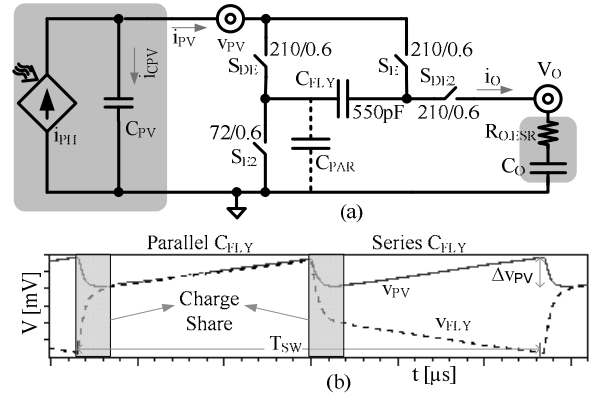


Fig. 6. (a) Switched-capacitor circuit and (b) its simulated waveforms.

**Design:** Worst-case ripple  $\Delta v_{PV(MAX)}$  occurs when  $i_{PV}$  is low, when only  $C_{PV}$ 's energy charges  $C_{FLY}$  quickly from  $V_{FLY(MIN)}$  to  $V_{PV(MIN)}$  in the parallel phase:

$$C_{PV} \Delta v_{PV(MAX)} = C_{FLY} (V_{PV(MIN)} - V_{FLY(MIN)}), \quad (7)$$

and rises slowly from there to  $V_{PV(MAX)}$ . Because  $V_O$  drops across  $C_{PV}$  and  $C_{FLY}$  (with a low  $i_{PH}$ ) at the end of the series phase,  $V_{FLY(MIN)}$  is  $V_O - V_{PV(MAX)}$  and  $\Delta v_{PV(MAX)}$  is

$$\begin{aligned} \Delta v_{PV(MAX)} &\approx \left( \frac{C_{FLY}}{C_{PV}} \right) (V_{PV(MIN)} + V_{PV(MAX)} - V_O) \\ &\approx \left( \frac{C_{FLY}}{C_{PV}} \right) (2V_{PV} - V_O) \leq 50 \text{ mV} \end{aligned} \quad (8)$$

So, to ensure  $C_{PV}$  does not discharge beyond  $\Delta v_{PV(MAX)}$ ,  $C_{PV}$  (at  $1 \text{ nF}$ ) should be considerably higher than  $C_{FLY}$ . A smaller  $C_{FLY}$ , however, decreases the charge the circuit delivers per cycle, so  $f_{SW}$  and associated losses rise as a result. In this case, switching  $550 \text{ pF}$  at  $74 \text{ kHz}$  keeps  $\Delta v_{PV}$  below  $50 \text{ mV}$  and transistors' aspect ratios in Fig. 6a ensure  $C_{FLY}$  charges completely in the parallel phase (across  $0.5T_{SW}$ ) for the highest possible  $i_{PH}$ .

**Losses:**  $C_O$  charges only in the series phase, and since  $C_{PV}$  does not supply power because there is no net change in its voltage (i.e., charge) across this phase, only  $i_{PH}$  reaches  $V_O$

(for  $0.5T_{SW}$ ) to deliver  $0.5i_{PH}V_O$  as output power  $P_O$ . Therefore, of  $P_{PV}$  (or  $i_{PH}V_{PV}$ ), the switches dissipate (as Ohmic power  $P_R$ ) what  $C_O$  fails to receive in  $P_O$ :

$$P_R = P_{PV} - P_O = i_{PH}(V_{PV} - 0.5V_O), \quad (9)$$

so, irrespective of the resistance (size) of the switch,  $P_R$  increases with  $i_{PH}$ , as does  $f_{SW}$ . An on-chip  $C_{FLY}$ , unfortunately, introduces a parasitic bottom-plate capacitor  $C_{PAR}$  (at roughly  $0.1C_{FLY}$  [8]) that an off-chip  $C_{FLY}$  does not, so the switches dissipate additional energy to charge and discharge  $C_{PAR}$ . In other words,  $P_R$  is higher when  $C_{FLY}$  is on chip, which is why internal  $P_{R(INT)}$  is higher than external  $P_{R(EXT)}$  in Fig. 7. Switch drivers also consume power  $P_G$  when they charge and discharge gate capacitors  $C_{G,EQ}$  every cycle:

$$P_G = 2(0.5C_{G,EQ}V_O^2)f_{SW}. \quad (10)$$

Since increasing  $i_{PH}$  means  $f_{SW}$  increases,  $P_G$  also increases with  $P_{PV}$ . As with the SI counterpart, Fig. 7 also assumes quiescent controller power  $P_Q$  is constant across  $P_{PV}$  at  $1 \mu W$ .

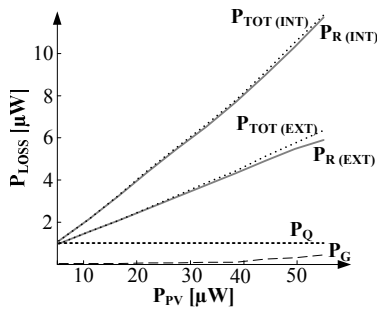


Fig. 7. Simulated on-chip and off-chip switched-capacitor losses across  $P_{PV}$ .

#### D. Inductor- versus Capacitor-Based Harvesters

Irrespective of the approach, RMS current increases with  $P_{PV}$ , so Ohmic losses  $P_R$  are proportional to  $P_{PV}$  and also dominant across most of  $P_{PV}$ .  $P_R$  is lower in SI converters, however, because for the same  $P_{PV}$ ,  $i_L$ 's peak is lower than  $i_{CFLY}$ 's in SC circuits, which means RMS currents are higher in SC implementations.  $P_R$  is also considerably higher when  $C_{FLY}$  is on chip, which means SC circuits trade efficiency for integration. More importantly, SI converters need only two transistors to boost  $v_{PV}$  to almost any output voltage  $V_O$ , whereas their SC counterparts require considerably more switches, and SC efficiencies tend to suffer when  $V_O$  varies [11]. This is important because the harvester's output is a battery voltage that spans, for example, 0.9 – 1.6 V for NiCd's and NiMH's, 2.7 – 4.2 V for Li Ions, and an even wider range for ultra capacitors. In other words, SI circuits that use only one in-package inductor seem better suited for harnessing light energy from miniaturized PV cells.

A more subtle, but equally important observation is that controller quiescent power  $P_Q$  consumes a considerable fraction of all the losses, where even though driving gates dissipate power  $P_G$ ,  $P_G$  is not as important. Note, however, these results only apply to chip-sized light-energy harvesters. Consider that, while voltage regulators draw whatever current is necessary from an input source to regulate the voltage across a variable load, light-energy harvesters regulate the voltage across an input source to draw and deposit as much current as possible into a low-impedance output: a battery. What is more, the power levels chip-sized PV cells generate

are substantially low, at less than  $100 \mu W$ , so the conclusions drawn in [9], which relate to *higher voltage* and *higher power voltage regulators*, do not necessarily apply here.

#### V. CONCLUSIONS

For chip-sized light-harvesting circuits to generate power, they must dissipate less energy than miniaturized photovoltaic (PV) cells generate, which might not even exceed  $100 \mu W$ . The problem is that the photon-current conversion process, the parasitic diode ( $D_{PV}$ ) in the PV cell, and the harvester circuit all consume power. Therefore, to maximize PV power  $P_{PV}$  and minimize  $D_{PV}$  losses, the harvester should regulate PV voltage  $v_{PV}$  to optimum target  $V_{PV(OPT)}$  within a small window  $\Delta V_{PV(MAX)}$ . Similarly, to maximize harvested output power, the circuit should be efficient, which is to say it should transfer and condition power by switching an in-package inductor. Still, Ohmic losses  $P_R$  are dominant and proportional to  $P_{PV}$ , with controller quiescent power  $P_Q$  not far behind and gate-charging losses  $P_G$  further back. Interestingly, capacitor-based circuits consume more Ohmic power  $P_R$  because they conduct higher RMS currents (since  $i_{CFLY}$  peaks to a higher value than  $i_L$ ). Moreover, on-chip implementations lose additional power in charging and discharging parasitic bottom-plate capacitors. In other words, switched-inductor harvesters harness more light energy from chip-sized PV cells than switched-capacitor circuits, which is especially important when  $P_{PV}$  is low, cloud cover and artificial lighting conditions persist, and unobtrusiveness (i.e., integration) is imperative.

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