

# A 0.7- $\mu\text{m}$ BiCMOS Electrostatic Energy-Harvesting System IC

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**Abstract**—Self-powered microsystems like wireless microsensors and biomedical implants derive power from in-package minibatteries that can only store sufficient energy to sustain the system for a short life. The environment, however, is a rich source of energy that, when harnessed, can replenish the otherwise exhausted battery. The problem is harvesters generate low power levels and the electronics required to transfer the energy to charge a battery can easily demand more than the power produced. This paper presents how a  $1 \times 1 \text{ mm}^2$  0.7- $\mu\text{m}$  BiCMOS vibration-supplied electrostatic energy-harvesting system IC produces usable energy. The IC charges and holds the voltage across a vibration-driven variable capacitor  $C_{VAR}$  so that ambient kinetic energy can induce  $C_{VAR}$  to generate current into the battery when capacitance decreases, as the plates separate. The precharger, harvester, monitoring, and control microelectronics draw enough power to operate, yet allow the system to yield (experimentally) 1.27, 2.14, and 2.87 nJ per vibration cycle for battery voltages at 2.7, 3.5, and 4.2 V, which at 30 Hz produce 38.1, 64.2, and 86.1 nW. Experiments further show that the harvester system prototype charges  $1 \mu\text{F}$  (emulating a small thin-film Li Ion) from 3.5 to 3.81 V in 35 s.

**Index Terms**—Electrostatic energy harvester IC, low energy, microsensor, microsystem, vibration.

## I. VOLTAGE-CONSTRAINED ELECTROSTATIC ENERGY HARVESTING

**M**ICROSCALE devices like sensing nodes in wireless networks [1], [2] and biomedical implants [3]–[5] typically operate in inaccessible environments where recharging and replacing a battery are prohibitive. For this reason, self-powering these systems from miniaturized energy sources, such as thin-film Li Ions [6]–[8] and microscale fuel cells [9], is important. The problem is limited space constrains energy storage to the point short lifetimes are only possible. By harnessing ambient energy, however, from light [10], thermal gradients [8], [11]–[13], and/or vibrations [14] and [15], harvesters can replenish what the system consumes, keeping its low-capacity battery charged and, in consequence, extending its operational life [16].

Although sunlight provides considerable energy, indoor lights furnish 1–2 orders of magnitude less energy, just as thermal gradients across a microscale platform cannot induce large enough temperature differences [14] to produce meaningful power levels (without the aid of impractically large heat sinks). Vibrations may not generate as much power as sunlight

but they consistently and reliably produce considerably more than indoor lighting and thermal gradients [14]. Converting energy from strain on piezoelectric materials [17]–[19] or motion of a coil through a magnetic field [20]–[22], however, generates ac voltages that require a power-hungry rectifier and demand difficult-to-integrate materials. Fortunately, microelectromechanical systems (MEMS) can integrate vibration-sensitive capacitors [14], [23] with which to harness kinetic energy [24] and [25].

As vibrations work against the electrostatic force of a mechanical variable capacitor  $C_{VAR}$  to push its plates apart, electrostatic harvesters draw and convert kinetic energy from the environment [14], [24]–[26]. One way of doing so is by constraining the charge in  $C_{VAR}$  so that, as vibrations separate  $C_{VAR}$ 's plates, capacitance decreases and capacitor voltage  $v_C$  increases ( $Q_{CONST} = C_{VAR}v_C$ ), augmenting the energy stored in  $C_{VAR}$  in the process. The drawback is that  $v_C$  can increase to voltages (e.g., 300 V) that easily exceed the breakdown limits of high-volume (low-cost) semiconductor processes (e.g., 5–12 V), requiring higher voltage transistors that are only available in more expensive technologies, like in silicon-on-insulator (SOI) technologies [27]. Alternatively, fixing the capacitor voltage and allowing vibrations to change capacitance produces charge  $q_C$  ( $q_C = C_{VAR}V_{CONST}$ ) in the more benign form of harvesting current  $i_{HARV}$ :

$$\begin{aligned} i_{HARV} &= \frac{dq_C}{dt} \\ &= \frac{d(C_{VAR}V_{CONST})}{dt} \\ &= V_{CONST} \left( \frac{\partial C_{VAR}}{\partial t} \right). \end{aligned} \quad (1)$$

Although constraining voltage is compatible with standard processes, typical implementations employ an additional voltage source [24] (which contradicts the goals of integration) to fix  $C_{VAR}$ 's voltage and an energy-transferring circuit (that consumes power) to charge the battery. Connecting  $C_{VAR}$  to a constraining capacitor (i.e., a low-capacity battery) via a unidirectional diode [28] and [29] holds  $C_{VAR}$ 's voltage, but only momentarily because  $i_{HARV}$  raises the constraining capacitor's voltage, so  $C_{VAR}$  must undergo a charge-constrained phase every cycle to keep up. Although viable, the basic problem here is that energy harvested during the charge-constrained phase does not charge the targeted battery. Including materials with a permanent charge such as electrets [30] and floating-charge electrodes [31] are better voltage references, but only at the expense of complicated assembly and fabrication processes. The proposed integrated circuit (IC) avoids an additional source

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by using the system's already-existing battery to constrain  $C_{VAR}$ 's voltage, driving  $i_{HARV}$  directly into the target battery without intervening microelectronics.

Charging the battery with ambient energy still requires monitoring, control, and precharge circuits that demand power to function. This paper presents how a voltage-constrained electrostatic energy-harvester system IC prototype is able to operate with low enough energy to produce a net energy gain. To this end, Sections II and III describe the proposed energy-harvesting scheme and accompanying system, while Section IV explains the design details of the IC. Sections V and VI then show and evaluate the experimental results obtained, drawing relevant conclusions in Section VII.

## II. ENERGY-HARVESTING SCHEME

As the battery clamps and holds  $C_{VAR}$ 's voltage  $v_C$ , vibrations work against its electrostatic force to separate its plates, decreasing  $C_{VAR}$  from maximum  $C_{MAX}$  to minimum  $C_{MIN}$ , and converting kinetic energy to electrical in the form of  $i_{HARV}$ . Before connecting  $C_{VAR}$  to the battery, the system must precharge  $C_{VAR}$  to battery voltage  $V_{BAT}$  to avoid incurring considerable Ohmic conduction losses in the connecting switch, as a significant voltage would otherwise exist across the conducting switch that would dissipate much of the energy harvested [32]. An ideal (i.e., quasi-lossless) precharge block, on the other hand, transfers enough energy to ensure  $v_C$  at  $C_{MAX}$  reaches  $V_{BAT}$ , resulting in a theoretical energy investment  $E_{INV}$  from the battery that is equivalent to

$$E_{INV} = \frac{1}{2} C_{MAX} V_{BAT}^2. \quad (2)$$

After connecting  $C_{VAR}$  to the battery, as shown in the Harvest phase of Fig. 1,  $C_{VAR}$  decreases in response to vibrations, charging the battery with  $i_{HARV}$  and augmenting its energy by  $E_{HARV}$ :

$$E_{HARV} = \int V_{BAT} i_{HARV}(t) dt = \Delta C_{VAR} V_{BAT}^2. \quad (3)$$

After reaching  $C_{MIN}$ , the IC disconnects  $C_{VAR}$  from the battery to avoid the reverse process (current) from discharging the battery. At this point, energy remains in  $C_{VAR}$  but its value is so low that attempting to recover it with another precharge-like energy-transfer process dissipates most of what remains. Instead, the IC leaves  $C_{VAR}$  open-circuited (i.e., under charge-constrained conditions) in the Reset phase (Fig. 1) so that as vibrations push the capacitor plates together and  $C_{VAR}$  increases,  $v_C$  decreases and resets to a lower value. When  $C_{VAR}$  reaches  $C_{MAX}$ , the IC again precharges  $C_{VAR}$  and the process repeats. Since harvested energy  $E_{HARV}$  surpasses  $E_{INV}$ , the energy in the battery increases with each cycle by an ideal net energy gain  $E_{NET}$ :

$$\begin{aligned} E_{NET} &= E_{HARV} - E_{INV} \\ &= \left( \frac{1}{2} C_{MAX} - C_{MIN} \right) V_{BAT}^2. \end{aligned} \quad (4)$$

In practice,  $E_{HARV}$  must overcome not only precharge investment  $E_{INV}$  but also the losses associated with each phase in the cycle. This is a considerable challenge because  $E_{HARV}$

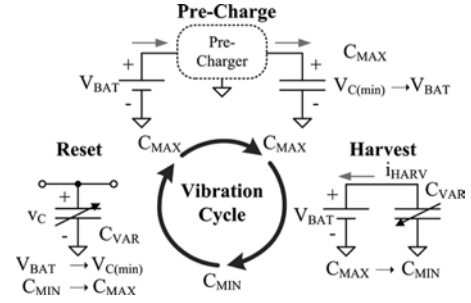


Fig. 1. Energy-harvesting phases in the prototyped system: precharge, harvest, and reset.

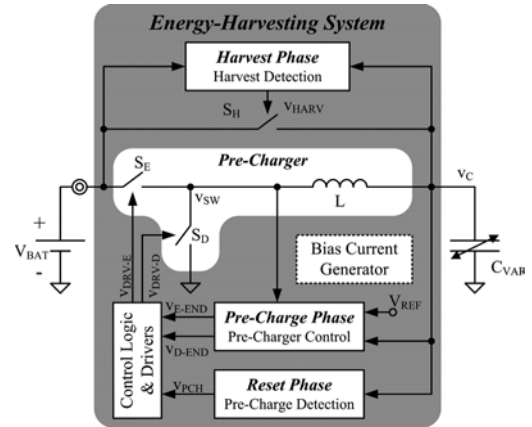


Fig. 2. Proposed energy-harvesting system.

is low to begin with and each phase requires monitoring and control circuitry to detect  $C_{MAX}$  during reset to initiate the precharge phase and  $C_{MIN}$  to disconnect  $C_{VAR}$  from the battery at the end of the harvesting phase. To mitigate these losses, the proposed system employs low-energy strategies such as operating with subthreshold currents and shutting off unused components, but not without carefully comprehending the low-bandwidth and startup implications of such actions.

## III. PROPOSED ENERGY HARVESTER SYSTEM

The proposed IC coordinates each phase in the energy-harvesting cycle by (i) detecting  $C_{MAX}$  during reset, (ii) precharging  $C_{VAR}$ , (iii) connecting  $C_{VAR}$  to the battery to allow vibrations to drive  $i_{HARV}$  into the battery, (iv) detecting  $C_{MIN}$  during the harvesting phase, and (v) disconnecting  $C_{VAR}$  from everything during reset. Each functional block in the system (Fig. 2) corresponds to a phase in the process that the digital controller enables and powers in sequence, one at a time as each phase occurs. For instance, the precharge detection block monitors when  $C_{VAR}$  reaches  $C_{MAX}$  during reset to trigger the next phase in the cycle: precharge. During precharge, the detection circuits shut off and the IC charges  $C_{VAR}$  to  $V_{BAT}$ . Afterwards, the precharger circuits shut off, prompting harvest switch  $S_H$  to connect  $C_{VAR}$  to  $V_{BAT}$ . During the ensuing phase, the controller powers the harvest detection circuits so they monitor when  $C_{VAR}$  reaches  $C_{MIN}$ , after which  $C_{VAR}$  resets and the controller again enables the precharger, allowing the cycle to repeat as vibrations swing  $C_{VAR}$  between  $C_{MAX}$  and  $C_{MIN}$ .

To start, the quasi-lossless inductor-based switching circuit in Fig. 2 transfers  $E_{INV}$  from the battery to charge  $C_{VAR}$  to  $V_{BAT}$ . To this end, the battery energizes both L and  $C_{VAR}$  with  $E_{INV}$  when closing energizing switch  $S_E$ . Once done, opening  $S_E$  and closing de-energizing switch  $S_D$  connects switching node  $v_{SW}$  to ground and de-energizes L into  $C_{VAR}$ . After  $C_{VAR}$  absorbs and exhausts L's energy, capacitor voltage  $v_C$  reaches  $V_{BAT}$  and  $S_D$  disengages, which is when the precharge phase terminates. Note that fully draining L and allowing its current  $i_L$  to remain at zero for a finite fraction of the vibration period is analogous to operating L in discontinuous-conduction mode (DCM), when referring to switching converters. Also notice the reason the circuit is quasi-lossless is because L allows the voltages across the switches to remain low (in the mV range) while they conduct  $i_L$ . As in buck converters, an asynchronous diode could replace  $S_D$ , but only at the expense of higher conduction losses because a diode drops roughly 0.7 V when conducting current.

Ideally, to charge  $C_{VAR}$  to  $V_{BAT}$ , the battery should energize L and  $C_{VAR}$  for 1/6 of their natural frequency, which corresponds to charging  $C_{VAR}$  during the energizing phase to  $0.5 V_{BAT}$  [32]. In practice, however, power losses across the system, delays, and other non-idealities (when energizing and de-energizing L) dissipate a portion of  $E_{INV}$ , which means  $C_{VAR}$ 's energizing target voltage must exceed  $0.5 V_{BAT}$  to compensate for these losses. In other words, actual  $E_{INV}$  must exceed its theoretical lower bound. Then, after fully de-energizing L into  $C_{VAR}$  (when  $i_L$  approaches zero),  $S_D$  shuts off to avoid discharging  $C_{VAR}$ . Note the precharge phase only lasts a small fraction of the vibration period (about 100–200 ns of 0.01–1 s) [14], which means  $C_{VAR}$ 's vibration-induced variation, as perceived by the precharger, is slow enough to seem constant near  $C_{MAX}$ .

After precharge, the IC connects  $C_{VAR}$  to the battery and vibrations decrease  $C_{VAR}$  and generate  $i_{HARV}$ , which charges the battery. The controller disconnects  $C_{VAR}$  once it reaches  $C_{MIN}$  because  $i_{HARV}$  in reverse would otherwise discharge the battery. Due to the intrinsic resistance of the connecting switch ( $S_H$ ),  $i_{HARV}$  induces a voltage drop that forces  $C_{VAR}$  to raise its voltage  $v_C$  slightly above  $V_{BAT}$  during the harvesting phase. The harvest-detection block then monitors  $v_C$  and prompts  $S_H$  to disengage when  $v_C$  drops to  $V_{BAT}$ , which happens when  $i_{HARV}$  decreases to zero, that is, when  $C_{VAR}$  reaches  $C_{MIN}$ . Although a diode would engage and disengage automatically with  $i_{HARV}$  (asynchronously), its forward voltage drop requires a brief charge-constrained phase as  $v_C$  increases a diode voltage above  $V_{BAT}$ , resulting in energy losses [32]. Using synchronous switch  $S_H$  is more efficient than a diode as long as its control circuitry consumes less power than the diode's. For optimal results, nAs bias the harvesting detection block in subthreshold and the system's control logic enables it only during the harvesting phase, which is half the vibration cycle.

After harvesting, the IC disconnects  $C_{VAR}$  and leaves it open-circuited during the reset phase so  $v_C$  can decrease automatically when  $C_{VAR}$  increases. During this phase, the precharge detector indirectly senses  $C_{VAR}$  and detects when it reaches  $C_{MAX}$ . Because  $v_C$  decreases with increasing  $C_{VAR}$ ,  $v_C$  begins to increase after  $C_{VAR}$  reaches  $C_{MAX}$  and starts

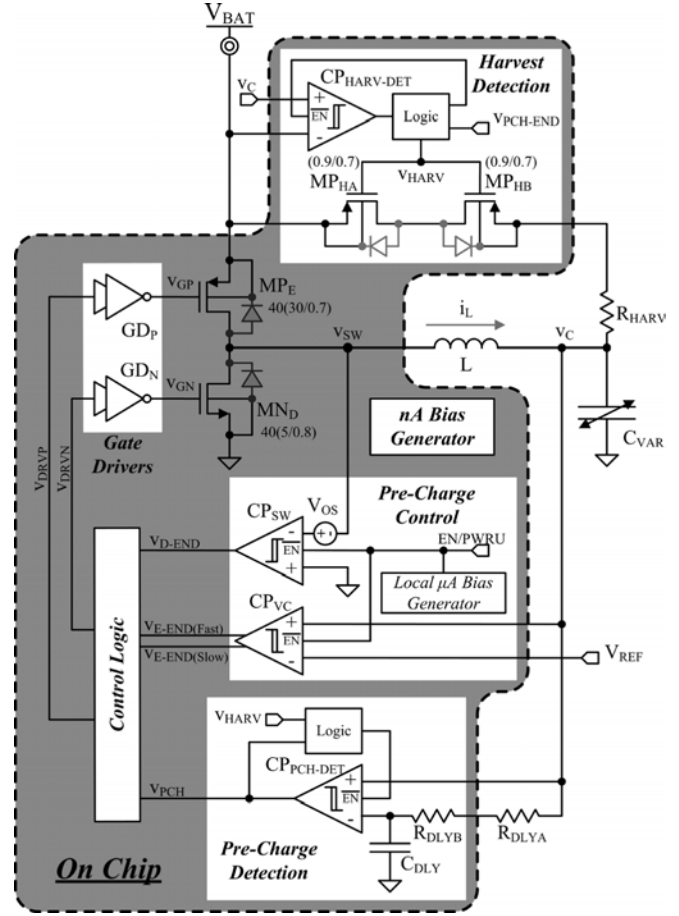


Fig. 3. Prototyped energy harvester (transistor dimensions are in  $\mu\text{m}$ ).

to decrease, which means minimum capacitor voltage  $V_{C(\min)}$  corresponds to when  $C_{VAR}$  is at  $C_{MAX}$ . In this way, the IC uses the remnant energy left in  $C_{VAR}$  after the harvesting phase to detect  $C_{MAX}$ , which the system would otherwise lose. Like the harvesting counterpart, subthreshold currents bias the precharge detector and it only engages during reset, which is half the vibration cycle.

#### IV. ENERGY HARVESTER IC PROTOTYPE

The harvesting system (Fig. 3) integrates all blocks into a single silicon IC, with the exception of L,  $C_{VAR}$ , and the current-setting resistors of the nA bias-current generator. Resistors  $R_{DLYA}$  and  $R_{HARV}$  are off chip for testability purposes only, to freely adjust their values when experimenting with the IC. Similarly, the IC relied on off-chip reference voltage  $V_{REF}$  to modify the pre-charging target voltage easily during experiments, optimum values of which depend on the losses across the system.

##### A. Precharger

$MP_E$  and  $MN_D$  in Fig. 4 and their inverting drivers energize and de-energize L to charge  $C_{VAR}$  to  $V_{BAT}$ . As L and  $C_{VAR}$  energize, comparator  $CP_{VC}$  senses  $v_C$  until it reaches  $V_{REF}$ , at which point  $CP_{VC}$  opens  $MP_E$  and, after a dead period during which time both switches remain off,  $MN_D$  closes to de-energize L. L's de-energizing current  $i_L$  then flows to  $v_C$  through

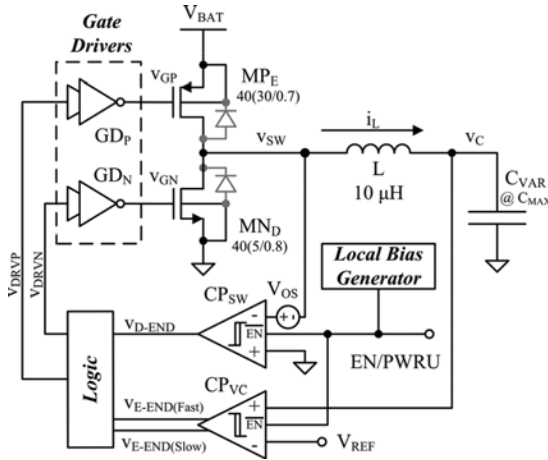


Fig. 4. Precharger circuit (transistor dimensions are in  $\mu\text{m}$ ).

$MN_D$ , causing  $v_{SW}$  to fall slightly below 0 V until  $i_L$  falls to 0 A.  $CP_{SW}$  senses when  $i_L$  reaches 0 A indirectly by monitoring when  $v_{SW}$  rises to 0 V, which indicates the end of the de-energizing step and the precharge phase.

$CP_{SW}$ 's delay, however, would keep  $MN_D$  engaged long enough to discharge  $C_{VAR}$ , had not a built-in offset voltage  $V_{OS}$  been included. The offset shifts the trip point so that  $CP_{SW}$  starts tripping just before  $v_{SW}$  reaches 0 V, relying on its delay for its output to transition when  $v_{SW}$  actually nears 0 V. Before either  $CP_{VC}$  or  $CP_{SW}$  becomes functional, however, the first step in the precharge process is to power their local bias-current generator. Once the bias is ready,  $MP_E$  closes and the generator powers both comparators, but only enables  $CP_{VC}$ , forcing  $CP_{SW}$  to remain high until the start of the de-energizing step. Note precharge only occurs during a diminutive fraction of the entire cycle (e.g., 200 ns of 33 ms) so all precharge circuits must be sufficiently fast, which means transistors in  $CP_{VC}$  and  $CP_{SW}$  must operate in strong inversion. Even so, because their currents only flow during precharge, they do not represent a significant energy loss.

As mentioned,  $CP_{VC}$  signals the end of the energizing step when  $v_C$  reaches  $V_{REF}$ .  $CP_{VC}$  (Fig. 5) uses an n-type input pair with a p-type load mirror to feed a common-source (CS) transistor and subsequently drive a digital inverter. High-impedance cascode current sources bias each gain stage and all the nMOS and pMOS bulks connect to 0 V and  $V_{BAT}$ , respectively, unless otherwise specified. CS  $MP_2$  further amplifies the signal from the first stage to decrease shoot-through (short-circuit) current in the ensuing inverters because a steeper transition decreases the time pull-up and -down transistors conduct simultaneously. Switch  $MN_H$  sinks additional current from the current mirror when  $v_{O2}$  is high to establish hysteresis. The differential pair features minimum channel lengths to keep delays short, even at the expense of accuracy, given adjustments in  $V_{REF}$  can compensate for offsets. The comparator generates fast and slow outputs  $v_{E-END(Fast)}$  and  $v_{E-END(Slow)}$  to create dead time between the energizing and de-energizing steps, which would otherwise produce shoot-through (short-circuit) current. When  $CP_{VC}$  trips high, for example,  $v_{E-END(Fast)}$  first opens  $MP_E$  to end the energizing step and, after the short delay  $R_{SL}$  and

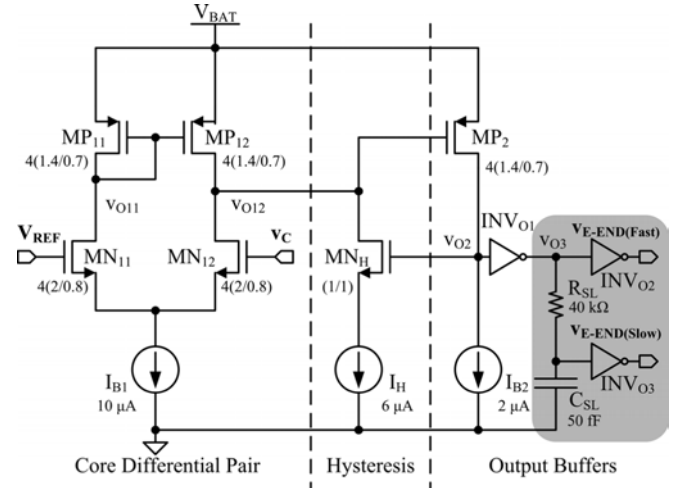


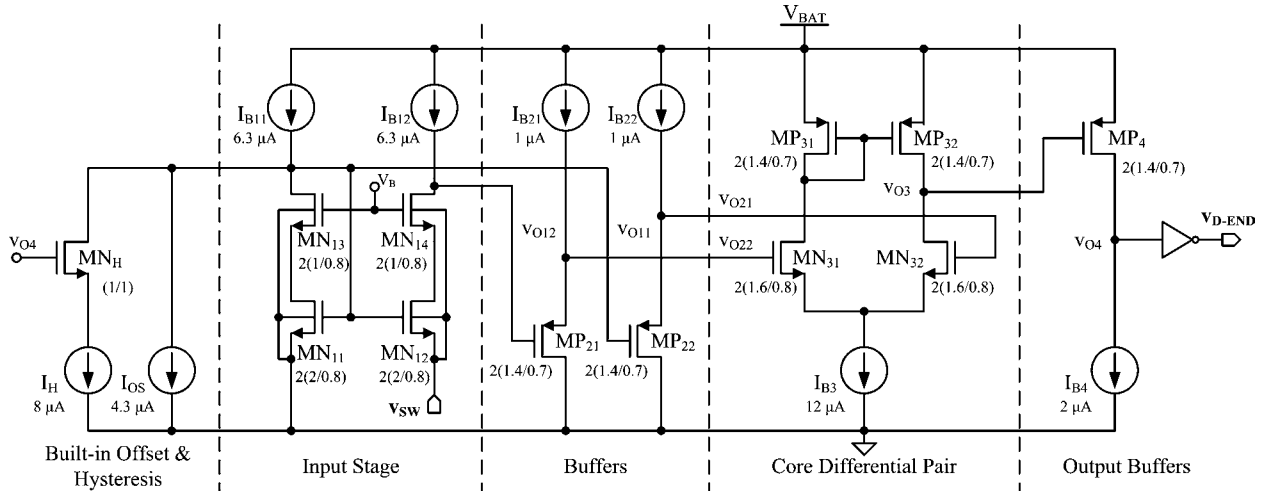
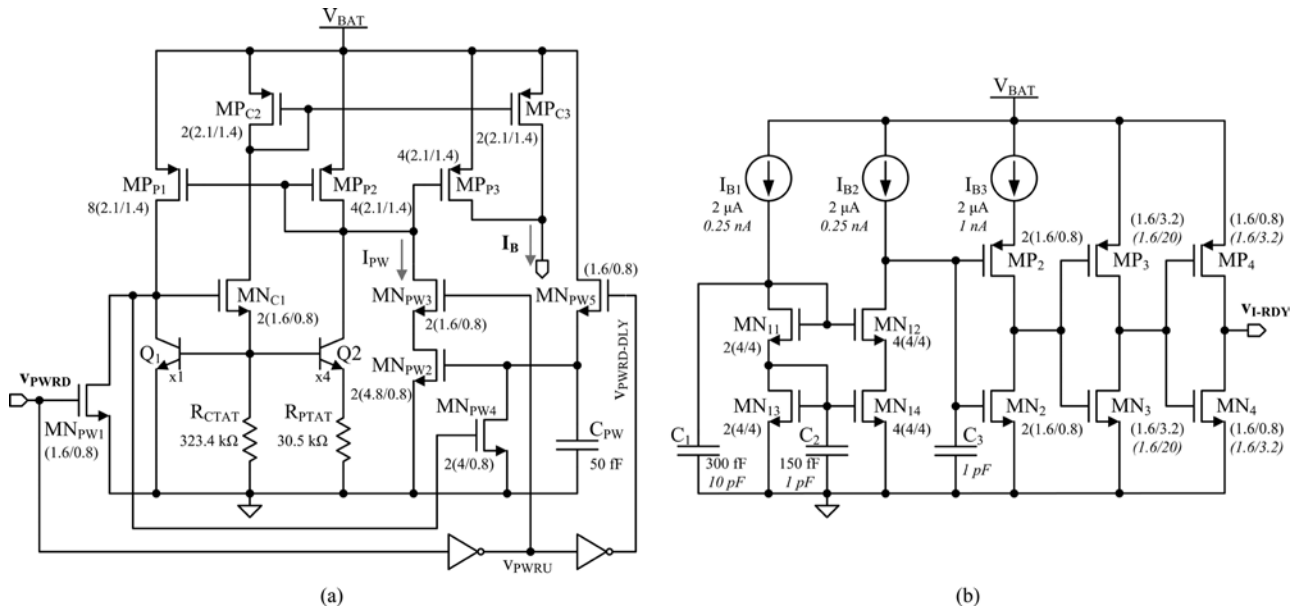
Fig. 5. Precharge energize comparator  $CP_{VC}$  (transistor dimensions are in  $\mu\text{m}$ ).

$C_{SL}$  produce,  $v_{E-END(Slow)}$  closes  $MN_D$  to start the de-energizing counterpart and enables  $CP_{SW}$ . Note only one decision in  $CP_{VC}$  (as in the other comparators) matters: when its output transitions high. For this reason, class-A  $MP_2$ 's sourcing current sets this high-speed transition and bias  $I_{B2}$  slews the other.

$CP_{SW}$ 's input stage (in Fig. 6) monitors voltages near and below 0 V with a common-gate, gate-coupled nMOS differential pair. pMOS source followers then level-shift the signal higher above 0 V to drive an nMOS differential pair, whose output drives CS pMOS amplifier  $MP_4$ . Offset current  $I_{OS}$  establishes a systematic imbalance that produces input-referred offset  $V_{OS}$  in  $CP_{SW}$ . Similarly, switch  $MN_H$  steers offset current  $I_H$  only when output  $v_{O4}$  is high to establish hysteresis so  $CP_{SW}$  cannot trip again until  $v_{SW}$  is well below 0 V. The bulks of the input NFETs are connected to their respective sources to prevent  $v_{SW}$ , which swings below 0 V, from inducing considerable substrate current through  $MN_{12}$ 's body diode. The systematic offset  $I_{OS}$  is, by design, large enough to overwhelm the random offset that results from placing  $MN_{11}$  and  $MN_{12}$  in separate p-type isolation tanks. Recall that at this point in the cycle, after  $i_L$  drops to 0 A,  $CP_{SW}$  trips low and signals the end of the de-energizing step and precharge phase, allowing the harvesting phase to begin while shutting all precharge circuits off and returning them to their previous states.

To generate the bias currents  $CP_{VC}$  and  $CP_{SW}$  require, the precharge block features its own local bias block. The circuit, shown in Fig. 7(a), creates a first-order temperature-compensated (bandgap-like) current  $I_B$  by combining  $MP_{P3}$ 's proportional-to-absolute-temperature (PTAT) current with  $MP_{C3}$ 's base-emitter defined current (i.e., complementary-to-absolute-temperature CTAT). The base-emitter voltage difference between NPN pair  $Q_1 - Q_2$ , which the circuit impresses across  $R_{PTAT}$ , is PTAT so  $R_{PTAT}$ 's current is also PTAT (when  $R_{PTAT}$ 's temperature coefficient is low). Similarly, impressing  $Q_1$ 's base-emitter voltage across  $R_{CTAT}$  induces a CTAT current through  $R_{CTAT}$ .

The control logic only powers and enables the current generator during the precharge phase, which again, is a


 Fig. 6. Precharge de-energize comparator  $CP_{SW}$  (transistor dimensions are in  $\mu\text{m}$ ).

 Fig. 7. (a) Precharger bias-current generator and (b) its ready-state recognition circuit (italic values correspond to the nano-ampere bias generator and dimensions are in  $\mu\text{m}$ ).

miniscule fraction of the vibration cycle. When power-down signal  $v_{PWRD}$  is high, the generator is off because  $MN_{C1}$  pulls  $Q_1 - Q_2$ 's base terminals to 0 V, keeping  $R_{PTAT}$  and  $R_{CTAT}$ 's currents at 0 A. In addition,  $v_{PWRD}$  engages  $MN_{PW5}$  to charge and initialize  $C_{PW}$  to a "threshold" voltage below  $V_{BAT}$  ( $MN_{PW4}$  is off). The purpose of precharging  $C_{PW}$  (at the gate of  $MN_{PW2}$ ) is to momentarily prompt a startup response by pulling current  $I_{PW}$  from PTAT mirror  $MP_{P1} - MP_{P2}$ . In other words, when  $v_{PWRD}$  first transitions low to power the circuit,  $MN_{PW3}$  engages and  $C_{PW}$ 's initial voltage induces  $MN_{PW2}$  to sink considerable current ( $I_{PW}$ ), but only until the circuit "starts," after which point  $MN_{PW4}$  discharges  $C_{PW}$  and shuts  $MN_{PW2}$  off [33]. Note that even though increasing  $I_{PW}$  accelerates the startup time, quiescent losses in the circuit remain the same since no quiescent current flows through the startup circuit before or after it powers, unlike conventional techniques [33]. To allow the bias generator to

settle to its steady state, the monitor circuit in Fig. 7(b) only signals the system the current generator is ready when a delayed version (by  $C_1 - C_2$ ) of the current generated in Fig. 7(a) is able to discharge  $C_3$  sufficiently to trip current-limited inverter  $MN_2 - MP_2$ .

The digital control logic (Fig. 8) synchronizes the energizing and de-energizing steps in the precharge phase. More specifically,  $v_{PCH}$  from the precharge detector prompts the system to commence precharge by signaling the current generator to start (when  $v_{PWRD}$  is low). Once the generator is ready,  $v_{I-RDY}$  transitions high and forces PMOS-gate signal  $v_{G_P}$  to close  $MP_E$ . When the energizing step ends,  $CP_{VC}$ 's fast output  $v_{E-END(Fast)}$  shuts  $MP_E$  off and slower output  $v_{E-END(Slow)}$ , after a short delay, engages  $MN_D$  and sets latch  $SR_{SW}$  with NMOS-gate signal  $v_{G_N}$ , where  $SR_{SW}$ 's output enables  $CP_{SW}$ . Tripping  $CP_{SW}$ 's output  $v_{D-END}$  low forces  $v_{G_N}$  low, which opens  $MN_D$ . Signals



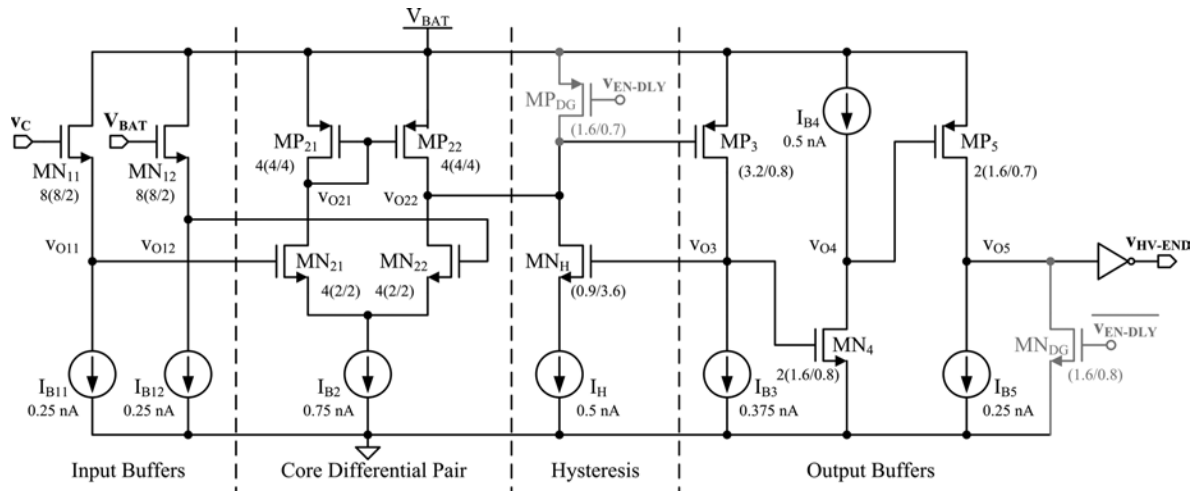
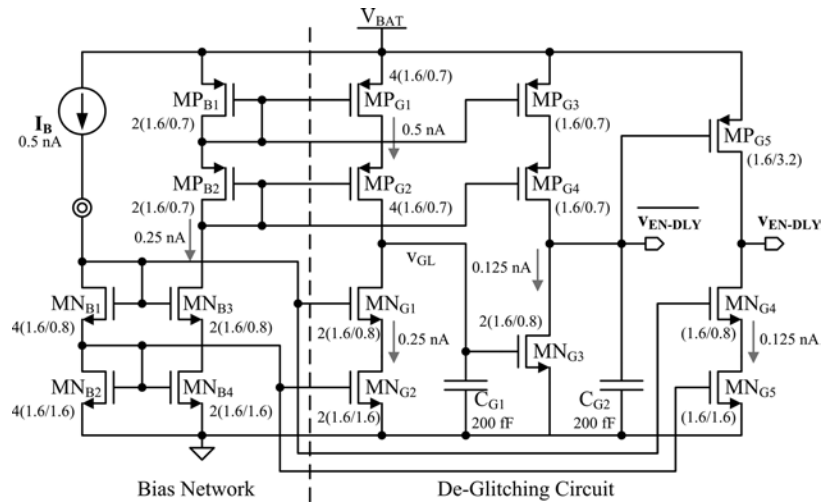
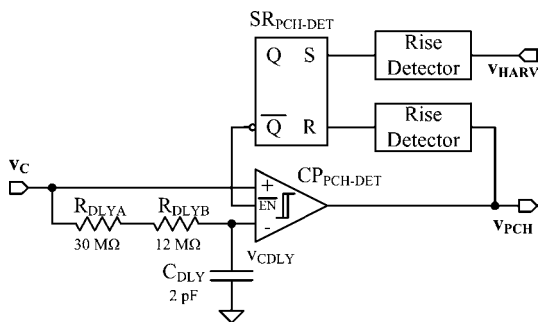

 Fig. 11. Harvest-Detect comparator  $CP_{HARV-DET}$  (transistor dimensions are in  $\mu\text{m}$ ).

 Fig. 12. Comparator  $CP_{HARV-DET}$ 's de-glitch circuit (transistor dimensions are in  $\mu\text{m}$ ).


Fig. 13. Precharge detection subsystem.

signaling  $C_{VAR}$  is ready for precharge. The challenge is typical vibration frequencies are in the 1–100 Hz range [14], and generating a discernable voltage across  $CP_{PCH-DET}$  requires a substantial delay between  $v_C$  and  $v_{CDLY}$ . Additionally, delay resistors dissipate energy proportional to the energy transferred to delay poly-poly capacitor  $C_{DLY}$ , which represents an over-investment. For this reason,  $C_{DLY}$  is low

at 2 pF, and to generate the delay necessary to detect  $V_{C(\min)}$  at 30 Hz,  $R_{DLY}$  is 42 M $\Omega$ . Of the 42 M $\Omega$ , 12 M $\Omega$  are on chip as  $R_{DLYB}$  in a “very-high sheet-resistivity” polysilicon strip and, for testing flexibility, 30 M $\Omega$  are off chip as  $R_{DLYA}$  in a thick-film resistor.  $R_{DLYB}$  occupied  $90 \times 120 \mu\text{m}^2$  of silicon area so integrating the remainder would have demanded  $360 \times 110 \mu\text{m}^2$ . To save area, substituting  $R_{DLY}$  with a subthreshold-operated transconductor is possible, but at the expense of additional power losses and design complexity.

To conserve energy, the circuit only powers  $CP_{PCH-DET}$  during reset. Digital signal  $v_{HARV}$ , which controls harvesting pMOS switch  $MP_H$  (in Fig. 3), transitions high to (i) disconnect  $C_{VAR}$  from the battery at the end of the harvesting phase (when  $C_{VAR}$  reaches  $C_{MIN}$ ) and (ii) set the set-reset (SR) latch of the precharge detector on its rising edge. The inverted output of the latch then powers and enables  $CP_{PCH-DET}$ , whose output  $v_{PCH}$  remains low (because disabling  $CP_{PCH-DET}$  forces  $v_{PCH}$  low) until  $v_C$  begins to increase. Once  $CP_{PCH-DET}$  trips, the rising edge of  $v_{PCH}$  resets the latch, whose output subsequently disables  $CP_{PCH-DET}$  and starts the precharge phase.

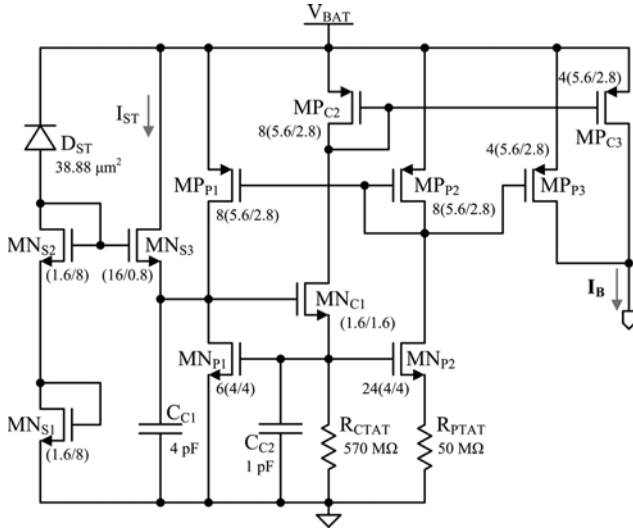


Fig. 14. Nano-ampere bias-current generator (transistor dimensions are in  $\mu\text{m}$ ).

Similar to the harvest-detect comparator,  $CP_{PCH-DET}$  conserves energy by powering for roughly each half cycle during reset and biasing with subthreshold currents. Its topology is similar to  $CP_{VC}$  (Fig. 5) but without  $RC$  delay and a pMOS input pair to detect  $v_C$  as it drops during reset. Hysteresis is included to filter noise jitter that would otherwise result when  $v_C$  and  $v_{CDLY}$  cross slowly. As a result,  $v_C$  must fall below  $v_{CDLY}$  by another 100 mV before  $CP_{PCH-DET}$  can trip. A deglitch circuit, like in Fig. 12, delays enable signals. Once operational,  $CP_{PCH-DET}$  initiates precharge when  $C_{VAR}$  reaches  $C_{MAX}$  and disables itself afterwards until the onset of the next cycle.

#### D. nA Generator

Subthreshold currents generated by the circuit in Fig. 14 bias the precharge and harvest detection comparators. The gate-source voltage difference between subthreshold-operated MOSFETs  $MN_{P1} - MN_{P2}$  is PTAT so the current it induces across  $R_{PTAT}$  is also PTAT. Similarly, forcing  $MN_{P1}$ 's gate-source voltage across  $R_{CTAT}$  generates a CTAT current through  $R_{CTAT}$  and  $MP_{C3}$  that, when combined with  $MP_{P3}$ 's PTAT current, produces a first-order temperature-compensated (bandgap-like) current  $I_B$ . The main challenge here is low currents demand high resistances, which is why the circuit uses 50- and 570-M $\Omega$ ; off-chip thick-film resistors. Note that other subthreshold designs [34], [35] require lower resistances by only deriving current from a PTAT voltage (in the 50-mV range) rather than a CTAT voltage, which is around 500 mV, the purpose of which is to temperature-compensate bias currents and avoid higher currents (power) at high temperatures.

The nA generator starts with the system and is always operational because, when not biasing a circuit in one phase, it powers another. Therefore, to minimize energy losses, the startup circuit must either shut off completely during normal operation or sink a negligibly low current. With the latter, the small leakage current reverse-biased p<sup>+</sup>/n-well diode  $D_{ST}$  in Fig. 14 produces biases long-length diode-connected NMOSFETs  $MN_{S1} - MN_{S2}$  to establish a reference voltage

for  $MN_{S3}$ . The idea is for  $MN_{S3}$  to prevent PTAT transistors  $MN_{P1} - MN_{P2}$  from shutting off by sourcing current into  $C_{C1}$  when  $MN_{C1}$ 's gate voltage attempts to drop, which indicates the PTAT generator is liable to enter a zero-current state —  $C_{C1} - C_{C2}$  keep noise transients from inadvertently engaging  $MN_{S3}$ . Note  $MN_{C1}$ 's gate voltage is sufficiently high during normal operation to keep  $MN_{S3}$  off. Lastly, a monitor circuit like in Fig. 7(b) ascertains when the generator is ready to prompts the system to proceed with startup.

#### E. Startup

The harvesting system synchronizes to the variations in  $C_{VAR}$  by (i) waiting until its nA-current generator is ready and (ii) subsequently discharging (and initializing)  $C_{VAR}$  to 0 V; the precharger then charges  $C_{VAR}$ , irrespective of its value. If  $C_{VAR}$  happens to be decreasing, harvest-detect comparator  $CP_{HARV-DET}$  senses when  $C_{VAR}$  reaches  $C_{MIN}$  (when  $i_{HARV}$  is 0 A) and prompts (synchronizes) the system to cycle through the ensuing reset and precharge phases, even if the first cycle harnesses little to no energy. Conversely, if the system starts when  $C_{VAR}$  is increasing, a reverse harvesting current discharges the battery slightly while causing  $v_C$  to fall below  $V_{BAT}$ , which triggers  $CP_{HARV-DET}$  and forces (synchronizes) the system into a reset phase. In this way, after one or two irregular cycles, the system starts and synchronizes to  $C_{VAR}$ , irrespective of  $C_{VAR}$ 's initial value.

## V. EXPERIMENTAL RESULTS

The proposed harvester was integrated into the 0.7- $\mu\text{m}$  BiCMOS  $1 \times 1 \text{ mm}^2$  silicon die in Fig. 15(a), packaged in a 32-pin plastic quad-flat package (PQFP), and tested on the printed-circuit board (PCB) in Fig. 15(b). The IC includes the entire system (Fig. 3) except L,  $C_{VAR}$ , and for testing purposes, bias, delay, and sense resistors  $R_{PTAT} - R_{CTAT}$ ,  $R_{DLYA}$ , and  $R_{HARV}$ . These resistors were untrimmed, and their values were unchanged in all samples measured. No action was taken to improve accuracy because a 20% variation in  $R_{DLY}$  (according to simulations) corresponded to only 1.7% variation in detecting  $C_{MAX}$  and 20% variations in  $R_{PTAT}$  and  $R_{CTAT}$  had negligible impact on the total energy harvested (at most 4.7% change). However,  $CP_{PCH-DET}$  includes sufficient input-referred-offset and voltage-gain margin to accommodate the 20% voltage variation that results between its input terminals  $v_C$  and  $v_{CDLY}$ . The IC also incorporates test-only circuits such as pin-out digital buffers, extra test-mode logic, and redundant comparators. The  $2 \times 2 \times 1 \text{ mm}^3$  10- $\mu\text{H}$  Coilcraft EPL2010 inductor used introduced a maximum equivalent series resistance (ESR) of 1  $\Omega$ . The purpose of the prototyped  $10.16 \times 20.32 \text{ cm}^2$  ( $4 \times 8 \text{ in}^2$ ) and 0.125 kg  $C_{VAR}$  in Fig. 16(a) was to emulate a MEMS counterpart and test the system.

#### A. $C_{VAR}$

$C_{VAR}$  in Fig. 16(a) features a top plate of two  $10.16 \times 20.32 \times 0.013 \text{ cm}^3$  ( $4 \times 8 \times 0.005 \text{ in}^3$ ) 1095-spring steel sheets and a  $10.16 \times 20.32 \times 0.046 \text{ cm}^3$  ( $4 \times 8 \times 0.018 \text{ in}^3$ ) steel bottom plate. Three non-conducting nylon screws with separating 0.1 cm-thick nylon washers connect the plates across their centerline axis. Before testing the IC, the inverting op amp

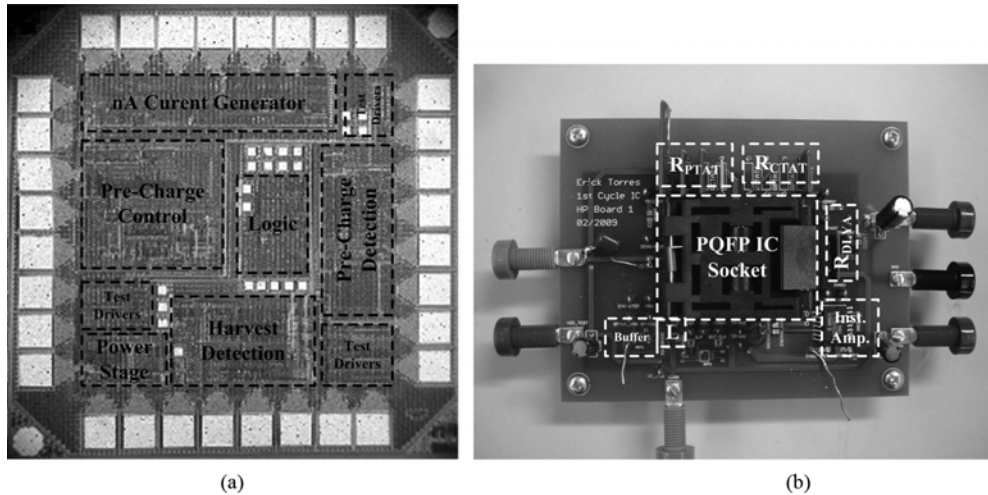


Fig. 15. (a) Die photograph of the  $1 \times 1 \text{ mm}^2$  energy-harvesting IC and (b) the printed-circuit board used to test it.

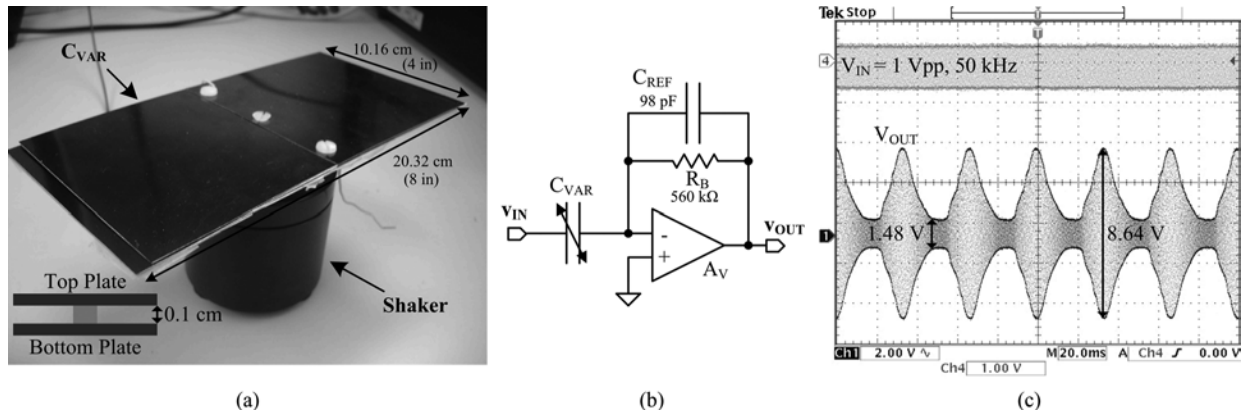


Fig. 16. (a) Vibration-driven variable capacitor prototype, (b) capacitance-sensing circuit, and (c) corresponding measurement results.

in Fig. 16(b) measures (via output  $v_{\text{OUT}}$ )  $C_{\text{VAR}}$  as it shakes by amplifying high-frequency input  $v_{\text{IN}}$  by  $C_{\text{VAR}}/C_{\text{REF}}$  [36] [Fig. 16(c)]. As a result, the gain across the circuit is a direct measure of  $C_{\text{VAR}}$ , when using a well-characterized reference capacitor  $C_{\text{REF}}$  (98 pF plus 14 pF from board parasitics). Ultimately, measurements show  $C_{\text{VAR}}$  resonates at 30 Hz and varies from 165.8 to 967.7 pF when shaken at the middle screw by a Brüel & Kjær 4810 vibration source with an acceleration of approximately  $70 \text{ m/s}^2$ . Note however that typical environments feature accelerations below  $12 \text{ m/s}^2$  [14].

### B. Harvest and Reset

A 100 V/V LTC1100 instrumentation amplifier with less than 0.075% of gain error and  $10 \mu\text{V}$  of offset measures  $i_{\text{HARV}}$  by sensing the voltage drop across  $R_{\text{HARV}}$  (100 k $\Omega$ ), but introduces about 25 pF of parasitic capacitance to  $C_{\text{VAR}}$ . Fig. 17 shows  $C_{\text{VAR}}$  generates up to 500 nA when using a battery at 3.5 V. As each harvesting phase ends,  $i_{\text{HARV}}$  reduces to 0 A and reset follows with  $C_{\text{VAR}}$ 's voltage  $v_{\text{C}}$  gradually dropping from its harvesting state of 3.5 V to a minimum [Fig. 17(a)]. Harvesting control signal  $v_{\text{HARV}}$  in Fig. 17(b) transitions accordingly, with a low state engaging  $MP_{\text{H}}$  to

connect  $C_{\text{VAR}}$  to the battery and a high state prompting the system to enter reset.

Current  $i_{\text{HARV}}$  represents (when integrated over time as it flows into the 3.5 V battery) an average gain of 11.11 nJ/cycle. The harvesting detector introduces a brief delay at the end of the harvesting phase that allows  $C_{\text{VAR}}$  to increase slightly while still connected to the battery, drawing a reverse current that discharges the battery by 342.64 pJ/cycle. The detector, which derives power from the 3.5 V battery and is active through the harvesting phase (about 20.0 ms/cycle on average), consumes a (measured) quiescent current  $I_{\text{Q}}$  of 2.30–3.32 nA, resulting in an average dissipation of 190.84 pJ/cycle. Similarly, the precharge detector draws a measured  $I_{\text{Q}}$  of 1.13–3.34 nA for the duration of the reset phase (approximately 13.3 ms/cycle on average), resulting in an average dissipation of roughly 94.53 pJ/cycle. The vibration period is on average 33.3 ms and its corresponding frequency is 30.0 Hz. The nA generator, which biases both detection blocks and remains operational through the entire period, sinks 3.22–3.72 nA from the 3.5 V supply, dissipating an average of 400.85 pJ/cycle. As Table I summarizes, the battery gains 10.58 nJ/cycle during harvesting, loses 94.53 pJ/cycle in reset, and loses another 400.85 pJ/cycle to the nA generator.

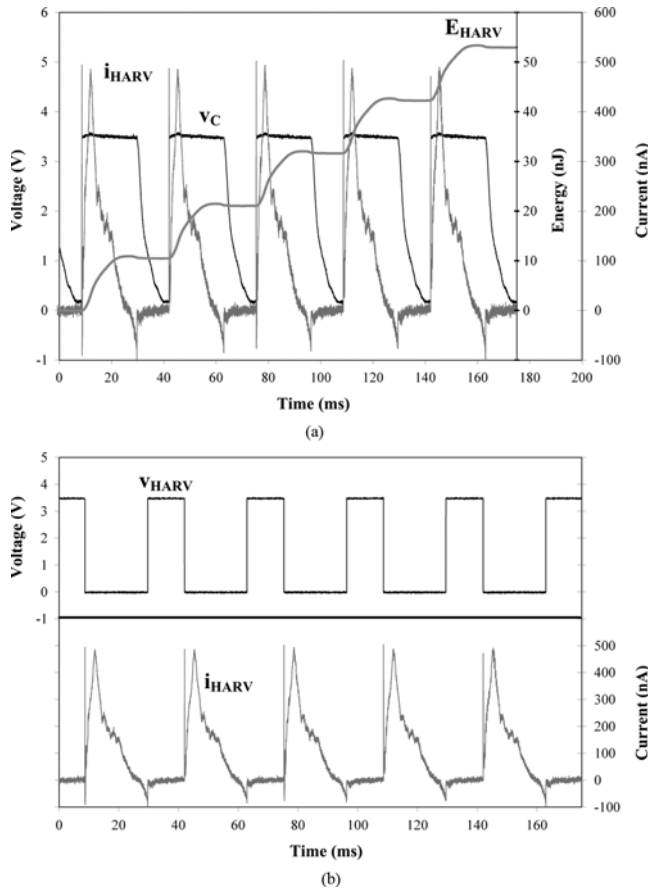


Fig. 17. Experimental measurements showing (a) variable capacitor voltage  $v_C$ , harvesting current  $i_{HARV}$ , extrapolated energy gain  $E_{HARV}$ , and (b) harvesting control signal  $v_{HARV}$  during five vibration cycles.

TABLE I  
MEASURED ENERGY CONSUMED AND GAINED BY THE PROTOTYPED HARVESTER SYSTEM

Phase		Measured Energy [nJ/cycle]		
		$V_{BAT} = 2.7$ V	$V_{BAT} = 3.5$ V	$V_{BAT} = 4.2$ V
Harvest Phase	Harvested Energy	+7.047	+11.114	+15.177
	Reverse Energy	-0.233	-0.343	-0.398
	Control Dissipation	-0.148	-0.191	-0.230
Reset Phase	Control Dissipation	-0.069	-0.095	-0.120
Pre-Charge Phase	Invested Energy	-5.629	-9.027	-13.005
	Returned Energy	+0.353	+0.662	+1.320
	Sense Resistor	+0.304	+0.485	+0.681
	Control Circuits	-0.048	-0.064	-0.067
Nano-Ampere Current Generator		-0.304	-0.401	-0.489
Net Energy Gain		<u>+1.273 nJ/cycle</u>	<u>+2.140 nJ/cycle</u>	<u>+2.869 nJ/cycle</u>

### C. Precharge

$C_{VAR}$  charges from close to 0 V to its 3.5 V target [Fig. 17(a)] between every reset and harvesting phase.  $C_{VAR}$ 's voltage  $v_C$  first rises to roughly 3 V [Fig. 18(a)] when the system energizes L and  $C_{VAR}$  from the battery, as energizing switch  $MP_E$ 's low gate voltage  $v_{GP}$  from Fig. 18(b) induces switching voltage  $v_{SW}$  in Fig. 18(a) to remain high.  $v_C$  then reaches 3.5 V when the system de-energizes L into  $C_{VAR}$  (as de-energizing switch  $MN_D$ 's high gate voltage  $v_{GN}$  forces  $v_{SW}$  to stay low). The system introduces an average dead time between  $MP_E$  and  $MN_D$  conduction events of 1.86 ns.

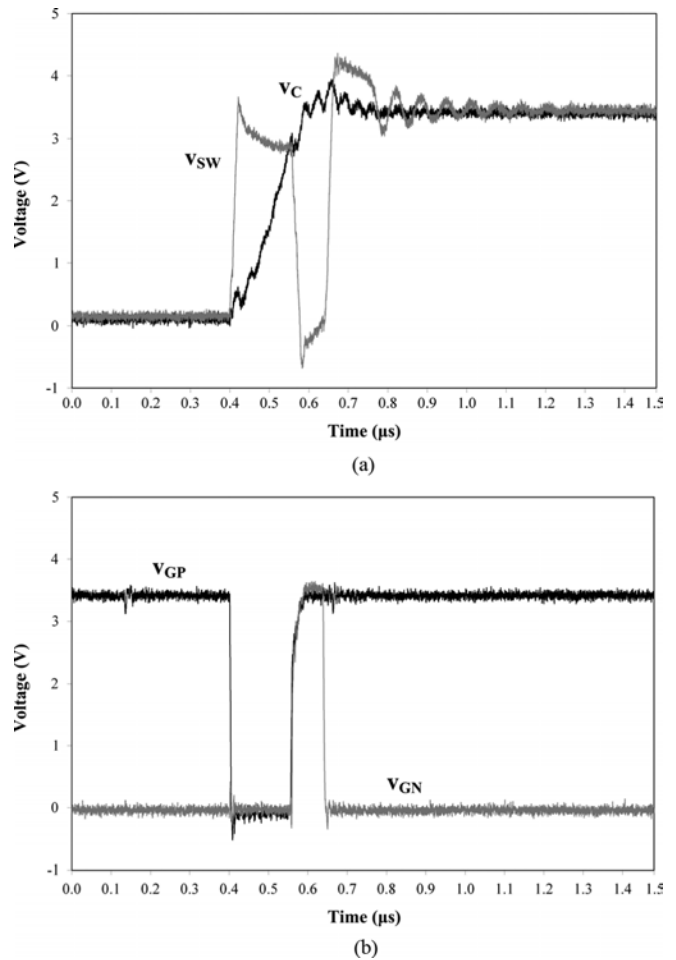


Fig. 18. Precharge waveforms showing (a) variable capacitor voltage  $v_C$  and switch-node voltage  $v_{SW}$  with corresponding (b) energize and de-energize gate-control signals  $v_{GN}$  and  $v_{GP}$ .

$V_{REF}$ , which sets  $v_C$ 's energizing target (and therefore the energizing time), was manually adjusted to ensure  $v_C$  reached  $V_{BAT}$  at the end of precharge. As before, although  $V_{REF}$  should in theory be  $0.5V_{BAT}$ , it was higher because the IC required more investment energy  $E_{INV}$  to compensate for the power lost in the circuit. As a result, because process and gradients across dice introduced parameter variations in the chips tested,  $V_{REF}$  varied between 2.5 and 2.8 V across prototyped ICs when tested at 3.5 V. In the end, the system energized L and  $C_{VAR}$  (on average) for about 155.44 ns, producing a peak inductor current of 23.34 mA (that subsequently dropped to 0 A -de-energized- in 79.23 ns) and an average end-of-precharge voltage of 3.79 V. Note switching node  $v_{SW}$  dropped to about  $-783$  mV and increased to 0 V during the de-energizing step. Also notice remnant energy in L and adjacent parasitic capacitors produced oscillations in  $v_{SW}$ , which the IC eventually dampened.

The IC raises precharge enable voltage  $v_{PCH}$  [Fig. 19(a)] when  $C_{VAR}$  reaches  $C_{MAX}$  to prompt the system to power the precharge current generator, which becomes fully functional after approximately 262.83 ns. Once biased, the logic initiates the energize/de-energize sequence (via gate-control signals  $v_{GP}$  and  $v_{GN}$  in Fig. 19(b) that subsequently charges  $C_{VAR}$  and powers both precharge comparators, enabling  $CP_{SW}$

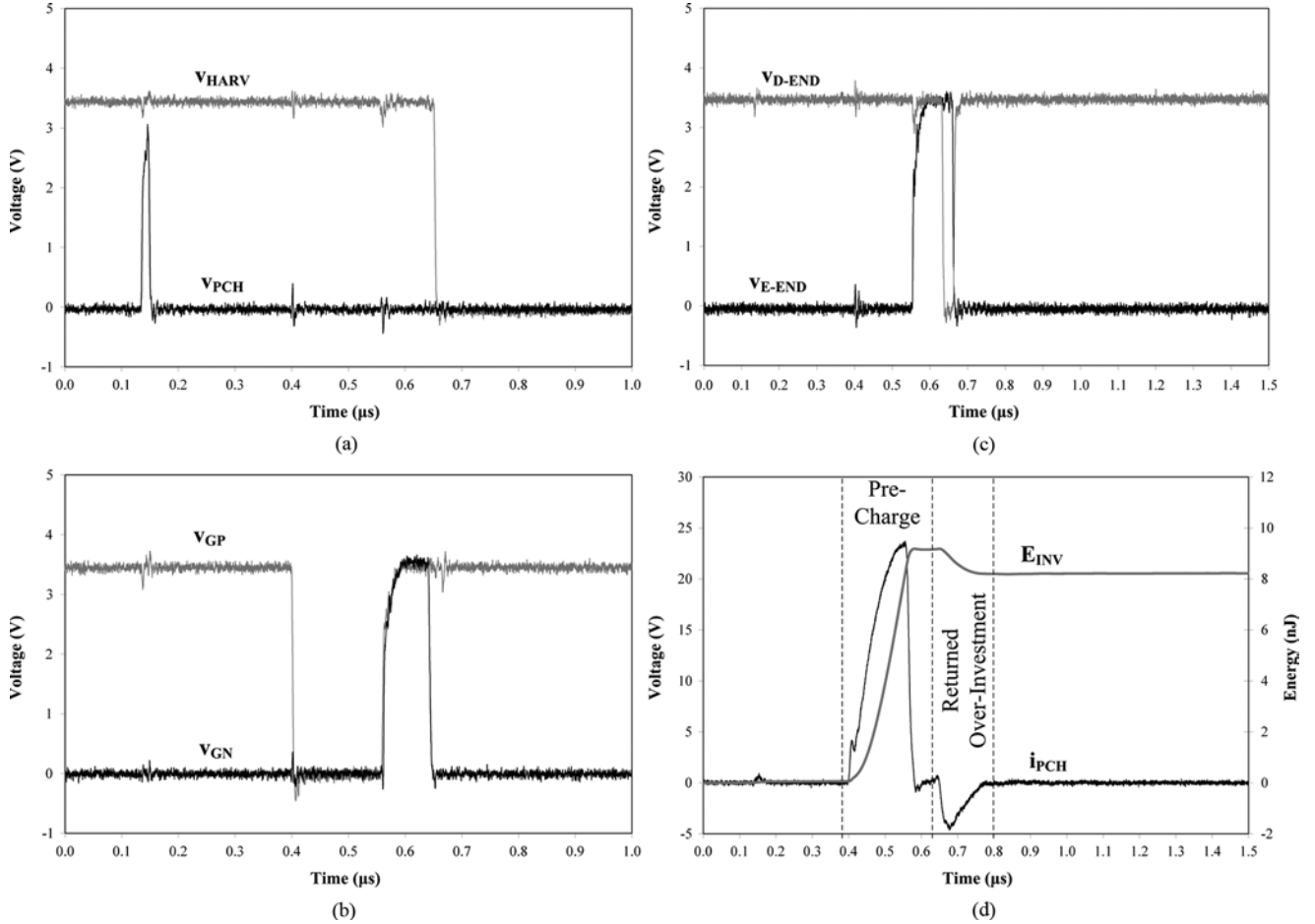


Fig. 19. (a) Precharge energize and de-energize control signals  $v_{CN}$  and  $v_{CP}$ , (b) onset of precharge phase signal  $v_{PCH}$ , and start of harvest phase signal  $v_{HARV}$ , (c)  $CP_{VC}$  and  $CP_{SW}$ 's outputs, (d) precharge current  $i_{PCH}$ , and extrapolated precharge investment energy  $E_{INV}$ .

only after the de-energize step begins. Both comparators and their current generator remain biased through the end of the pre-charge phase, marked by the fall of  $v_{HARV}$ . In the end, the current generator remains operational for about 499.63 ns, drawing 12.01–12.82  $\mu\text{A}$  from the 3.5 V battery and using approximately 21.62 pJ/cycle.

Energizing comparator  $CP_{VC}$ 's output  $v_{E-END}$  remains low until  $v_C$  reaches  $V_{REF}$  and de-energizing comparator  $CP_{SW}$ 's output  $v_{D-END}$  stays high until the end of the de-energizing step [Fig. 19(c)].  $CP_{VC}$  draws 22.13–24.91  $\mu\text{A}$  for about 141.29 ns while  $v_{E-END}$  is low and 29.33–34.62  $\mu\text{A}$  for an additional 95.51 ns until precharge ends. Similarly,  $CP_{SW}$  draws about 20.12–28.85  $\mu\text{A}$  while it holds  $v_{D-END}$  high (for 205.57 ns). Built-in input offset  $V_{OS}$ , which is 153.43 mV on average, causes  $CP_{SW}$  to trip low slightly before the de-energizing step ends, which allows  $CP_{SW}$  to draw 16.74–23.78  $\mu\text{A}$  for about 31.23 ns. In all,  $CP_{VC}$ ,  $CP_{SW}$ , and their bias generator together demand 63.65 pJ/cycle, of which  $CP_{VC}$  dissipates 22.16 pJ/cycle and  $CP_{SW}$  19.88 pJ/cycle.

The average energy the battery invested into the system to precharge  $C_{VAR}$  ( $E_{INV}$  in Fig. 19(d)) was 9.03 nJ/cycle (as measured from the battery current drawn through a series 10  $\Omega$  sense resistor). Recall  $E_{INV}$  includes the losses the logic switches and gate drivers in the IC incur during precharge. For a 3.5 V battery, for example,  $i_L$  increased (on average)

to 23.34 mA, overcharging  $C_{VAR}$  to 3.79 V. The additional 290 mV in  $C_{VAR}$  caused the system to return the over-invested energy to the battery at the beginning of every harvesting phase, which is why the battery receives an average of 662.02 pJ/cycle (i.e., as  $i_{PCH}$  peaks at  $-3.6$  mA and  $E_{INV}$  drops to roughly 8.37 nJ/cycle) when harvesting switch  $MP_H$  first closes. In all, the system invested 7.94 nJ/cycle. Note the budget in Table I adds the 485.04 pJ/cycle the 10  $\Omega$  sense resistor dissipated back because the only reason the system required this energy in the first place was to test it. (Table II summarizes the IC's experimental performance.)

#### D. Energy Gain

The total energy the system drew from vibrations in  $C_{VAR}$  exceeded all losses, producing a net positive gain of 2.14 nJ/cycle for a 3.5 V battery, which is equivalent to 64.2 nW at 30 Hz. The system also produced gains of 1.27 and 2.87 nJ/cycle at 2.7 and 4.2 V, which represents the operating range of typical Li Ions [7]. Fig. 20 illustrates how this gain charged 1  $\mu\text{F}$  ( $C_{BAT}$ ), which emulates a microscale battery, from 3.5 to 3.81 V in 35.16 s when setting  $V_{REF}$  to 2.8 V. Note a real battery (e.g., a 1 mAh thin-film Li Ion) has substantially higher capacity than 1  $\mu\text{F}$  and its charging rate is considerably slower. As  $C_{BAT}$ 's voltage increases,  $C_{VAR}$  should precharge to an increasingly higher level, demanding  $V_{REF}$  to increase

TABLE II  
IC PERFORMANCE SUMMARY

Die Information			$1 \times 1 \text{ mm}^2$ 0.7- $\mu\text{m}$ BiCMOS Chip		
Number of Transistors			799 Transistors		
$V_{BAT}$ Range			2.7 V	3.5 V	4.2 V
Pre-Charge Control	CP <sub>VC</sub>	$I_Q$ , High Output	27.8-32.9 $\mu\text{A}$	29.3-34.6 $\mu\text{A}$	30.5-35.8 $\mu\text{A}$
		$I_Q$ , Low Output	21.0-23.7 $\mu\text{A}$	22.1-24.9 $\mu\text{A}$	23.0-25.8 $\mu\text{A}$
	$t_{ON,AVG}$ (High/Low) Avg. $ V_{OS} $	105.5/136.3 ns 54.7 mV	95.5/141.3 ns 57.0 mV	63.3/147.7 ns 63.6 mV	
CP <sub>SW</sub>	$I_Q$ , High Output	16.9-24.2 $\mu\text{A}$	20.1-28.9 $\mu\text{A}$	22.2-32.0 $\mu\text{A}$	
	$I_Q$ , Low Output	13.8-19.9 $\mu\text{A}$	16.7-23.8 $\mu\text{A}$	18.7-25.9 $\mu\text{A}$	
$t_{ON,AVG}$ (High/Low) Avg. $ V_{OS} $	199.1/42.6 ns 186.6 mV	205.6/31.2 ns 153.4 mV	185.1/25.9 ns 142.1 mV		
Local $\mu\text{A}$ Bias	$I_Q$ $t_{ON,AVG}$	11.5-12.3 $\mu\text{A}$ 562.5 ns	12.0-12.8 $\mu\text{A}$ 499.6 ns	12.4-13.2 $\mu\text{A}$ 376.2 ns	
Harvest Detection	CP <sub>HARV-DET</sub>	$I_Q$	2.3-3.3 nA	2.3-3.3 nA	2.4-3.4 nA
		$t_{ON,AVG}$ Avg. $ V_{OS} $	20.5 ms 8.3 mV	20.0 ms 7.4 mV	19.7 ms 7.1 mV
Pre-Charge Detection	CP <sub>PCH-DET</sub>	$I_Q$	1.1-3.2 nA	1.1-3.3 nA	1.2-3.4 nA
		$t_{ON,AVG}$ Avg. $ V_{OS} $	12.9 ms 5.6 mV	13.3 ms 3.3 mV	13.6 ms 3.0 mV
nA-Bias Generator			$I_Q$		
			3.2-3.7 nA		
Net Energy Gain per Cycle			1.273 nJ		
Power Gain at 30 Hz			38.19 nW		

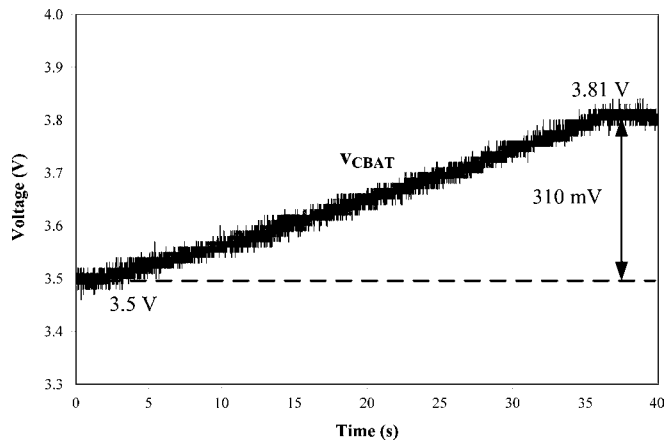


Fig. 20. Voltage profile of prototyped energy-harvesting system charging  $1 \mu\text{F}$ .

accordingly. Because  $V_{REF}$  is fixed, however, the system was eventually unable to invest sufficient energy into  $C_{VAR}$  to avoid  $v_C - V_{BAT}$  mismatch voltage losses across  $MP_H$  from increasing to the point a gain was no longer possible. As a result, the system stops charging  $C_{BAT}$  at 3.81 V. Including a feedback loop to dynamically tune  $V_{REF}$  to ensure  $v_C$  reaches  $V_{BAT}$  in precharge would eliminate the problem, except the losses in the same must be low enough for the system to continue generating a net positive gain.

## VI. DISCUSSION

The fact the prototype generated and channeled 2.14 nJ/cycle (i.e., 64.2 nW at 30 Hz) into a 3.5 V battery means the system can replenish some of the energy a wireless microsensor, for example, consumes. The generated power may seem low for practical applications but duty-cycling the sensor to operate a fraction of the time viably enables the system to accumulate sufficient energy in the battery to supply the power needed (when demanded). That is to say, the on-board battery powers the sensor's high-power tasks, such as wireless transmission

and readout, only after the battery amasses enough energy from the harvester. Consider, for instance, that 10 ms of wireless transmission at 5 mW and sensing at 10  $\mu\text{W}$  for 1 ms [16], [37] requires about 50  $\mu\text{J}$ , so according to the energy harvested from a 3.5 V battery, the harvester can replenish the total energy used in 778.04 s (in 13 min.). In other words, allowing the wireless micro-sensor to sense and transmit once every 13 min. enables the prototype to harvest from the environment all the energy the system requires, extending its operational life almost indefinitely, barring the wear-and-tear effects of the components.

The fundamental advantage of constraining  $C_{VAR}$ 's voltage instead of its charge is sub-5 V operation because the 50–300 V that restraining charge would otherwise produce [27] require higher voltage transistors, which only lower volume (higher cost) semiconductor technologies offer. Another benefit is using the already existing battery-to-be-charged to constrain voltage. These functional gains, however, result at the expense of lower energy because energy is proportional to voltage, and 2.7–4.2 V generates considerably lower power levels than 50–300 V. Note that matching the capacitor's electrostatic force to the damping mechanical forces produces the highest possible energy, albeit with further system complexities and, as a result, additional power losses. Nevertheless, drawing low power over time can ultimately harvest vast amounts of energy, which low-power and duty-cycled microsensors can viably manage and endure.

The prototype suffers from a few disadvantages that an otherwise improved design could relinquish. To start, as mentioned already, a low-bandwidth feedback loop should dynamically adjust  $V_{REF}$  to ensure the system charges  $C_{VAR}$  to  $V_{BAT}$ , even as  $V_{BAT}$  changes and/or other system conditions change. The designer should also optimize the speed and losses of the IC to operate at the known vibration frequency. In the presented case,  $C_{VAR}$ 's resonance frequency and capacitance range were unavailable during the design phase so optimizing the precharger's switching-conduction tradeoff losses was

difficult. Additionally, operating the detection circuits for only a fraction of each half cycle would reduce losses. Finally, including battery-protection features by monitoring  $V_{BAT}$  every several vibration cycles would complete the system at a small incremental (energy) expense.

Note that the prototype outputs usable power to the microsystem even when using a non-optimal energy-conversion device (i.e., transducer). More efficient transduction schemes maximize mechanical-electrical energy conversion by minimizing mechanical losses like air friction [14]. From an electrical standpoint, a transducer optimized for voltage-constrained harvesting seeks to maximize  $\Delta C$ , rather than increase  $C_{MAX}/C_{MIN}$ , which benefits charge-constrained systems. When integrated, a MEMS device would have to also manage low pull-in voltages, stiction, and relatively large areas (to realize high capacitances), so an optimized solution will more than likely exhibit both a smaller  $\Delta C$  and a lower  $C_{MAX}$  (e.g., 500–100 pF) and, because of the lighter mass, resonate at higher frequency. These characteristics partially compensate one another because, while a smaller  $\Delta C$  reduces the energy harvested, a lower  $C_{MAX}$  requires less investment energy and a shorter period decreases the time (energy) detection blocks operate (in each cycle). Shorter vibration periods, however, require faster comparators and proper adjustment of the precharge detection RC delay circuit. Nevertheless, the aim and significance of the presented prototype is to convert as much energy as the transducer avails, irrespective of the quality (efficiency) of the transducer, research for which others better trained in the art currently conduct.

The design used the 5 V n- and p-type MOSFETs and 8 V NPN BJTs that TI's high-volume BiCMOS process availed. Only two instances in the entire system exploit the bipolar features offered: (1) the p-tank that embeds  $CP_{SW}$ 's n-type input pair in Fig. 6 and (2) the vertical NPN BJTs that generate the PTAT current in Fig. 7(a). Although these choices reduce noise sensitivity, improve bias accuracy, and use smaller transistors, an all-CMOS design that allows the nMOS pair to lie in the p-type substrate and employs large subthreshold MOSFETs in place of BJTs (as in Fig. 14) would work. The CMOS solution could also integrate on chip the external voltage reference and off-chip resistors the prototyped system used for testing flexibility and proof-of-concept purposes.

## VII. CONCLUSION

The presented IC harvested 1.27, 2.14, and 2.87 nJ/cycle from vibrations at 30 Hz, generating 38.1, 64.2, and 86.1 nW, and used the energy to charge a battery at 2.7, 3.5, and 4.2 V and charge a 1  $\mu\text{F}$  battery-emulating capacitor from 3.5 to 3.81 V in 35 s. The system did this by efficiently sensing and synchronizing a variable capacitor's state as it cycled from  $C_{MAX}$  and  $C_{MIN}$  to (i) precharge it at  $C_{MAX}$ , (ii) harvest while it decreases to  $C_{MIN}$ , and (iii) reset automatically as it increases back to  $C_{MAX}$ . Producing a net energy gain, however, ultimately translates to reducing losses, which is why the system time-managed and biased its circuits to operate only when needed and with just enough energy (deep in subthreshold). Although further duty-cycling the circuit, dynamically adjusting the precharge

target voltage, improving the nA generator, and building a reliable and efficient MEMS variable capacitor could further reduce losses and increase output power, the system nonetheless produced a net gain that could viably extend the life of a wireless microsensor indefinitely.

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