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Designing 1-V Op Amps Using Standard Digital CMOS Technology

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***Abstract*— This paper addresses the difficulty of designing 1-V capable analog circuits in standard digital complementary metal–oxide–semiconductor (CMOS) technology. Design techniques for facilitating 1-V operation are discussed and 1-V analog building block circuits are presented. Most of these circuits use the bulk-driving technique to circumvent the metal–oxide–semiconductor field-effect transistor turn-on (threshold) voltage requirement. Finally, techniques are combined within a 1-V CMOS operational amplifier with rail-to-rail input and output ranges. While consuming 300 μW, the 1-V rail-to-rail CMOS op amp achieves 1.3-MHz unity-gain frequency and 57° phase margin for a 22-pF load capacitance.**

***Index Terms*— CMOS analog integrated circuits, current mirrors, differential amplifiers, operational amplifiers.**

I. Introduction

FACTORS associated with the scaling of complementary metal–oxide–semiconductor (CMOS) technology such as reliability and density are driving down supply voltages. Furthermore, the rapid growth of portable applications promotes battery operation which favors low voltage and low power circuits. As a result, many suggest that future implementation of mixed analog–digital circuits using standard CMOS will have power supplies of 1.5 V or less [1], [2]. Communication large-scale integrations (LSI's) are predicted to target 1-V operation [3].

Threshold voltages of future standard CMOS technologies may not decrease much below what is available today [4]. This poses a great challenge to CMOS analog/mixed-signal circuit design. Consider the standard push–pull CMOS amplifier/inverter and transmission gates, these circuits require the analog power supply to be at least equal to the sum of the magnitudes of the n-channel and p-channel thresholds [5]. This implies that low-voltage analog circuits are incompatible with the CMOS technology trends of the future. To circumvent this conflict without requiring costly development of CMOS technologies with lower thresholds or an high-efficiency on-chip dc–dc converter to increase the internal supply voltage (which scaling may not tolerate), circuit techniques must be developed that are compatible with future stan technology trends.

This paper focuses on developing analog circu that are compatible with future CMOS technologi circuit techniques which permit low voltage op large thresholds offer the potential for more thoro ing the technology at any voltage range even if l voltage technologies become standard. Analog bu circuits such as differential amplifiers and cur which achieve 1-V operation will be described in of the blocks will then be used to design and impl CMOS rail-to-rail input/output op amp that has be in standard 2-μm CMOS technology having thresh in the range of ±0.8 V.

II. Building Blocks for 1-V CMOS Analo

A limitation to implementing analog circuits at is the threshold voltage. The metal–oxide–semicon effect transistor (MOSFET) must be turned on perform any type of signal processing. This for CMOS technology the power supplies mus following requirement

$$V_{DD} + |V_{SS}| \geq V_{GS} = V_{DSsat.} + |V_T$$

for strong inversion operation where V_{DD} is the po supply, V_{SS} is the negative power supply, and magnitude of the largest threshold of the nMO transistors. Furthermore, when gate-driving the M supply voltage requirement becomes

$$V_{DD} + |V_{SS}| \geq V_{GS} = V_{DSsat.} + |V_T| + V$$

The turn-on or threshold voltage requirement ulti strains signal swing and consequently dynamic r MOSFET is bulk-driven, then the voltage overhea with V_T is removed from the signal path.

A. The Bulk-Driven MOSFET

Probably the most important solution to the thr age limitation is the bulk-driven MOSFET. Fig. a nMOSFET structure cross section where a p-v is assumed. For simplicity, a junction field-effe (JFET) schematic symbol labeled "channel JFET Fig. 1 to represent the bulk-driven MOSFET. The potential is taken to a dc voltage that is suffici on the MOSFET. The drain is connected norm signal is applied between the bulk and the source.

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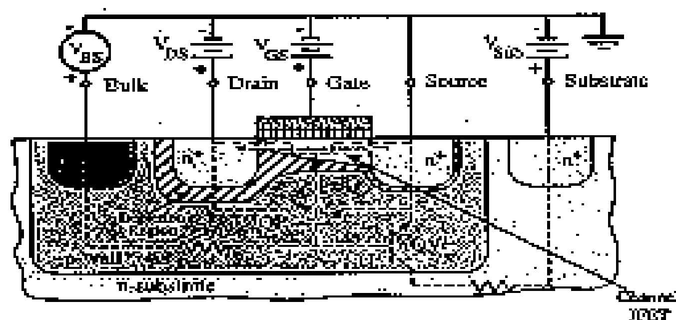

Fig. 1. Cross section of n-channel MOSFET (p-well CMOS technology).

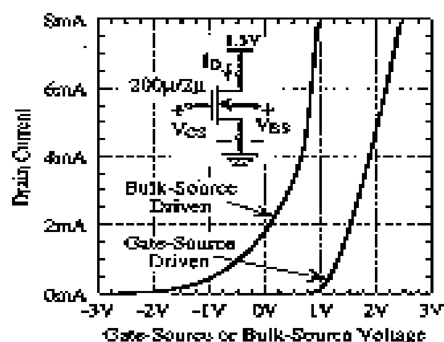

Fig. 2. Measured linear I_D versus V_{BS} for the bulk-driven MOSFET and V_{GS} for the standard MOSFET.

flowing from the source to drain is modulated by the reverse bias on the bulk–channel junction. The result is a junction field-effect transistor with the bulk as the signal input (gate). Consequently, a high-input impedance depletion-mode device results.

To understand the bulk-driven MOSFET better, consider the experimental transconductance characteristics shown in Fig. 2. This plot shows drain current versus bulk-source voltage ($V_{GS} = 1.5$ V) and drain current versus gate-source voltage ($V_{BS} = 0$ V). Although the W/L is large, smaller values of W/L simply reduce the value of I_{DSS} ($I_D @ V_{BS} = 0$ V) for the JFET. It is appropriate to use a JFET parameter such as I_{DSS} to describe the bulk-driven MOSFET given its depletion-mode behavior.

First-order theory [6] gives the dependence of the drain current, i_D, of a MOSFET as

$$i_D = \frac{K'W}{L}\left(v_{GS} - V_T - \frac{n}{2}v_{DS}\right)v_{DS}, \quad v_{DS} \leq V_{DSsat} \tag{3}$$

and

$$i_D = \frac{K'W}{2nL}(v_{GS} - V_T)^2(1 + \lambda v_{DS}), \quad v_{DS} \geq V_{DSsat} \tag{4}$$

where

$$n = 1 + \frac{C_{BC}}{C_{ox}} + \frac{qNFS}{C_{ox}} = 1 + \frac{\gamma}{2\sqrt{\phi_j - V_{BS}}}$$
$$= 1 + \eta = 1 + \frac{g_{mb}}{g_m} \tag{5}$$

and

$$V_{DSsat} = \frac{v_{GS} - V_T}{n}.$$

The parameters in (5) are identical with s
parameters for MOSFET's. However, to desc
operation, the V_T term in (3) and (4) is expa

$$i_D = \frac{K'W}{L}\Big(V_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - \cdots}$$
$$+ \gamma\sqrt{2\phi_F} - \frac{n}{2}v_{DS}\Big)v_{DS}, \quad v_{DS}$$

and

$$i_D = \frac{K'W}{2nL}\big(V_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - \cdots}$$
$$+ \gamma\sqrt{2\phi_F}\big)^2(1 + \lambda v_{DS}), \quad v_{DS}$$

These equations are used for the theoretical p
bulk-driven MOSFET's drain current but tes
that they need to be reexamined to permit b
between experimental and theoretical results.
that the Berkeley short-channel insulated-gate
[7] can model bulk-source operation reasona
ever, the BSIM model tends to over estimate
as the bulk-source junction is forward biased

The bulk-driven MOSFET has several a
tages. The obvious advantage is the depleti
which allows zero, negative, and even small p
bias voltage to achieve the desired dc current
to larger input common-mode ranges that cou
be achieved at low power supply voltages. An
advantage of the bulk-driven MOSFET is
poly gate to modulate the bulk-driven MOSF
gate can totally shutoff the channel, the on
bulk-driven MOSFET modulated by the gat
Furthermore, throughout extensive experimen
of bulk-driving the MOSFET, latch-up has no
a problem.

Matching between individual bulk-driven
similar to that of standard MOSFET's. As
MOSFET's operation is depletion-mode, it i
describe it with JFET parameters I_{DSS} and V_P
age). Experimental data shows that the bulk-dr
I_{DSS} and V_P varies by ±4.2% and ±1%, re
for the same transistors the K' varies by ±
±2.9%. A potential advantage of the bulk-
is that the small signal transconductance, g_m
be larger than the MOSFET's transconduc
is demonstrated by examining the expressio
below:

$$g_{mb} = \frac{di_D}{dv_{BS}} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{BS}}}$$

The bulk-driven MOSFET transconductance
gate-driven MOSFET transconductance if

$$V_{BS} \geq 2\phi_F - 0.25\gamma^2 \approx 0.5 \text{ V}$$

Of course, there may be appreciable curren
bulk-source junction under these conditions.

One disadvantage of the bulk-driven MOSFET is its input capacitance. Consider the frequency response of the bulk-driven MOSFET compared to that of a gate-driven MOSFET. The gate-driven MOSFET's frequency response capability is described by its transitional frequency, f_T.

$$f_{T,\text{gate-driven}} \approx \frac{g_m}{2\pi C_{gs}} \tag{11}$$

where C_{gs} is the gate-to-source capacitance [6]. At frequencies beyond f_T, the device no longer provides signal gain. Likewise, for the bulk-driven MOSFET

$$f_{T,\text{bulk-driven}} \approx \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} = \frac{\eta g_m}{2\pi(C_{bs} + C_{bsub})} \tag{12}$$

where η is the ratio of g_{mb} to g_m and typically has a value in the range of 0.2 to 0.4, C_{bs} is the bulk-to-source capacitance, and C_{bsub} is the well-to-substrate capacitance. In [8] convenient normalization factors are provided for comparing C_{bs} to C_{gs} for different device layouts in a 3 μm CMOS process. According to [8], for an interdigitated layout, $C_{bs} \approx 0.18C_{gs}$ for the nMOS. The proportionality of C_{bsub} to C_{gs} is approximated using the bulk area and periphery, the well doping density, the substrate doping density, and applied voltage bias across the bulk-substrate pn junction. For digital CMOS technology, the well and substrate doping density is approximately 10^{16} cm^{-3} and 10^{15} cm^{-3}, respectively [9], [10]. Similar to the C_{bs} estimate, consider a pessimistic zero-bias estimate for C_{bsub} (as with any depletion capacitance, C_{bsub} reduces with reverse-bias of the well-substrate junction). In the bulk-driving technique the well-substrate pn-junction is never forward-biased. Using the doping information, the zero-bias C_{bsub}/area estimated value is 0.087 fF/μ^2 [9]. A comparison to C_{gs} is made once a bulk area is selected for a given MOSFET. A reasonable estimate of bulk area is approximately three times the source/drain diffusion area of MOSFET. For a minimum gate length device with a gate width W, the bulk area is approximately $3(W4L_{\min})$. Conservatively, the resulting capacitance is multiplied by 2 to account for the bulk-to-substrate sidewall depletion capacitance. For saturated strong inversion MOSFET operation and using the previously mentioned approximations it can be shown that [11]

$$f_{T,\text{bulk-driven}} \approx \frac{\eta}{3.8} f_{T,\text{gate-driven}}. \tag{13}$$

In scaling CMOS technology to shrink the minimum feature size, the above ratio improves as C_{ox} increases by the scaling factor $S > 1$, and the C_{bsub}/area parameter should only increase by a factor of $\sqrt{S}$ if the well and substrate doping densities each increase by a factor of S [10]. Because of scaling, (13) becomes

$$f_{T,\text{bulk-driven}} \approx \frac{\eta\sqrt{S}}{3.8} f_{T,\text{gate-driven}}. \tag{14}$$

If a CMOS technology currently has 1.0 μm minimum feature size, for example, and later is scaled such that a 0.5-μm minimum feature size is achieved, the corresponding S factor for this scenario is 2. While $f_{T,\text{bulk-driven}}$ probably will not equal $f_{T,\text{gate-driven}}$ in a future standard CMOS technology, utilizing the bulk-driven technique should not sa deal of frequency response.

Another potential disadvantage of the bulk-dri is noise. Obviously the channel noise current i both the gate-driven and bulk-driven cases. gain factor referring the channel noise current distinguishes the bulk-driven case from the gat Also, the bulk (or well) sheet resistance of th MOSFET can contribute additional thermal attention must also be given to gate resistance, if process is used. Normal MOSFET geometries do optimum bulk-driven MOSFET from the viewp The noise considerations for the bulk-driven i explicitly described in the bulk-referred mean voltage expression for the MOSFET [11]

$$\overline{v}^2_{n,\text{bulk}} = \left(\frac{8KT(1+\eta)}{3\eta^2 g_m} + \frac{KF}{2fC_{ox}WLK'\eta^2} + \times \left(\sum_{i=1}^{N} R_{bi} + \frac{1}{\eta^2}\sum_{i=1}^{N} R_{gi}\right)\right)\Delta f$$

where N is the number of gate fingers within itated MOSFET structure, R_{bi} is the effective resistance for the ith gate channel, and R_{gi} is series gate-metal resistance of the ith gate. MO noise and flicker noise referred to the bulk described by the first and second terms, resp last two terms above describe the thermal noi to bulk- and gate-metal resistance. The N^{-2} (15) is an encouraging result since the noise co gate resistance, determined by polysilicon sheet approximately 22 Ω/square (nonsilicided), is η^{-2}, a factor nominally between about 9 and influence caused by gate resistance is reduced by a highly interdigitated MOSFET structure, i.e., with many individual gate strips or gate fingers. Th the summation of individual bulk resistance actu with interdigitization, whereas the sum of all gate resistance remains *constant* with interdigitiza to minimize bulk-referred noise for the bulk-driv the physical layout of the device should use generously. The contacts should be as close as each gate finger, which minimizes the noise co bulk resistance determined by well sheet resistivi imately 2500 Ω/square. The aforementioned she values correspond to the MOSIS 2-μm n-well CM

B. Differential Amplifiers

One of the key building blocks in analog ci differential amplifier. The bulk-driven differential is shown in Fig. 3. For the nMOS example sh technology), the gates of both devices are tied to An inversion layer channel is formed within eac

[1] MOSIS VLSI fabrication service, Information Sci Univ. Southern California, Pasadena, CA. [Online]. Availa mosis.org/intro.html.

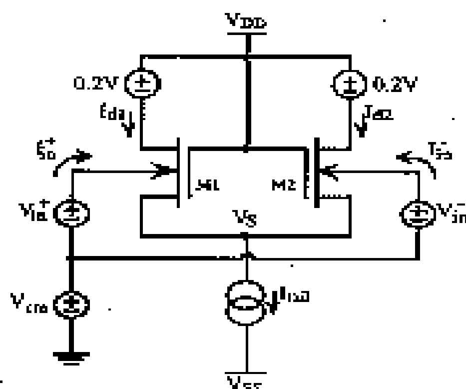

Fig. 3. Schematic for bulk-driven differential pair measurements.

Because the source-coupled MOSFET's have isolated individual wells, a differential voltage signal is applied between the bulk terminals of M1 and M2. The differential input signal, via the bulk-to-channel transconductance action of the pair, causes current to be steered between M1 and M2 such that

$$i_1 - i_2 = G_{mb} v_{in} \tag{16}$$

where G_{mb} is the differential transconductance and v_{in} is the differential input voltage signal. Using first-order theory, the differential transconductance of the pair is described by

$$G_{mb} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{cm} + V_S}} = \frac{\gamma\sqrt{(K'/n)(W/L)I_{tail}}}{2\sqrt{2\phi_F - V_{cm} + V_S}} \tag{17}$$

where V_{cm} is the voltage common to both bulk terminals (common-mode), V_S is the source-coupled node voltage, and I_{tail} is the tail current biasing the differential pair. V_{cm} can move rail-to-rail, since the MOSFET's bulk-source junction is amenable to both reverse and forward biases. Within a 1-V supply, V_{cm} cannot forward-bias the bulk-source junctions enough to strongly turn-on the parasitic lateral and vertical BJT's (shown in Fig. 1) thereby compromising the pair's input impedance. The variation in threshold voltage with common-mode voltage makes this possible. Threshold voltage reduces for forward-biasing of the bulk-source junction, and as a result V_S follows V_{cm} to a degree. For a nMOS pair, as V_{cm} moves beyond mid-supply toward V_{DD}, the source-coupled node also moves toward V_{DD}.

Measured data on a bulk-driven differential pair fabricated in 2-μm p-well CMOS technology is shown in Figs. 4 and 5. The circuit schematic for all the measurements is shown in Fig. 3. In all cases, the aspect ratios of M1 and M2 are 400 μm/2 μm with the 1-V supply voltage realized by V_{DD} = +0.5 V and V_{SS} = −0.5 V. The n-substrate is tied to +0.5 V. For a mid-supply common-mode voltage, the circuit's measured transconductance varies from 75 μS for I_{tail} = 10 μA to approximately 310 μS for I_{tail} = 50 μA. For two tail currents, 40 and 50 μA, the bulk-driven differential pair's transconductance is measured as a function of common-mode voltage and plotted in Fig. 4. In Fig. 4 a second-order

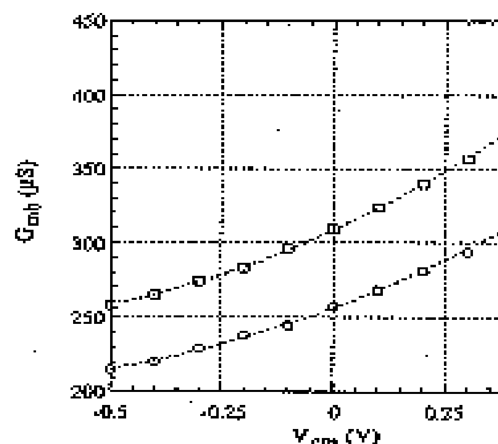

Fig. 4. Measured common-mode voltage influence on ... tial pair transconductance.

polynomial curve fit to the data is performed, dashed lines. Using the V_{cm} = 0 V value of of each tail current case as the nominal value differential pair's transconductance at V_{cm} below the nominal value for the 40 μA case nominal for the 50-μA case. The BDDP's is 28% above nominal for the 40-μA case, nominal for the 50-μA case at $V_{cm} = V_{DD}$. G_{mb} as a function of common-mode voltage (17). Taking the derivative of (17) with resp

$$\frac{\partial G_{mb}}{\partial V_{cm}} = \frac{\gamma}{4} g_m (2\phi_F - V_{cm} + V_S)$$

The measurement results demonstrate that a increases the rate at which G_{mb} changes wit gate transconductance g_m is greater for the 5 case, resulting in more total variation of G_m in the 40-μA case.

As mentioned earlier for the nMOS pair technology), the threshold voltage reduces proaches V_{DD}, allowing the source-coupled n to rise. Measurements of this behavior are for the same bulk-driven differential pair a Since the largest tail current of 50 μA re V_{GS}, its corresponding V_S is the nearest to −0.5 V in these measurements. For a cons the measured data indicates that V_S is appro function of V_{cm}. For 50-μA tail current, V_S re reaches V_{DD} = +0.5 V, indicating a 500-m of each MOSFET's bulk-source junction, the entire common-mode sweep. Even at this ex measurements indicate that I_{in}^{+} (the circuit's p current) only reaches 2 nA. In addition, the become evenly spaced for tail currents grea This indicates that the nMOS BDDP move strong inversion saturation operation for a tail 10 and 20 μA.

For a 1-V total supply voltage with th driven differential pair's gate-coupled node fi

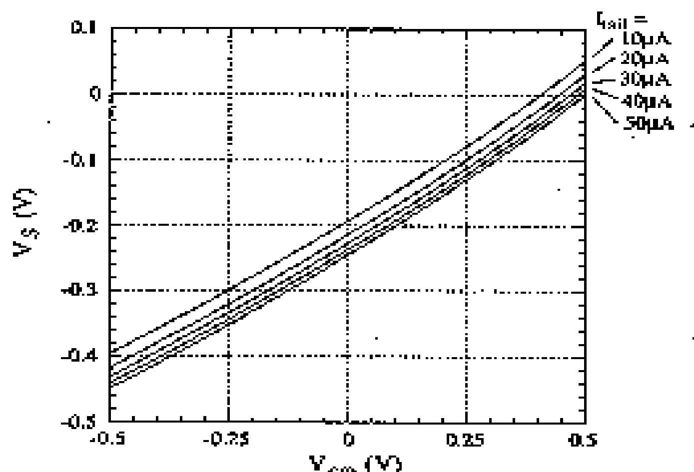

Fig. 5. V_S versus V_{cm} for BDDP circuit.

voltage headroom for the tail current sink reduces as V_{cm} moves toward V_{SS}. From Fig. 5 the 20 μA tail current bias corresponds to V_S reaching -0.4 V when $V_{cm} = -0.45$ V, leaving 100 mV across the tail current sink. When using a single MOSFET to provide the tail current, proper design of the bulk-driven differential amplifier can provide adequate V_{DS} voltage headroom for the tail current device to maintain saturated operation over the entire rail-to-rail input common-mode range (ICMR).

The BDDP circuit's input and output capacitance determines its frequency response. The dominant parasitic capacitors of the BDDP circuit are shown explicitly in Fig. 6(a). Also depicted are the equivalent input capacitance ($C_{\text{in,eq}}$) and the equivalent output capacitance ($C_{L,\text{eq}}$) which consist of parasitic capacitors. R_L represents an arbitrary load. For comparison, Fig. 6(b) provides a similar illustration of the gate-driven differential pair. For the bulk-driven differential pair

$$(C_{\text{in,eq}})_{\text{bulk-driven}} \approx C_{bs} + C_{b\text{sub}} + (1 - (-g_{mb}R_L))C_{bd} \tag{19}$$

and

$$(C_{L,\text{eq}})_{\text{bulk-driven}} \approx C_{gd} + C_{ds} + C_{bd} \tag{20}$$

where $-g_{mb}R_L$ is the inverting voltage gain across each C_{bd} causing Miller Effect. For the gate-driven differential pair

$$(C_{\text{in,eq}})_{\text{gate-driven}} \approx C_{gs} + (1 - (-g_m R_L))C_{gd} \tag{21}$$

and

$$(C_{L,\text{eq}})_{\text{gate-driven}} \approx C_{gd} + C_{ds} + C_{bd}. \tag{22}$$

The equivalent load capacitance in both cases is equal. If the two differential pairs are equivalently loaded, the pole at their respective outputs is identical. There is a significant difference in input capacitance. In fact, in terms of input capacitance, the two circuits share no common capacitive elements. Furthermore, given the factor of η difference in

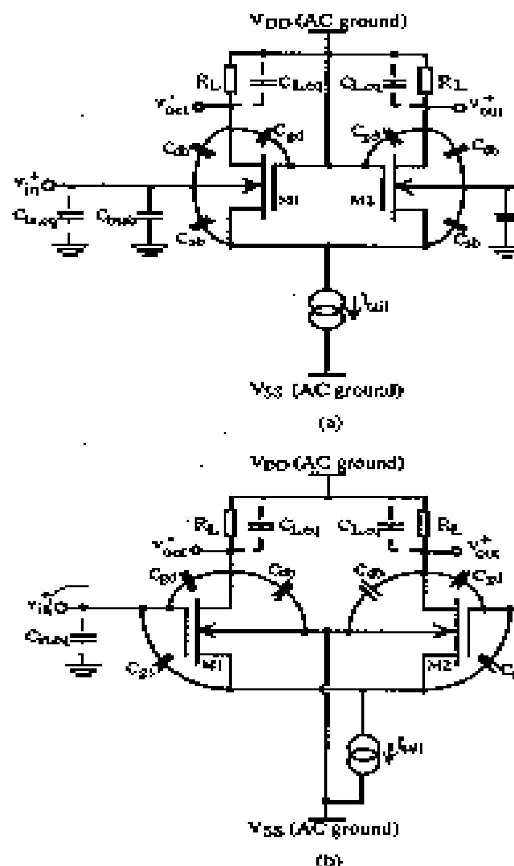

Fig. 6. Dominant capacitors of the bulk-driven differentia[...] the gate-driven differential pair (b).

voltage gain between the two circuits, there is [...] difference in Miller effect influencing each inpu[...] Since the bulk-driving technique avoids the st[...] bias condition of the bulk-source junction η [...] less than one, implying that the Miller Effe[...] the BDDP's input capacitance is less than tha[...] differential pair. This means that the BDDP's [...] is less than that of gate-driven differential pair [...] tail current and load. The difference in input [...] only a concern if the driving signal source has [...] resistance.

Methods for loading the BDDP become lir[...] Consider resistive loads for the BDDP: The opti[...] menting resistors in digital CMOS technology a[...] gate metal, well diffusion, source/drain diffusi[...] operated MOSFET's. Within a 1-V supply, how[...] operated MOSFET is not an option as only 1 [...] be applied to the MOSFET, making its V_{DSsat} [...] 200–300 mV if V_T is in the range of 700 to [...] such a low V_{DSsat}, it is practically impossible [...] that the MOSFET will be triode-operated. M[...] the standpoint of flicker noise, the passive resist[...] more attractive because their noise is essentiall[...]

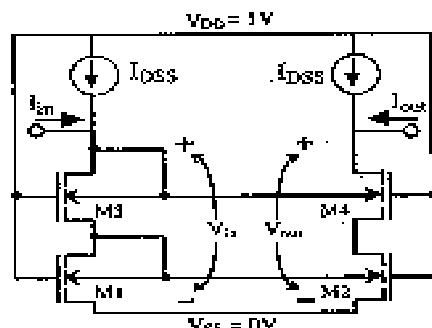

Fig. 7. Cascode bulk-driven MOSFET current mirror.

The allowable voltage drop across the load element, however, is less than 0.5 V to avoid strongly forward-biasing the drain-bulk junction when the input common-mode voltage nears one of the supply rails. In addition to the practical limitation of g_{mb} of less than 1 mS, voltage gains of even 3 V/V are not feasible for a 1-V resistively loaded BDDP with passive resistor loads. Active current sources or current mirrors must be used to load a 1-V bulk-driven differential amplifier, at the expense of additional noise.

C. Current Mirrors

One of the problems with MOSFET or BJT current mirrors is that a significant voltage must be dropped across the input device. If the bulk-driven MOSFET is operated with the bulk-source junction slightly forward biased, this voltage drop is minimized. A MOS cascode current mirror capable of 1-V operation is shown in Fig. 7 [12]. Note that instead of the gate-drain diode connection used in the standard MOS cascode current mirror, this new current mirror has a bulk-drain connection. The bulks of M1–M2, M3–M4 are tied together and all the gate connections for this n-type version (p-well technology) go to the most positive voltage available, V_{DD}. This approach dramatically improves the input and output current matching compared to the simple bulk-driven current mirror reported in [13] since both of the bottom devices operate in the active region. Also, using the cascode devices, the output conductance of the mirror is decreased to reasonable levels, much lower than in [13]. If a quiescent current equal to I_{DSS} of the bulk-driven MOSFET is applied to the input and output, then good matching between the input and output currents can be achieved down to values approaching zero. The primary advantage of Fig. 7 is the very low voltage required at the input of the current mirror. Fig. 8 shows experimental results for Fig. 7 with 100 μm/2 μm transistors and 200 μm/4 μm transistors. The input voltage drop across a sample of four current mirrors is shown to the right of the output characteristics. Note that the voltage drop across the input can be much less than 0.5 V for appreciable currents. In Fig. 8, I_{DSS} is included in both I_{in} and I_{out}. Fig. 8(b) indicates that I_{DSS} for the 200 μm/4 μm device must be between 10 μA and 20 μA since good matching is achieved at 20 μA and higher, but not at 10 μA. As expected, the matching of the transistors

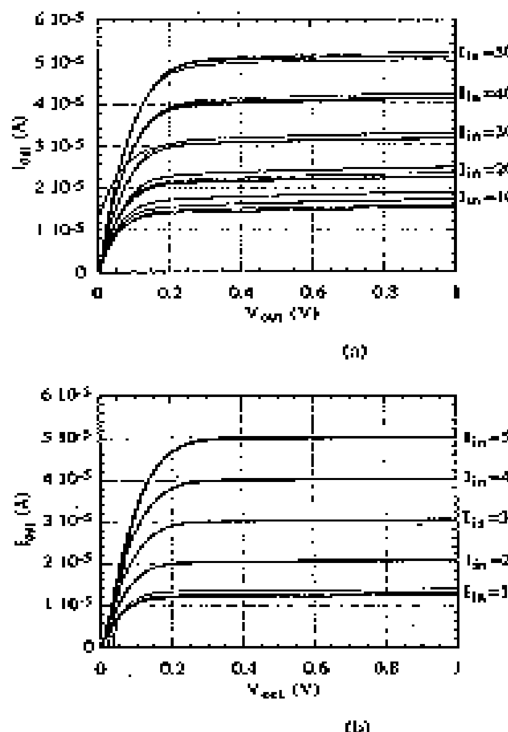

Fig. 8. Results of four identical bulk-driven MOSFE (a) 100 μm/2 μm and (b) 200 μm/4 μm transistors. T gives the voltage drop across each current mirror inpu

is much better using 4-μm channel length 2-μm channel lengths.

The small-signal frequency response of cascode current mirror (BDCCM) circuit is

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb2}}{(C_{bs1\&2} + C_{bsub1\&2} + C_{bd1}} \times \left(\frac{1}{s + \frac{g_{mb1} + g_{bs1}}{C_{bs1\&2} + C_{bsub1\&2} + C_{b}}} \right.$$

indicating a dominant single-pole response small-signal impedance at the bulk coupled For comparison, consider the familiar ga current mirror's frequency response. Its co the same device names as the BDCCM circ

$$\frac{i_{out}}{i_{in}} \approx g_{m2}\frac{v_{gs2}}{i_{in}} = g_{m2}\frac{v_{gs1}}{i_{in}}$$
$$\approx \frac{g_{m2}}{(C_{gs1} + C_{gs2} + C_{bd1})}\left(\frac{1}{s + \frac{g_{m1}}{C_{gs1} + C}} \right.$$

where C_{bd3} is neglected because of the nearl across it while the circuit is operating. Th in form to the BDCCM circuit given by (dominant pole frequency response determi signal impedance at the coupled node of th devices. The gate-driven cascode current greater bandwidth in its frequency response

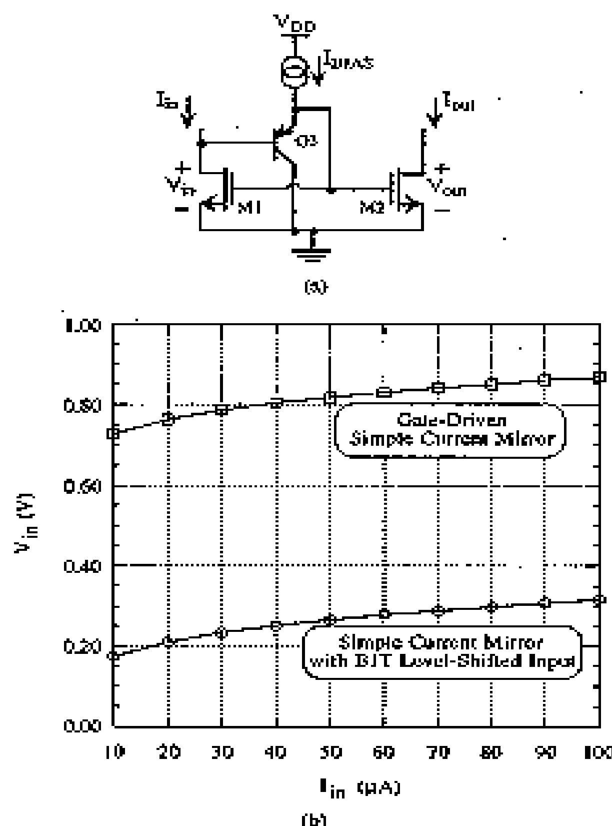

Fig. 9. Schematic of 1-V simple current mirror with (a) level-shifted input and (b) comparison of input voltage requirements of simple current mirrors.

associated with its dominant pole is considerably less than the BDCCM circuit's dominant pole capacitance. The BDCCM circuit, however, is capable of 1-V operation whereas the gate-driven cascode current mirror is not.

Another 1-V capable current mirror is the simple current mirror with level-shifted input (SCMLS) shown in Fig. 9. This circuit is a variation of the gate-driven simple current mirror. The BJT emitter-follower provides a level-shift between the circuit's input and the gate node. This reduces the input voltage requirement. The input voltage is described by

$$V_{in} = V_{GS1} - V_{EB3} \tag{25}$$

which is comparable to V_{DSsat} if $V_{Tn} \approx 800$ mV and $V_{EB} \approx 700$ mV. Over a wide range of input current levels, guaranteeing $V_{DS1} > 0$ V is difficult if a pMOS level-shifter (source-follower) is used since typically $|V_{Tp}| \geq V_{Tn}$. The minimum output voltage is identical to that of the gate-driven simple current mirror.

$$V_{out,min.} = V_{DS2sat}. \tag{26}$$

Note that the BJT in this circuit, a p-n-p, is readily available in digital n-well CMOS technology; therefore, no additional fabrication steps are needed. This BJT is implemented as a lateral [14], [15] or vertical device [16], [17]. In either case, an isolated n-well serves as the base. For a la source/drain diffusions serve as the emitter and co gate metal surrounding the emitter to define the d width. For the vertical p-n-p no gate metal is the substrate serves as the collector which is a common-collector configurations. The vertical p-n less silicon area, but tends to have lower beta tha p-n-p.

The small-signal input resistance of the SCML readily approximated by replacing the emitter–fo an ideal unity-gain buffer, a reasonable assumptio transfer characteristic and the high resistance s into the base of a current source biased emitter–fo SCMLS circuit's small-signal input resistance is d

$$r_{in} = \frac{1}{g_{m1} + g_{ds1}} \approx \frac{1}{g_{m1}}$$

where the $1/g_{m1}$ approximation is valid if M1 minimum gate length device with $g_{m1} \gg g_{ds1}$. is identical to the gate-driven simple current m Another similarity is the small-signal output resis

$$r_{out} = r_{ds2}.$$

DC measurements made on the SCMLS are Fig. 9(b) and Fig. 10(a). The devices are fabric MOSIS 2-μm n-well CMOS technology process. are 400 μm/2 μm nMOSFET's. The BJT is impl a lateral p-n-p with ten minimum geometry (4 μ emitters, biased at 10 μA. For comparison, the m are repeated on a gate-driven simple current mirror with the same M1 and M2 devices. So that gate-dr current mirror can also remain within a 1-V suppl current level is kept below 100 μA for all measu approximately 30 μA, the 400 μm/2 μm nMOS operate in moderate inversion. To generate Fig. 1(voltage of each mirror circuit is swept from 0 to 1 input current from 10 to 100 μA in 10 μA incr both mirrors, the output device appears to saturate a same output voltage level. The small-signal outpu indicated by the slope of each curve from abo V, is also identical. In the simple current mirro output current matching occurs only when V_{DS} SCMLS circuit input/output current matching o the output voltage is between 200 to 300 mV, de the input current level. For the gate-driven cur matching occurs at an output voltage between mV. The difference in output voltage between mirrors at which current matching occurs is in the difference in input voltage requirements betw circuits. Fig. 9(b) shows the input voltages for the mirrors corresponding to each input current leve entire range of input currents, the SCMLS circ approximately 550 mV less input voltage than the current mirror, even as the input device M1 ope transitional region of weak-to moderate inversion input current levels of 10–30 μA. The differen voltages is more than 50% of the allotted 1 V bud circuits. As a result, only the SCMLS circuit is

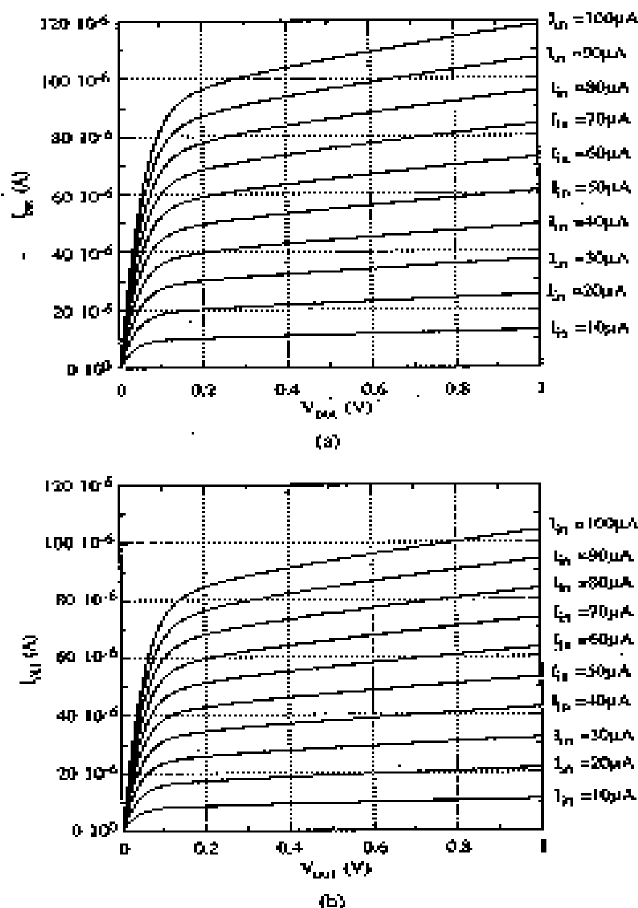

Fig. 10. Measured performance of simple current mirrors: (a) with BJT level shifting and (b) gate-driven.

load for a differential pair in a 1-V circuit. Since the BJT available in CMOS technology can have a beta of more than 200, its base current does not contribute significant error in input/output current matching in the SCMLS circuit.

The small-signal frequency response of the SCMLS circuit is described by [11]

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{m1}}{C_{\mu 3}+C_{bd1}}\left(\frac{1}{s+\frac{g_{m1}+g_{ds1}}{C_{\mu 3}+C_{bd1}}}\right). \quad (29)$$

indicating that the SCMLS has a dominant pole frequency response. This is similar in form to the gate-driven current simple current mirror's transfer function which is approximately equal to the result given in (24). Hence, if $C_{\mu 3}+C_{bd1}$ in (29) is less than $C_{bd1}+C_{gs1}+C_{gs2}$, then the SCMLS circuit will have greater bandwidth capability than the gate-driven simple current mirror. Given the structure of the BJT, C_{μ} is equivalent to $C_{bd}+C_{bsub}$ for pMOS in n-well technology. In the implementation of the SCMLS circuit the BJT is quite small, thus providing a C_{μ} equivalent to $C_{bd}+C_{bsub}$ of a *small* pMOS. Furthermore, implementing Q3 as a substrate p-n-p provides a C_{μ} equivalent to just C with careful consideration in the physical the SCMLS circuit should easily surpass a driven simple current mirror in frequency re Simulations verify that the SCMLS circuit ca a factor of two increase in frequency bandw the gate-driven simple current mirror. When BDCCM circuit, the SCMLS provides more 10 greater frequency bandwidth capability.

III. A 1-V CMOS Op Amp with Ra Input/Output Capability

The analog building blocks described ab building of CMOS op amps to operate at ve standard CMOS technology. One previously V CMOS op amp [5] utilizes the bulk-driven pair and composite transistors. A more th terized 1-V CMOS op amp design is now provides improved phase margin, unity-gai rate, and output signal swing to achieve rail-t performance.

A. Op Amp Schematic

The 1-V rail-to-rail CMOS op amp is Since device count and therefore, circuit co at a minimum, power dissipation in the hund is readily obtained. The input stage cons M1–M2, loaded by the SCMLS circuit. BDDP at the input provides rail-to-rail IC style current mirror is preferred because frequency bandwidth and low input voltage emitter–follower Q6 serves as a level-shifter stage and output stage. Less than 17% of current demand is needed for the two emi and Q6. Using a pMOS level-shifter in p induce systematic offset and, for the sam lower frequency parasitic pole than the emi level-shifter buffers the input stage from minimizing the capacitance at the output stage. Both Q5 and Q6 are CMOS com n-p BJT's where the base width is defin appropriately biased at V_{DD} to insure subs for BJT operation. The Class-A output stage M7 loaded by active current source M12 t PSRR [18]. R_z and C_c are the compensatio Miller pole-splitting technique [19]. With pole at the emitter of Q6 is not detrimenta phase margin. The op amp is biased wit source (I_{bias}) which is replicated and scal M8–M12. The op amp's gain–bandwidth pr loop gain are described by

$$\mathrm{GBW} \approx \frac{g_{mb1}}{2\pi C_c}$$

and

$$A_{vol,dc} \approx \frac{g_{mb1}g_{m7}}{(g_{ds2}+g_{ds4})(g_{ds7}+$$

respectively.

Fig. 11. 1-V rail-to-rail CMOS op amp schematic.

A total quiescent power dissipation of 300 μW is achieved with the selected current bias (I_{bias}) of 50 μA. I_{bias} = 50 μA corresponds to a 100-μA tail current, 100-μA quiescent current for the nMOS output driver M7 and 25-μA emitter currents for Q5 and Q6. Device aspect ratios are also given in Fig. 11. At the expense of adding significant parasitic capacitance to the design, a 6-μm gate length is chosen for M10 and M12 to minimize the output conductance of the tail current source and output stage current source, respectively, without cascoding. To minimize noise, the transconductance of the input differential pair is maximized for the 100-μA tail current by using the largest possible aspect ratio for M1 and M2 while still maintaining saturated strong inversion operation. Minimum gate lengths for M1 and M2 are used to avoid excessive parasitic capacitance at the output of the input stage. This limits the output impedance of the input stage which is detrimental to gain but beneficial to bandwidth. Using minimum gate lengths for M3 and M4 results in no significant further reduction in input stage output impedance since $\lambda_n < \lambda_p$. To minimize systematic offset, M7 is a scaled replica of M3 and M4. Selecting a minimum gate length for M7 is also desirable as it maximizes aspect ratio while keeping parasitic capacitance at a minimum. Minimizing C_{gs} for M7 pushes the parasitic pole at the emitter of Q6 out in frequency. In addition, a maximum g_{m7} pushes the load capacitance pole out in frequency. Both contribute to an increased phase margin.

Class-AB operation of the output stage, rather than Class-A, is desirable from the standpoint of power dissipation, but this would require using p-type current mirrors in the op amp such as the BDCCM (comprised of pMOSFET's in n-well technology), a pMOS gate-driven simple current mirror, or a current mirror using lateral p-n-p BJT's. The first two of these have limited frequency bandwidth at 1 V large device sizes required. Since CMOS-com p-n-p BJT's tend to exhibit low Early voltage, current mirror would have limited output im diminishes the op amp's achievable voltage g reasons, a Class-A output stage is utilized in t rail-to-rail op amp.

B. Op Amp Performance

The measured and simulated performance of rail-to-rail op amp is given in Table I. V_{DD} an V and −0.5 V, respectively, were chosen to c the mid-supply voltage at 0 V. MOSIS provi model for HSPICE utilized during the simulatio n-well CMOS technology with 2-μm minimu also available through MOSIS, was selected. data given in Table I verifies that the op amp a rail ICMR and output swing. The op amp has gain of 48.8 dB at a mid-supply common-mod with V_{cm} = mid-supply, a phase margin of gain frequency of 1.3 MHz is achieved for capacitance (see Fig. 12). Furthermore, unity-g still maintained even for a 102-pF load capac the four samples, approximately 1–3 dB higher gain is predicted in the simulation relative to results, possibly caused by the optimistic λ valu models. This results in lower device g_{ds} an higher gain. This could also justify the 11° margin from simulation predictions compared t phase margin, in addition to the 3-pF diffe capacitance.

TABLE I

SUMMARY OF 1-V CMOS RAIL-TO-RAIL OP AMP PERFORMANCE. UNLESS INDICATED OTHERWISE, EACH MEASUREMENT RESULT REPRESENTS AN AVERAGE FOR THE FOUR CHIP SAMPLE

parameter	simulated value	measured value
DC open-loop gain	44.6dB (V_{cm}=mid-supply)	48.8dB (V_{cm}=mid-supply)
I_{DD} (supply current)	300μA	287μA
Unity-gain frequency	1.3MHz (V_{cm}=mid-supply)	1.3MHz (V_{cm}=mid-supply)
Phase margin	68° (V_{cm}=mid-supply)	57° (V_{cm}=mid-supply)
ICMR	-395mV to 470mV	-475mV to 450mV
Output swing	-485mV to 498mV	-475mV to 491mV
SR^+ SR^-	0.82V/μs 2.2V/μs	0.7V/μs 1.6V/μs

THD, A_{vcl}=-1V/V	-74.0dB (0.020%)
	for (750mV$_{p-p}$, 1kHz sinewave)
	-71.1dB (0.028%)
	for (750mV$_{p-p}$, 10kHz sinewave)
		-59.6dB (0.105%)
		for (750mV$_{p-p}$, 1kHz sinewave)
		-56.2dB* (0.155%)
		for (750mV$_{p-p}$, 10kHz sinewave)

THD, A_{vcl}=+1V/V	-61.3dB (0.086%)
	for (750mV$_{p-p}$, 1kHz sinewave)
	-56.6dB (0.148%)
	for (750mV$_{p-p}$, 10kHz sinewave)
		-58.6dB (0.117%)
		for (750mV$_{p-p}$, 1kHz sinewave)
		-56.5dB* (0.150%)
		for (750mV$_{p-p}$, 10kHz sinewave)

$\overline{v_{ni}}$	18nV/√Hz (white noise only)	376nV/√Hz @ 1kHz 181nV/√Hz @ 10kHz 81.3nV/√Hz @ 100kHz 43.6nV/√Hz @ 1MHz
CMRR	56.2dB at 10kHz	NA
V_{DD} PSRR	83.7dB at 1kHz 82.2dB at 10kHz 59.1dB at 100kHz	60.8dB at 10kHz 54.8dB at 100kHz 21.7dB at 1MHz
V_{SS} PSRR	43.2dB at 1kHz 40.2dB at 10kHz 23.2dB at 100kHz	44.8dB at 10kHz 25.6dB at 100kHz 4.86dB at 1MHz
V_{os}	NA	chips 1-4: 1.2mV, 4.5mV, 3mV, -1.5mV

Note: V_{DD}=+0.5V, V_{SS}=-0.5V, C_L=25pF (simulated data) and C_L=22pF (measured data);
* one sample only

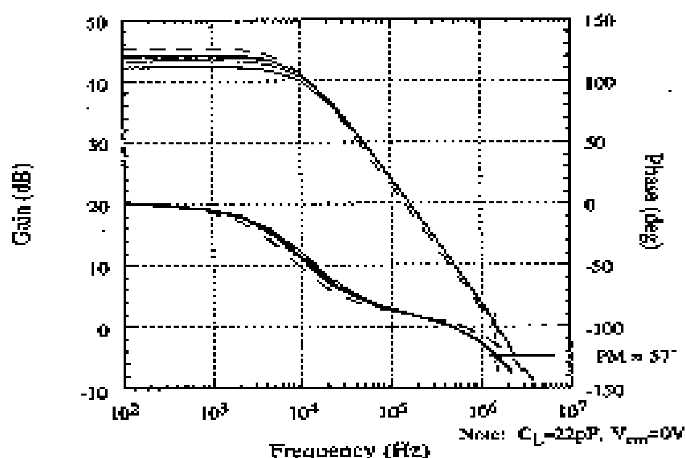

Fig. 12. Measured open-loop frequency response of 1-V CMOS WDR op amp (four-chip sample, C_L = 22 pF). The dashed lines represent the simulation result (C_L = 25 pF).

The positive-going slew rate (SR^+) of 0.7
the low quiescent current chosen for the Cla
A negative-going slew rate (SR^-) of 1.6
Asymmetrical slew rates are typical of C
Obtaining higher slew rates would require
dissipation.

In the unity-gain noninverting (buff
(A_{vcl} = +1 V/V), an average THD of
four samples is measured for a 1 kHz 750
sinewave input signal. For the same inpu
A_{vcl} = −1 V/V, an average THD of −59.
across the four samples of the 1-V rail-
amp. For these measurements, external 1-
used to select A_{vcl} = −1 V/V. The si
performance is overly optimistic by approxi
the inverting configuration but comparable f
configuration. This indicates that the sim
significant common-mode gain nonlinearity
stage, which could cause a second-order ha

fore significant THD [20]. The actual distortion measurements, however, indicate comparable distortion performance for both the inverting and noninverting op amp configurations, as described above. The bulk-driving technique utilized in the input stage did not seem to hinder distortion performance. The simulated low-frequency common-mode rejection ratio is just over 56 dB. This simulation excluded random offset effects.

The 1-V rail-to-rail CMOS op amp's input-referred noise characteristic is dominated by flicker noise. This is primarily caused by the nMOS load devices in the input stage and the minimum gate length required in the input differential pair. As discussed previously, using resistive loads for the input stage is desirable for reducing flicker noise, but utilized at the expense of input stage gain. With only a 1-V supply voltage, minimal voltage drop is allowed across resistive loads, severely limiting their resistance value.

The Class-A output stage with nMOS driver provides the 1-V rail-to-rail CMOS op amp with a measured low-frequency V_{DD} PSRR of over 60 dB and over 20 dB at 1 MHz. With the exception of low-frequency (10 kHz) V_{DD} PSRR, the simulated PSRR values agree within a few decibels of the measured values. This discrepancy is also attributed to optimistic λ values in the device models.

Since a four-chip sample is inadequate for standard deviation analysis, the 1-V rail-to-rail CMOS op amp's measured input offset voltage (V_{os}) for each chip is provided in Table I. In each case the magnitude of V_{os} remains less than 5 mV. The op amp occupies a 1536 μm × 986 μm area in 2 μm CMOS technology.

IV. Conclusion

Bulk-driving and prudent level-shifting permit the implementation of analog circuits at supply voltages as low as the MOSFET's threshold voltage plus approximately 200 mV. The bulk-driving technique removes the MOSFET's threshold voltage or turn-on requirement from the signal path and a device with depletion characteristics is obtained. Consequently the bulk-driven MOSFET provides a practical solution to enhancing input common-mode range. Realistically, this behavior can be achieved by adding one additional mask level to the standard CMOS process. However, the premise of this paper was that the technology would not be modified in any way to accommodate the analog circuits.

Some of the 1-V-capable analog circuit building blocks described in this paper were used to design a 1-V CMOS op amp with rail-to-rail ICMR and output swing. The op amp was implemented in a standard CMOS technology having a 2-μm minimum channel length and threshold voltages in the range of ±0.8 V. While driving a 22-pF load, the 1-V CMOS rail-to-rail op amp achieves 1.3-MHz unity-gain frequency with 57° phase margin.

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