

A Feedforward $10\times$ CMOS Current-Ripple Suppressor for Switching Power Supplies

Lucas A. Milner, *Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Senior Member, IEEE*

Abstract—With the advent of wireless microsensors and other microscale applications, switching supplies fully integrated on chip or into the package are desirable and often necessary. The problem with small inductors is that they exhibit low inductance and larger equivalent series resistance (ESR); in other words, they induce larger ripples in the output and higher conduction power losses. This brief presents and verifies a current-ripple suppression technique in which a discrete $2 \times 2 \times 1 \text{ mm}^3$ $4.7\text{-}\mu\text{H}$ inductor is effectively multiplied by subtracting a replica of the inductor's ac ripple current, allowing only a residual ripple to reach the output. Experimental results from a complementary metal-oxide-semiconductor integrated circuit prototype demonstrate a current- and output-ripple reduction of $10.8\times$ and $25.8\times$, respectively. The ESR power savings in the smaller inductor favorably offset the quiescent power lost in the multiplier (128 mW), outperforming its higher nonmultiplied $47\text{-}\mu\text{H}$ counterpart at high loads (above 250 mA).

Index Terms—Active filter, dc-dc power conversion, inductor, multiplier, power electronics, switching supply.

I. INTEGRATED INDUCTORS

DUE TO their versatility and efficiency, switched-inductor regulators are commonly featured in portable and stationary electronics. Unfortunately, the inductors are large and bulky when compared to other parts of the circuit. Their size cannot easily be reduced because of the inherent switching action of these converters creates an undesirable output voltage ripple that is inversely proportional to the inductance. The buck converter in Fig. 1, for example, alternately connects v_{SW} to dc input supply V_{IN} and ground to produce a square voltage that L_O and C_O filter. Filtered v_O is therefore equivalent to v_{SW} 's average (dc portion) plus a small ripple Δv_O , whose ripple amplitude depends on L_O and C_O . A lower L_O , as a result, generates larger current and voltage ripples Δi_L and Δv_O , i.e.,

$$\Delta i_L \approx \frac{V_{IN} d_{MP} d'_{MP}}{L_O f_{SW}} \quad (1)$$

$$\Delta v_O \approx \frac{V_{IN} d_{MP} d'_{MP}}{8 L_O C_O f_{SW}^2} \quad (2)$$

where d_{MP} is M_P 's duty cycle, d'_{MP} is $1 - d_{MP}$, and Δi_L 's effects on C_O 's capacitance often overwhelm those of C_O 's equivalent series resistance (ESR) [1]. Although integrating

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The authors are with the Georgia Tech Analog, Power, & Energy Research Laboratory, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: lamilner@ece.gatech.edu; rincón-mora@gatech.edu).

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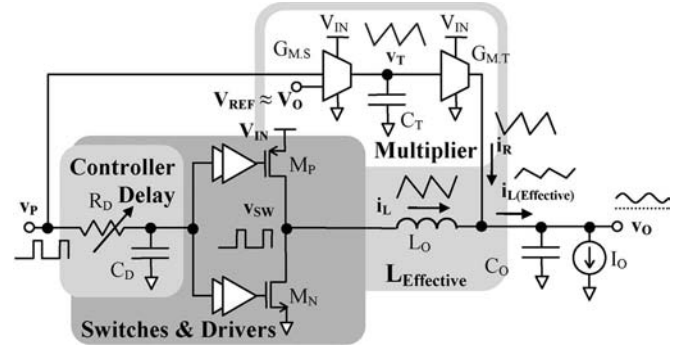


Fig. 1. Inductor-multiplied buck (R_D , L_O , and C_O are off chip).

inductors would increase power density and facilitate ultra-portable microsystems, the inductance required is large and difficult to include on chip or in the package.

Some techniques for reducing the required inductance have already been presented in the literature (Section II) but not without their shortcomings. Section III therefore describes the proposed inductor-multiplying technique and an integrated CMOS embodiment. Section IV then documents the experimental performance of the prototype, Section V discusses the results, and Section VI draws relevant conclusions.

II. REDUCING THE REQUIRED INDUCTANCE

The most straightforward means of reducing the inductance required is by increasing the switching frequency f_{SW} [2]–[6]. This approach, however, superimposes significant and often impractical tradeoffs in switching supplies, like the need for deep-submicrometer technologies to limit parasitic switching losses [2]–[5] or high-voltage transistors to withstand the large oscillations in high-frequency resonant converters [6].

Without increasing frequency, inductor current ripple Δi_L can still be suppressed, and there are a number of on-chip strategies involving additional active (power-consuming or lossy) filter circuitry. Adding a linear regulator between the switching regulator and the load, for instance, can suppress the ripple if the ripple's frequency is within the regulator's bandwidth. Unfortunately, the output voltage has to be reduced (i.e., dropped or bucked) by at least the amplitude of the ripple Δv_{SUPPLY} (plus $V_{DS(sat)}$ of the series power device), which constitutes another conduction loss ($I_{LOAD} \Delta v_{SUPPLY}$).

Alternatively, the active circuitry can be added in parallel [7]–[12]. Such circuitry must generate a ripple current that complements Δi_L such that when the two currents combine at the output, output capacitor C_O only absorbs a small residue, producing, in theory, a negligibly small output ripple Δv_O , as if the inductance itself was larger [8]. Reducing the voltage across

inductor L_O also suppresses Δi_L , but this requires additional voltage sources [8], [13]. Similarly, multiphase converters employ several simple converters in parallel that switch out of phase so that their respective inductor currents combine and cancel, except that the decrease in ripple greatly varies with duty cycle (and, therefore, with load current), and each added phase requires its own inductor and power switches, whereas inductor multiplication suffers neither problem.

III. PROPOSED INDUCTOR MULTIPLIER

A. Feedforward Approach

A feedback-based inductor multiplier senses Δi_L and generates a current to cancel Δi_L . The delay of inverted replica current i_R , however, creates a current offset that limits current multiplication factor M_I , which represents the ratio of Δi_L to the current ripple that reaches C_O ($\Delta i_{L(\text{eff})}$). For instance, M_I cannot exceed $12.5\times$ when the delay is 1% of switching period T_{SW} [14].

Predicting Δi_L can eliminate the systematic delay associated with a feedback loop. To that end, just as L_O produces triangular ripple Δi_L by integrating its square voltage v_L (i.e., $\Delta i_L = \int v_L/L_O dt$), C_T in the proposed circuit (Fig. 1) produces a triangular voltage Δv_C that emulates Δi_L by injecting a proportionally equivalent square current i_C into C_T (i.e., $\Delta v_C = \int i_C/C_T dt = \int v_L G_{M.S}/C_T dt$). Because v_P is in phase with v_{SW} and swings from 0 to V_{IN} , just as v_{SW} does and the converter regulates v_O to V_{REF} , the voltage that $G_{M.S}$ translates into i_C is roughly equivalent to v_L (i.e., $v_L \equiv v_{\text{SW}} - v_O \approx v_P - V_{\text{REF}}$). Therefore, converting Δv_C back to a current via transconductor $G_{M.T}$ produces the desired (and predicted) inductor-emulating replica current i_R (i.e., $I_R = \Delta V_C G_{M.T}$), as long as i_R 's amplitude matches Δi_L 's. The circuit ensures that the amplitudes are equal by tuning C_T , $G_{M.S}$, or $G_{M.T}$ to equate $C_T/(G_{M.S}G_{M.T})$ to L_O . Notice that the circuit automatically adjusts i_R to changes in V_{IN} and V_O (as it does i_L) because v_P and V_{REF} emulate v_{SW} and V_O , where v_P and v_{SW} carry V_{IN} .

The tuning process requires trimming, calibration during start-up and power-on-reset events, or an additional correcting low-bandwidth feedback loop to accommodate process variations in $G_{M.S}$, C_T , and L_O . In the prototype, the resistors that set $G_{M.T}$ were off chip and manually adjusted (trimmed) for testability and proof of concept. Employing negative feedback to continually tune the system, however, would also adjust for thermal and aging effects. Note that the bandwidth of such a correcting loop need not be high because its response time would not affect the converter and its multiplier during load dumps.

B. Two-Stage IC Embodiment

Replica current i_R must reach v_O in time to cancel Δi_L , so the transconductors must be fast. To ease their speed requirements, their switching input is derived from further back in the signal chain (i.e., with some lead time), from signal v_P instead of v_{SW} because v_P not only mimics (i.e., is in phase) but also slightly precedes v_{SW} . Additionally, $G_{M.S}$ must accommodate a rail-to-rail input common-mode range (ICMR) because v_P (as does v_{SW}) switches from ground to V_{IN} , and since $G_{M.T}$

generates i_R , $G_{M.T}$ must be efficient and able to source large currents (equivalent to Δi_L).

First-Stage Transconductor $G_{M.S}$: Achieving rail-to-rail ICMR operation with a standard differential pair is not trivial, which is why $G_{M.S}$'s input stage (Fig. 2) is slightly different. In this case, unity-gain amplifier A_{UG} ensures that the voltage across resistor R_i is $v_P - V_{\text{REF}}$, which, as mentioned earlier, is the equivalent of $v_{\text{SW}} - v_O$, so $G_{M.S}$ reduces to $1/R_i$. This way, the differential pair's input common-mode voltage is always at V_{REF} , which is considerably easier to accommodate, while allowing the overall circuit to sustain wide swings in v_P .

As v_P transitions from V_{IN} to zero, the current through R_i and M_{NdA} changes from $(V_{\text{IN}} - V_{\text{REF}})/R_i$ to $-V_{\text{REF}}/R_i$, increasing in one direction and decreasing in the other. Complementary differential transistor M_{NdB} therefore changes by the same amount but in the opposite direction. $M_{PmA} - M_{PmC}$ then mirrors M_{NdB} 's current to the output, where C_T integrates it. The square-wave voltage at v_P thus causes a square-wave current through R_i and a triangular voltage across C_T .

In practice, $G_{M.S}$'s average output current is not zero, and because v_T is a high-impedance node, v_T 's average voltage drifts to V_{IN} or ground, which means that mirror or bias-current transistors $M_{PmC} - M_{PcC}$ or $M_{NdC} - M_{NbE}$ are not saturated and distort v_T . A slow low-gain feedback loop is consequently included to regulate the dc voltage of this node well within the supplies. In Fig. 2, differential pair $M_{PdA} - M_{PdB}$ and current mirror $M_{NIA} - M_{NIC}$ comprise that feedback loop, which regulates v_T to a fraction of V_{IN} at $V_{\text{IN}} R_{bB}/(R_{bB} + R_{bA})$ or, in this case, $3V_{\text{IN}}/5$. This shunt-feedback loop also decreases the impedance at v_T but only within its bandwidth (as set by filters R_f and C_f and enhanced by the Miller effect through gain stage $M_{N1B} - M_{NcA} - R_a$), which is designed well below switching frequency f_{SW} . Maintaining the impedance high at f_{SW} is important to preserve v_T 's piecewise-linear shape. The prototype includes a series coupling capacitor C_s to allow v_T 's average to be externally controlled, without affecting the operation of the transconductor.

Second-Stage Transconductor $G_{M.T}$: With amplifier A_I in negative-feedback configuration (Fig. 4), $G_{M.T}$ superimposes triangular voltage v_T across R_1 , so the resulting triangular current i_C flows through M_{NfB} . $M_{NfB} - R_1$ drives sourcing output transistor M_{PmB} via input mirror transistor M_{PmA} . Thus, R_1 ultimately sets transconductance $G_{M.T}$. Similarly, $M_{NfC} - R_2$, which mirrors $M_{NfB} - R_1$, drives sinking output transistor M_{NmB} via M_{NmC} . Note that amplifiers A_{BUF1} and A_{BUF2} diode-connect (as unity-gain buffers) M_{PmA} and M_{NmC} to ensure that they mirror M_{NfB} and M_{NfC} 's currents. They accelerate the response of the output mirrors by decoupling the large parasitic capacitances at the gates of M_{PmB} and M_{NmB} from the drains of M_{NfB} and M_{NfC} , which exhibit high resistance. M_{NmC} is necessary to sink the difference between I_{BIAS} and I_{R1} and keep the current source transistors in saturation during the phase of v_T when v_R/R_1 is less than I_{BIAS} .

Since $G_{M.T}$ only drives an ac output current (i.e., i_R equals $-\Delta i_L$), its average must equal zero, which means that the circuit must cancel (subtract) the average current v_T 's dc component that V_T produces in M_{NfB} and M_{NfC} . M_{PbB} and M_{PbC} with M_{PbA} 's help accomplish this by sourcing $M_{NfB} - M_{NfC}$'s average current (i.e., M_{NfA} 's current) back into M_{NfB} and M_{NfC} . Notice that M_{NfA} 's gate voltage is

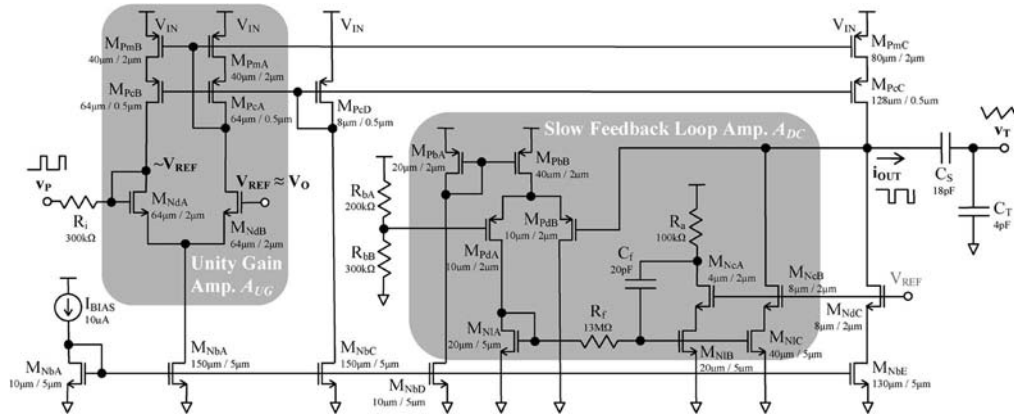


Fig. 2. Fully integrated (on-chip) first-stage transconductor $G_{M,S}$.

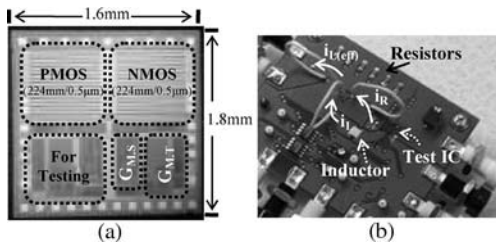


Fig. 3. (a) Die photograph. (b) PCB prototype.

a low-pass-filtered version of $M_{NfB}-M_{NfC}$'s, so $M_{NfA}-R_3$ mirrors $M_{NfB}-M_{NfC}$'s average current. As a result, when M_{NfB} 's or M_{NfC} 's instantaneous current rises above its average, M_{PmA} sources or M_{NmA} sinks the difference between its instantaneous and average currents, half-wave rectifying M_{PmA} and M_{NmA} 's respective out-of-phase drain currents and removing the dc component that V_T would otherwise produce in i_R . A dc offset here impacts both L_O 's current i_L and power dissipation, so the mirrors employ common-centroid geometries and include offset-reducing cascode transistors.

Integrated System: Fig. 3(a) presents the die photograph of the system, which includes $G_{M,S}$ and $G_{M,T}$, the complementary power switches of the buck converter, their respective drivers, dead-time logic, the proportional-to-the-absolute-temperature current-bias generator, various input-output buffers, and duplicates of individual blocks in the multiplier for testing purposes. While the entire die is $1.6 \times 1.8 \text{ mm}^2$, the power switches use most of the total area. Because no single V_{IN} -to- V_{OUT} conversion ratio was more important, the switches were designed to introduce no more than $300 \text{ m}\Omega$ and enlarged to exploit the die area available, which is why the aspect ratios of both n- and p-type transistors were $224 \text{ mm}/0.5 \text{ }\mu\text{m}$. Resistors R_1 , R_2 , and R_3 in Fig. 3(b), which determine transconductance $G_{M,T}$, are off chip and on the printed circuit board (PCB) to increase testing flexibility. Three extra resistors are needed to bias $G_{M,T}$'s duplicate circuit, so six resistors appear in total.

The prototyped PCB (Fig. 1) includes a series RC delay block in the converter path to match i_L 's total delay to i_R 's because $G_{M,S}$ and $G_{M,T}$'s combined bandwidth slows i_R more than large-power switches M_P and M_N delay i_L . This delay was manually adjusted in the experiments for testability and proof of concept, but a low-bandwidth feedback loop could au-

tomatically modify it. Nevertheless, the ability to equate delays in any way (with a slow correcting loop, for instance) highlights a key advantage that results from a feedforward-derived i_R , because the delay of a feedback-derived i_R is uncorrectable. Similarly, R_1 , R_2 , and R_3 in $G_{M,T}$ (Fig. 4) adjusts i_R 's amplitude to match i_L 's, and again, a low-bandwidth feedback loop could automatically tune them, so a calibration step during start-up and power-on-reset events would be unnecessary. Incidentally, notice that v_P in Fig. 1 is a good approximation of v_{SW} , except for the brief dead-time diode voltage drops in v_{SW} and the slight ohmic drops across M_P and M_N when conducting i_L . These variations, however, constitute negligible errors in i_R , when compared against the residual delay and nonlinearity of i_R .

IV. RESULTS

A. Inductor Multiplication

Although the technique is ultimately aimed at integrated inductors, the objective here is to test the viability and efficiency of CMOS inductor multiplication. Therefore, the system used a discrete $2 \times 2 \times 1 \text{ mm}^3$ $4.7\text{-}\mu\text{H}$ inductor and a 16-nF capacitor. Note that higher capacitances are typical because C_O suppresses output ripple, but the proposed circuit relaxes that requirement because a smaller C_O achieves similar performance with the proposed multiplier. Furthermore, note that L_O is nearly the size of the IC—as close to an integrated inductor as anything else readily available, except that integrated inductors today are not as good. Without the multiplier, when f_{SW} is 1 MHz , Δi_L and Δv_O were 216 mA and 1.76 V , and note that Δv_O is so large that (1) and (2) are no longer accurate. By contrast, when using a $47\text{-}\mu\text{H}$ inductor, Δi_L and Δv_O were 18.6 mA and 140 mV .

Fig. 5(a) illustrates the experimental waveforms of the inductor-multiplied buck converter with $4.7 \text{ }\mu\text{H}$ when I_O is 0.3 A . Note that i_R is inverted and superimposed on i_L to illustrate how well they match. They are nearly perfectly in phase and almost equal in amplitude. Fig. 5(b) shows the resulting $\Delta i_{L(\text{eff})}$, which flows into C_O . Combined, the results are comparable with those of the converter with $47 \text{ }\mu\text{H}$: $\Delta i_{L(\text{eff})}$ is 14.2 mA , and Δv_O is 68 mV . Current-mode multiplication factor M_I is therefore 10.8 ($154 \text{ mA}/14.2 \text{ mA}$), as also corroborated across a $0\text{--}830\text{-mA}$ load range but not shown because of space constraints.

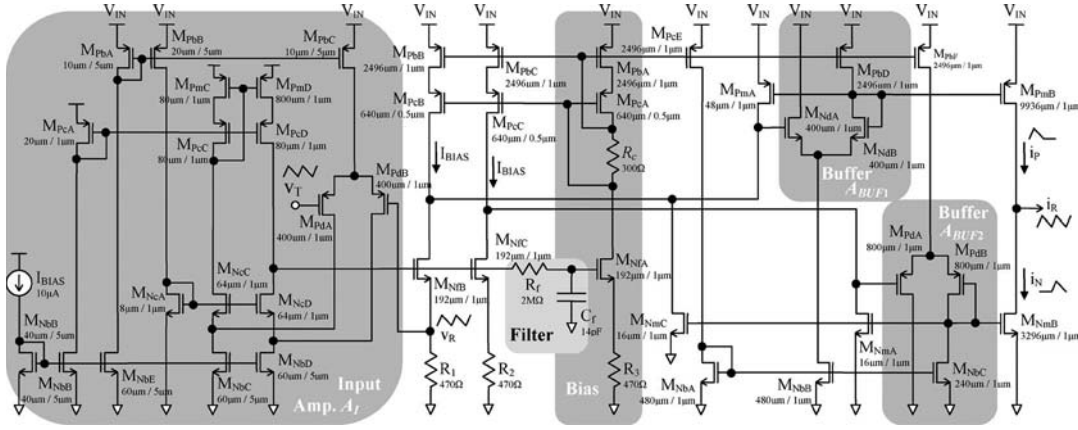


Fig. 4. Second-stage transconductor $G_{M.T}$ (R_1 , R_2 , and R_3 were off chip).

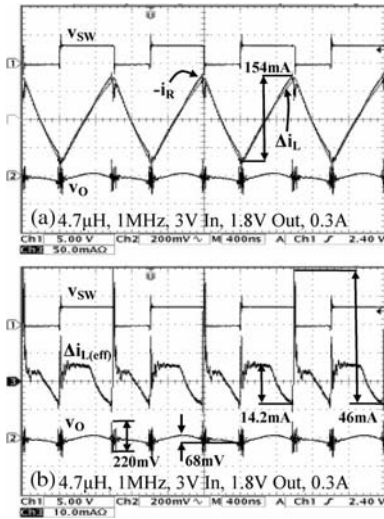


Fig. 5. Experimental (a) i_L , $-i_R$, and (b) $i_{L(\text{eff})}$ switching waveforms of the buck converter with the multiplier.

Notice that the graph of $-i_R$, although close to i_L 's, crosses i_L 's more than once per period as a result of crossover distortion in $G_{M.T}$, so $\Delta i_{L(\text{eff})}$, which only refers to $i_{L(\text{eff})}$'s ac portion, similarly crosses zero multiple times, developing higher frequency components in $\Delta i_{L(\text{eff})}$. Fortunately, because C_O 's impedance is lower at a higher frequency, ripple Δv_O is lower than expected. As a result, voltage-mode inductor multiplication factor M_V was 25.8 (1.76 V/68 mV), which is higher than M_I . Note that if C_O 's ESR R_{ESR} is high enough to overwhelm C_O 's capacitive droop, Δv_O would be the ohmic drop of $\Delta i_{L(\text{eff})}$ across R_{ESR} (i.e., $\Delta v_O \approx \Delta i_{L(\text{eff})} R_{\text{ESR}}$), so Δv_O would follow $\Delta i_{L(\text{eff})}$, and M_V would equal M_I . Nonetheless, both metrics verify that the proposed inductor multiplier outperforms a similar converter with ten times the inductance. Note the transient spikes in $\Delta i_{L(\text{eff})}$ and Δv_O , which measure 46 mA and 220 mV, are the products of high-frequency noise in the PCB that loads are often able to filter.

B. Power Efficiency

The multiplier (i.e., $G_{M.S}$, C_T , and $G_{M.T}$) is an additional circuit that dissipates power, particularly output power transistors M_{PmB} and M_{NmB} (in $G_{M.T}$ in Fig. 4) because they source and sink considerable current (i_R). The power lost

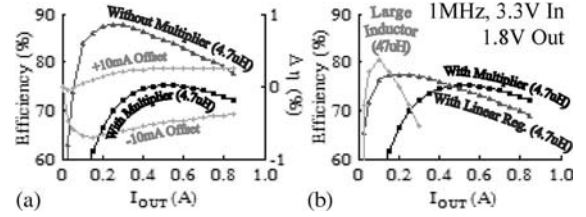


Fig. 6. Experimental efficiency of (a) the multiplier and (b) other schemes (the power lost in the series device in the linear regulator is simulated).

in M_{PmB} and M_{NmB} is proportional to the voltage across them and the portion of i_R they conduct. The voltages across M_{PmB} and M_{NmB} are nearly constant in steady state, and their respective ohmic power losses $P_{C.PmB}$ and $P_{C.NmB}$ [15] are

$$P_{C.PmB} = (V_{\text{IN}} - V_O) \left(\frac{\Delta i_R}{8} \right) \quad (3)$$

$$P_{C.NmB} = V_O \left(\frac{\Delta i_R}{8} \right). \quad (4)$$

In other words, most of the power lost in the multiplier is proportional to i_R and, by translation, Δi_L . Additionally, if i_R is offset by a small amount I_{OS} , the supply power will increase by approximately $0.5V_{\text{IN}}I_{\text{OS}}$ (e.g., 16.5 mW with 10-mA I_{OS}), but power equal to $V_{\text{IN}}\Delta i_{L(\text{eff})}I_{\text{OS}}$ will be supplied to the output. The difference, which may be negative, is additional loss incurred by the multiplier circuitry, but if the duty cycle is near 0.5, then the difference is very small. Although these losses cannot be neglected, they do not increase with I_O , unlike switching and dc conduction losses P_{SW} and $P_{C.DC}$ in the converter [15], i.e.,

$$P_{\text{SW}} = \frac{I_O V_{\text{IN}} t_x f_{\text{SW}}}{4} \quad (5)$$

$$P_{C.DC} = (R_{\text{SW}} + R_{L.\text{ESR}}) I_O^2 \quad (6)$$

where R_{SW} is the effective (total) switch resistance, $R_{L.\text{ESR}}$ is L_O 's ESR, and t_x is the switch transition time. $P_{C.DC}$ is slightly reduced if I_{OS} is positive and increased if I_{OS} is negative, but this affects efficiency by less than 1% [Fig. 6(a)]. All of this is to say that efficiency degradation is less severe at higher loads, because the output power increases but multiplier losses do not (Fig. 6(a): from 10% lower at 0.5 A to 5% lower at 0.8 A).

TABLE I
DESIGN SPECIFICATIONS AND FOM COMPARISON

	Proposed	[6]Resonant	[7]Hybrid	[11]FF i _R
V _O /V _{IN}	1.8V/3.3V	7V/3.6V	4V/9V	5V/12V
f _{SW}	1MHz	30MHz	145kHz	67kHz
#L _C	2	10	2	2
L•C	4.7μH•16nF	553nH•44nF	17μH•20μF	16μH•26μF
Δv _O	3.8%	1.1%	0.2%	0.8%
FOM	1	2.135	0.004	0.001

V. DISCUSSION

Although the multiplier significantly reduces Δi_L and Δv_O , it does so at the expense of efficiency. In all fairness, however, while increasing L_O may achieve the same ripple attenuation, power efficiency may likewise decrease with higher L_O 's because their ESRs are necessarily higher when constrained to the same volume. The 4.7- μ H inductor used, for example, has 280 m Ω of ESR (roughly equivalent to the ON-resistance of the switches), whereas the ESR of a 47- μ H inductor in a similar footprint is 2.18 Ω . As a result [Fig. 6(b)], the efficiency of the same converter with the larger inductor decreases at a faster rate with respect to increasing I_O than its multiplied counterpart (because $P_{C,DC}$ increases with I_O^2 , whereas multiplier losses remain constant). In this case, the multiplier is more efficient when I_O is greater than 250 mA.

Inductor multiplication also favorably compares with adding a linear regulator in series with the converter. For a fair comparison, the series regulator must step down the incoming voltage enough to keep its pass device in saturation when the ripple is at its negative peak. As a result, the power lost across the series device depends on the converter's Δv_O , which varies with C_O . Typical linear regulators, for instance, require a step-down (dropout) voltage of at least 300 mV ($V_{DS(sat)}$), so, at best, regulating the converter's output to 2.1 V (1.8 V + 300 mV) to accommodate the series regulator produces a loss that linearly increases with I_O , i.e.,

$$P_{C.MP(LDO)} = V_{DS(sat)} I_O. \quad (7)$$

The multiplier's loss remains unchanged as I_O increases; therefore, the multiplier outperforms the regulator past 450 mA. What is more, the linear regulator may not attenuate the ripple as much because its bandwidth, which determines power-supply rejection, does not typically extend far enough beyond the converter's f_{SW} to suppress noise. Nevertheless, since the multiplier is less efficient at light loads, sometimes, a hybrid of the two techniques may be optimal. Applying this technique to integrated inductors, which exhibit lower inductances and higher ESRs, is possible but with either lower accuracy or reduced efficiency because of higher Δi_L and Δv_O .

Ultimately, a comparison with the state of the art should normalize the application, but that is almost impossible. Still, comparing the number and size of passives (#L_C and $L_O C_O$) and accuracy (Δv_O) to the proposed (with #L_C, L'_O , C'_O , and $\Delta v'_O$) yields an informative figure of merit (FOM), i.e.,

$$\text{FOM} = \left(\frac{L'_O C'_O}{L_O C_O} \right) \left(\frac{\Delta v'_O}{\Delta v_O} \right) \left(\frac{\#L_C}{\#L_C} \right). \quad (8)$$

This FOM (Table I) indicates the proposed circuit compares favorably with [7] and [11] and slightly unfavorably with [6],

which relies on higher f_{SW} to keep $L_O C_O$ lower. However, [6] produces large oscillations at L_O 's switching node.

VI. CONCLUSION

This brief has proposed, presented, and experimentally verified a CMOS inductor current-ripple suppressor IC that reduced the current ripple of a discrete $2 \times 2 \times 1$ mm³ 4.7- μ H inductor by a factor of 10.8 and the converter's output voltage ripple by a factor of 25.8. Although the added quiescent power losses to the converter degraded the overall efficiency by 5% at the peak load, a 10 \times larger inductor in the same package degraded the converter efficiency even more (as a result of a higher ESR). Similarly, as load current increases, the power dissipated across the pass device $M_{P(LDO)}$ of a linear regulator, when added in series with the existing converter, eventually becomes even larger than the constant losses that the multiplier prototype incurs. Therefore, current-ripple suppression can avoid the high-ESR losses associated with high inductances constrained to small volumes by multiplying the low inductances of integrated inductors without degrading the accuracy of the converter, albeit with lower light-load efficiency.

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