A Single-Inductor 0.35-µm CMOS Energy-Investing Piezoelectric Harvester

Dongwon Kwon, *Member, IEEE*, and Gabriel A. Rincón-Mora, *Fellow, IEEE*
Georgia Institute of Technology, Atlanta, Georgia, U.S.A.
E-mail: dkwon3@gatech.edu and rincon-mora@gatech.edu
Address: 777 Atlantic Drive, Atlanta, GA 30332, U.S.A., Tel: (+1) 404-723-1376

Abstract—Although miniaturized piezoelectric transducers usually derive more power from motion than their electrostatic and electromagnetic counterparts, they still generate little power. The reason for this is that the electromechanical coupling factor is low, which means the damping force that tiny transducers impose on vibrations (when drawing power) is hardly noticeable. The single-inductor 0.35-µm CMOS piezoelectric harvester proposed in this paper counters this deficiency by investing energy from the battery into the transducer. The idea is to strengthen the electrostatic force against which vibrations work. This way, the circuit draws more power from the transducer, up to 79 µW from a 2.7-cm piezoelectric cantilever that is driven up to 0.25 m/s^2. Of the 79 µW drawn at 0.25 m/s^2 when investing 91 nJ of battery energy, the system outputs 52 µW, which is 3.6 times more output power than the 14.5 µW that a full-wave bridge rectifier with zero-volt diodes at its maximum power point can deliver from the same source. With 630 nW lost to the controller, power-conversion efficiency peaks at 69% when the harvester outputs 46 µW of the 67 µW it draws from the transducer at 0.25 m/s^2 when investing 0.8 nJ of battery energy.

Index Terms—Piezoelectric harvester, electrostatic damping force, energy investment, ambient vibration and motion, switched single-inductor ac–dc converter, switching supply, powering wireless microsensors, small miniaturized transducers.

I. Piezoelectric Harvesters

Wireless microsensors can add energy-saving and performance-enhancing intelligence to the human body, moving mechanical systems, and other inaccessible places, not to mention difficult-to-manage infrastructures like manufacturing plants, hospitals, and military camps [1]–[4]. Unfortunately, the batteries that these small systems can afford to incorporate are tiny and, as a result, easily exhaustible. This is a challenge because sending personnel to recharge or replace batteries is often impossible or prohibitively expensive, especially when considering a large network of devices. Luckily, energy in light, heat, electromagnetic radiation, and motion is vast, environmentally safe, and inexpensive. But more importantly, harvesting ambient power eliminates the bulky "tank" that fuel cells and batteries typically require.

Of possible sources, kinetic energy in motion is attractive because vibrations are abundant in the environment. This is why piezoelectric transducers are popular today, and because they generate more power from motion under similar space constraints than their electrostatic and electromagnetic counterparts [2]–[3]. With this technology, vibrations shift the molecular structure of piezoelectric materials to separate charge and establish a voltage across the surfaces. The electrostatic force that results then reinforces the elastic force of the material to work against vibrations. This way, the device draws energy in both the mechanical domain as potential energy and in the electrical domain as charge.

In a harvesting system, the transducer in Fig. 1a converts kinetic energy in motion E_{KE} into electrical energy E_{EE}. A harvester circuit then draws what it can from E_{EE} as input energy E_{IN} to output charge energy E_{CHG} with which to replenish a battery or a storage capacitor. Internally, the alternating current i_{PZ} and parallel capacitance C_{PZ} in Fig. 1b model how charges in the transducer establish the electrostatic force that dampens vibrations [4]. Resistance R_{LEAK} represents the dielectric leakage of the transducer, which is usually insignificant.

Unfortunately, the alternating voltages that vibrations produce across C_{PZ} cannot charge a battery or a capacitor directly. Modern systems resort to full- or half-wave diode-bridge rectifiers for this purpose. To reduce power consumption and the threshold voltage above which these rectifiers can draw current, engineers often replace asynchronous diodes with synchronous MOS switches [5]–[8]. But still, when vibrations are weak and transducers are tiny [9]–[10], piezoelectric voltages can be so low that diode-bridge rectifiers can only extract power when their rectified outputs v_{RECT} are impractically low. This constraint limits diode-bridge networks to applications that exhibit strong vibrations or that can accommodate large transducers.

Interestingly, diode-bridge networks generate maximum power when v_{RECT} is half of v_{PZ}'s open-circuit amplitude $v_{PZ(OC)}$. This is why [11]–[12] incorporate a switching converter and a capacitor C_{RECT} that decouples the battery voltage v_{BAT} from v_{RECT} and loads C_{RECT} only to the extent that v_{RECT} stays near its maximum power point. Since vibration strength can change with time, [11]–[12] also interrupt the harvesting process to monitor $v_{PZ(OC)}$ and adjust v_{RECT}. This approach is good for periodic vibrations whose $v_{PZ(OC)}$ hardly changes over time because the time between sacrificial refresh cycles can be long. $v_{PZ(OC)}$ for shock-induced and other random vibrations, however, changes from cycle to cycle, so halting the process to sense $v_{PZ(OC)}$ is less viable in these latter cases.

Another limitation to diode-bridge rectifiers is that i_{PZ} must first charge C_{PZ} to v_{RECT} before the system can clamp v_{PZ} to v_{RECT} and output power. In other words, i_{PZ} loses charge energy to C_{PZ} when transitioning v_{PZ} between $-v_{RECT}$ and $+v_{RECT}$. [13] cuts this requirement in half by discharging C_{PZ} to ground with a switch and using i_{PZ} to raise v_{PZ} to $-v_{RECT}$ or $+v_{RECT}$ from ground. Better yet, [13]–[14] drain C_{PZ} into a recycling inductor L_{RE} and use the energy deposited in L_{RE} to recharge C_{PZ} in the other direction. This way, the system recycles C_{PZ}'s energy and i_{PZ} can therefore flow almost continuously into v_{RECT}. For this, though, the system requires a full-wave diode-bridge rectifier, a switching converter that decouples v_{BAT} from v_{RECT},

a rectifying capacitor, and a recycling inductor along with its synchronizing network, which combined dissipate more power and occupy more space than its non-recycling predecessors.

Instead, [15]–[16] let i_{PZ} energize C_{PZ} across i_{PZ}'s half cycles and use an inductor to quickly drain C_{PZ} into a battery between half cycles. This way, the system discards the full-wave diode-bridge rectifier, the rectifying capacitor, and the recycling inductor to save energy and space. Still, the electrostatic force that small transducers establish is so poor that output power is low when vibrations are weak.

[17]–[18] invest energy into C_{PZ} to strengthen the electrostatic force and, as a result, draw more power from vibrations. For this, though, [17]–[18] require multiple off-chip inductors and a high battery voltage. The harvester simulated in [19], briefly presented in [20], and prototyped and evaluated here, however, invests, draws, and transfers energy with one inductor, two switches, and a controller. To comprehend the mechanics of the system, Section II explains how the harvester invests energy to draw more power from weak vibrations and Section III describes the integrated circuit (IC) fabricated for this purpose. Sections IV and V then evaluate and discuss measured performance and Section VI draws relevant conclusions.

II. Energy-Investing System

A. Role of Investment

Extracting power from kinetic energy in motion ultimately diminishes the effects of the propelling force. This means that harvesting energy opposes motion and, as a result, slows down the transducer. Therefore, boosting the opposing force that a transducer imposes draws more energy from movement. Except, raising this force beyond a critical threshold can damp motion to such an extent that movement ceases. Exceeding this critical damping point, however, is unlikely with small transducers because their electromechanical coupling factor is substantially low.

In the case of piezoelectric transducers, the charge across the piezoelectric capacitance C_{PZ} establishes the electrostatic force that converts kinetic energy E_{KE} in motion into static electrical

energy E_{EE} [18]. This means that recycling or investing battery energy to charge C_{PZ} strengthens the damping force with which the transducer opposes motion to convert more mechanical energy into the electrical domain. To see this, consider that linear changes in C_{PZ}'s voltage v_{PZ} produce quadratic changes in C_{PZ}'s energy $0.5C_{PZ}v_{PZ}^2$. So pre-charging C_{PZ} to V_{PC} with energy E_{PC} or $0.5C_{PZ}V_{PC}^2$ and allowing i_{PZ} to charge C_{PZ} further to $V_{PC} + \Delta v_{PZ}$ ultimately deposits $C_{PZ}\Delta v_{PZ}V_{PC}$ more energy than the $0.5C_{PZ}\Delta v_{PZ}^2$ that i_{PZ} can output without V_{PC}:

$$E_{NET} = E_{PZ(F)} - E_{PC} = 0.5C_{PZ}\left(V_{PC} + \Delta v_{PZ}\right)^2 - 0.5C_{PZ}V_{PC}^2 = 0.5C_{PZ}\Delta v_{PZ}^2 + C_{PZ}\Delta v_{PZ}V_{PC}, \quad (1)$$

where E_{NET} is the net energy delivered and $E_{PZ(F)}$ is C_{PZ}'s energy when v_{PZ} is $V_{PC} + \Delta v_{PZ}$. Note that this holds only as long as the transducer's opposing force is below the over-damping point.

B. Proposed Energy-Investing Harvester

In the proposed system in Fig. 2, switches M_{NPZ} and M_{PBAT} open across i_{PZ}'s positive half cycle to let i_{PZ} charge C_{PZ} to positive peak $v_{PZ(PK)+}$. M_{PBAT} then closes across investment time τ_I to deposit battery energy into inductor L_H, the result of which is to raise L_H's current i_L to roughly 20 mA. Next, M_{PBAT} opens and M_{NPZ} closes to drain C_{PZ}'s harvested energy into L_H across τ_{H+}. M_{NPZ} remains closed until L_H depletes all its energy (when i_L is zero) back into C_{PZ} to pre-charge C_{PZ} to negative pre-charge voltage $-V_{PC}$. In other words, the system invests battery energy and the energy harvested across i_{PZ}'s positive half cycle back into C_{PZ}, which means the transducer's electrostatic damping force is higher across i_{PZ}'s negative half cycle than across the positive counterpart.

After the investment process, M_{NPZ} and M_{PBAT} again open to allow i_{PZ} to charge C_{PZ} further in the negative direction. At the end of i_{PZ}'s negative half cycle, when v_{PZ} peaks at $-v_{PZ(PK)-}$, M_{NPZ} closes across τ_{H-} to discharge C_{PZ} into L_H. Afterwards, M_{NPZ} opens and M_{PBAT} closes across τ_{CHG} to drain L_H into the battery v_{BAT}.

Since transferring energy into and out of L_H only requires 7 µs of the 3.5-ms vibration period, the system can invest and harvest energy with just one inductor. Plus, because the switched

inductor does not need to clamp v_{PZ} to v_{BAT} to draw the energy harvested in C_{PZ}, the system can raise V_{PC} well above v_{BAT} and $v_{PZ(PK)+}$ to establish a higher damping force in the transducer. In practice, however, the transducer's critical damping point, the conduction and gate-drive losses that result from investing energy into C_{PZ}, and in extreme cases, the time required to invest energy ultimately limit V_{PC}.

In this process, the system recycles the energy harvested E_{H+} across i_{PZ}'s positive half cycle and draws battery energy $E_{I(BAT)}$ to invest E_{PC} or $0.5C_{PZ}V_{PC}^2$ into C_{PZ}. v_{BAT} therefore supplements E_{H+} in E_{PC} and also supplies the power that conduction, gate-drive, and quiescent losses E_{LOSS+} in the system consume to this point in the cycle:

$$E_{I(BAT)} = E_{PC} - E_{H+} + E_{LOSS+} = 0.5C_{PZ}V_{PC}^2 - 0.5C_{PZ}v_{PZ(PK)+}^2 + E_{LOSS+}. \quad (2)$$

At the end of i_{PZ}'s negative half cycle, L_H delivers the portion of C_{PZ}'s energy $0.5C_{PZ}v_{PZ(PK)-}^2$ that the system does not dissipate as losses E_{LOSS-} to v_{BAT} as E_{CHG}:

$$E_{CHG} = 0.5C_{PZ}v_{PZ(PK)-}^2 - E_{LOSS-}. \quad (3)$$

As a result, v_{BAT} receives the charge in E_{CHG} that v_{BAT} did not lose with $E_{I(BAT)}$:

$$E_{NET} = E_{CHG} - E_{I(BAT)} = 0.5C_{PZ}\left(v_{PZ(PK)-}^2 - V_{PC}^2 + v_{PZ(PK)+}^2\right) - E_{LOSS+} - E_{LOSS-}. \quad (4)$$

So if the effects of losses on v_{PZ} are minimal and those of damping are negligible, which is often the case in miniaturized transducers when stimulated with weak vibrations, $v_{PZ(PK)-}$ is roughly $V_{PC} + v_{PZ(PK)+}$ like Fig. 2 shows. E_{NET} therefore reduces to

$$E_{NET} = C_{PZ}v_{PZ(PK)+}^2 + C_{PZ}v_{PZ(PK)+}V_{PC} - E_{LOSS+} - E_{LOSS-}, \quad (5)$$

which is greater than the system can harvest when not investing energy to charge C_{PZ} to V_{PC}.

III. Integrated Circuit

The harvester proposed in Fig. 3 integrates the power switches from Fig. 2 with the controller into a 0.35-µm CMOS integrated circuit (IC). The 15-nF–10-MΩ transducer C_{PZ}–R_{PZ}, the 330-µH–1.6-Ω inductor L_H, the battery v_{BAT}, and the negative-peak detector that Schottky diode D_{SS}

and the 36-nF capacitor C_{SS} realize are off chip. The purpose of the negative-peak detector is to establish a substrate voltage that is sufficiently low to keep the body diodes of all NFETs in the system from inadvertently forward-biasing when C_{PZ}'s v_{PZ} falls below ground to $-v_{PZ(PK)-}$. The detector, however, is not necessary when isolated NFETs are available, or when another converter generates a negative bias voltage, as in [13]. The benefits of D_{SS} and C_{SS} over the competing alternatives are lower power, less silicon area, and the use of a more mainstream and less costly CMOS technology.

A. Power Stage

Power switches M_{NPZ} and M_{PBAT} in Fig. 3 are thick-oxide 15-V devices because their interconnecting terminals swing with v_{PZ} above v_{BAT} and below ground. Since L_H's current i_L momentarily peaks to milliamps to deliver microwatts on average to v_{BAT}, conduction losses can be significant, so M_{NPZ}'s and M_{PBAT}'s channel lengths are minimum at 1.5 μm. Channel widths are high at 40 and 90 mm to similarly reduce Ohmic losses, but not to the extent that higher parasitic gate capacitance requires more gate-drive power than wider transistors would save with lower conduction losses [23]. In other words, these channel widths should balance Ohmic and gate-drive losses.

NMOS Driver: Still, $-v_{PZ(PK)-}$ is so low with respect to ground that driving M_{NPZ}'s gate across v_{BAT} and $-v_{PZ(PK)-}$ dissipates considerable power. But since M_{NPZ}'s gate v_{GN} only needs a portion of $v_{PZ(PK)-}$, M_{NPZ}'s driver DRV_N in Fig. 4 produces no more than a voltage-divided fraction of what flying capacitor C_F samples when C_F connects across v_{BAT} and V_{SS}:

$$V_{DRV} = \left(v_{BAT} + |V_{SS}|\right)\left(\frac{C_F}{C_F + C_{GN}}\right), \tag{6}$$

where C_{GN} is M_{NPZ}'s gate capacitance, V_{DRV} is the voltage that C_F ultimately drives, and C_F sets V_{DRV} to $0.4(v_{BAT} + |V_{SS}|)$. So when v_{BAT} is 4 V and $-v_{PZ(PK)-}$ is –5.5 V, $|V_{SS}|$ is roughly 5.5 V and V_{DRV} is, as a result, about 3.8 V. For this, M_{PC} and M_{NC} close to charge C_F to $v_{BAT} + |V_{SS}|$ while

M_{TGND} grounds v_{GN} to open M_{NPZ} across i_{PZ}'s positive half cycle. Then, M_{PC}, M_{NC}, and M_{TGND} open and M_{PD} and M_{TD} close to connect C_F across v_{GN} and v_{PZ}. M_{NPZ} closes here because v_{GN} is at this point, as v_{PZ} transitions to $-V_{PC}$, above v_{PZ} by V_{DRV}. Then, the controller opens M_{PD} and M_{TD} and closes M_{TPZ} to connect v_{GN} to v_{PZ} and, as a result, open M_{NPZ} across i_{PZ}'s negative half cycle. When v_{PZ} peaks to $-v_{PZ(PK)-}$, the controller again closes M_{PD} and M_{TD} to close M_{NPZ} and therefore drain C_{PZ} into L_H.

This way, with a lower gate-voltage swing, the driver dissipates 8 of the 24 nJ that the circuit would have consumed had a conventional rail-to-rail inverter driven M_{NPZ}. In other words, the power that M_{NPZ} and its driver dissipate when gate-drive and Ohmic losses are optimally balanced for low power [23] is higher when swinging from V_{SS} to v_{BAT}. Here, as Fig. 4a shows, M_{NPZ}'s gate drive is also independent of v_{PZ} and, as a result, consistent across half cycles. M_{NPZ}'s peak gate voltage is also higher than the voltage (i.e., v_{BAT}) that a rail-to-rail driver would have established. This higher drive helps offset the unfavorable effect that M_{NPZ}'s body effect has on its threshold voltage v_{TN} and, ultimately, on its resistance the Ohmic power it dissipates.

Two PFETs in series with their N-well bulks attached to their intermediate junction implement M_{PC}, half of M_{TPZ}, and half of M_{TGND} to keep their body diodes from conducting when either terminal voltage rises above the other. M_{TD}, M_{TPZ}, and M_{TGND} are transmission gates because NFETs suffer from bulk effect to V_{SS} when v_{PZ} is positive and PFETs do not receive sufficient gate-drive voltages when v_{PZ} is negative. Because v_{GN} rises above and falls below v_{BAT} by more than one PMOS threshold voltage, cross-coupled PFET pair M_{P1}–M_{P2} in the high-voltage selector of Fig. 4b supplies the inverters that drive M_{TPZ2}–M_{TPZ3} and M_{TGND2}–M_{TGND3} with the higher voltage of the two voltages: v_{GN} or v_{BAT}. With the higher voltage, the inverters can keep the PFETs off when they should remain off. Note that the non-overlapping clock and the logic gates that drive M_{PD}, M_{TPZ}, and M_{TGND} keep adjacent switches from shorting supplies and dissipating shoot-through power.

PMOS Driver: Because M_{PBAT} in Fig. 3 connects to v_{BAT}, M_{PBAT}'s gate v_{GP} only needs to reach v_{BAT} and ground to open and close M_{PBAT}. This is why the supplies to the PMOS driver DRV_P in Fig. 5 are v_{BAT} and ground. Ground-connecting transistors M_{P5b} and M_{P5d} are P type to limit M_{PBAT}'s and M_{P5a}'s gate drives to v_{BAT} because NFETs would have connected their gates to V_{SS} and consumed, as a result, more gate-drive power. Plus, discharging their gates to ground keeps gate current from discharging C_{SS} and i_{PZ} from having to re-charge C_{SS} through D_{SS} in Fig. 3. Since M_{P5a} and M_{P5b} are large devices, separate inverter chains built with increasingly higher width–length transistors drive their gates. To keep M_{P5a} and M_{P5b} from conducting considerable shoot-through current, the first NAND gate in the series senses and waits until the other large transistor is off, the result of which is the introduction of "dead time" between transitions.

Ringing Suppressor: At the moment when the system opens M_{NPZ} and M_{PBAT} in Figs. 2 and 3, the switching node v_{SW} is either at $-V_{PC}$ or v_{BAT}. This means, v_{SW}'s parasitic capacitance C_{PAR} in Fig. 6 has remnant energy, so L_H can drain and recharge C_{PAR} until series resistances dissipate the energy. The purpose of M_{RS} in Fig. 3 and M_{N6a}–M_{P6b} in Fig. 6 is to ground v_{SW} when M_{NPZ} and M_{PBAT} open. Draining C_{PAR} suppresses the resonant oscillations that normally follow.

B. Controller

The comparator CP_{PK} in the peak-detector block of Fig. 3 senses when C_{PZ}'s v_{PZ} peaks to synchronize the system to i_{PZ}'s half cycles. When v_{PZ} rises in the positive half, for example, C_{PK} supplies current into R_{PK} to establish a positive voltage v_{RPK} across R_{PK}. But when v_{PZ} reverses and falls, C_{PK}'s current and R_{PK}'s v_{RPK} also reverse to trip CP_{PK} and raise v_{PK}. The control logic in Fig. 7 then pulls $v_{GP(INV)}$ high to close M_{PBAT}, and as a result, draw battery energy into L_H. v_{DLY} in the tunable delay τ_I in Fig. 3 then determines how long v_{BAT} energizes L_H. So after v_{DLY} rises, the logic in Fig. 7 responds by opening M_{PBAT} when $v_{GP(INV)}$ falls and closing M_{NPZ} when $v_{GP(MON)}$ and v_{GGND} fall, commanding the system to drain C_{PZ} into L_H. When L_H's i_L is close to

zero, which happens when the inductor depletes, comparator CP_{LD} in Fig. 3 raises v_{LD} to disable CP_{LD} and prompt the logic in Fig. 7 to raise v_{GPZ} and, in consequence, open M_{NPZ}.

As v_{PZ} falls in the negative half, C_{PK} continues to pull current from R_{PK} to produce a negative voltage in v_{RPK}. When v_{PZ} reverses and rises, C_{PK}'s current and R_{PK}'s v_{RPK} also reverse to trip CP_{PK}, lower v_{PK}, and reset v_{GPZ} low. This closes M_{NPZ} and drains C_{PZ} into L_H. After τ_{H-} in Fig. 3 lapses, v_{DLY} transitions low to raise v_{GGND} and open M_{NPZ}. Stored energy in L_H in the form of i_L then drives switching node v_{SW} above v_{BAT} until the charge-control comparator CP_{CHG} in Fig. 3 trips, which then lowers v_{CHG} and raises $v_{GP(HARV)}$. This ultimately closes M_{PBAT} to drain L_H into v_{BAT}, until CP_{CHG} senses that L_H's i_L produces close to zero volts across M_{PBAT}. At this point, v_{CHG} rises and $v_{GP(HARV)}$ drops to open M_{PBAT} again and start another harvesting cycle.

Peak Detector: Peak-detecting comparator CP_{PK} in Fig. 3 consists of two identical comparators CP_{PK+} and CP_{PK-} from Fig. 8. When v_{PK} is low across i_{PZ}'s positive half cycle, CP_{PK-} is off and CP_{PK+} detects when v_{PZ} peaks to $v_{PZ(PK)+}$. CP_{PK+}'s output v_{O+} sets the latch, which in turn disables CP_{PK+}, prompts the system to invest v_{BAT} energy into L_H, and then enables CP_{PK-} after about 100 µs. This 100-µs delay keeps the comparators from tripping erroneously when M_{NPZ} and M_{PBAT} switch. Across i_{PZ}'s negative half cycle, CP_{PK-} monitors v_{PZ} and trips when v_{PZ} reaches $-v_{PZ(PK)-}$. At this point, CP_{PK-}'s output v_{O-} resets the latch to disable CP_{PK-}, send a command to deplete C_{PZ} into L_H, and enable CP_{PK+} after another deglitch period.

Since R_{PK} connects to ground and the voltage that R_{PK} drops is not substantial, a PMOS differential pair M_{P8a}–M_{P8b} in Fig. 8 senses R_{PK}'s v_{RPK} and feeds an NMOS mirror M_{N8a}–M_{N8b}, and together they drive a common-source transistor M_{N8c}. Because M_{N8c} pulls v_{O8b} quickly and bias transistor M_{P8g} slews v_{O8b}, the inputs of CP_{PK+} and CP_{PK-} connect to C_{PK} and R_{PK}, so that M_{N8c} pulls v_{O8b} when v_{PZ} peaks. This way, the comparators respond quickly. M_{P8j} steers an offset current into M_{N8a}–M_{N8b} when v_{O8b} is low to establish hysteresis after v_{PZ} peaks in the form of an

intentional input-referred offset. The purpose of the hysteresis is to keep noise in the slow analog inputs from inadvertently tripping CP_{PK+} and $CP_{PK–}$.

Tunable Delays: The SR-latches in Fig. 9 coordinate and synchronize which and when delay times τ_I and $\tau_{H–}$ from Fig. 3 start. V_{INV} and V_{HARV} adjust how much current flows through R_I and R_H and into C_{RAMP} to set the delay times τ_I and $\tau_{H–}$ that C_{RAMP}'s v_{RAMP} requires to trip M_{N9e}. This way, when v_{PK} in Fig. 3 transitions high at the end of i_{PZ}'s positive half cycle, the Invest latch in Fig. 9 closes M_{P9c}–M_{N9c} to steer R_I's current into C_{RAMP}, and after τ_I, M_{N9e} trips and sets the output latch to generate a high end-of-delay signal v_{DLY}. Similarly, the Harvest latch prompts M_{P9d}–M_{N9d} to steer R_H's current into C_{RAMP} to establish $\tau_{H–}$.

M_{N9e} and M_{N9g} form a positive-feedback loop at v_{O9a} that accelerates v_{O9a}'s falling transition. v_{O9a} therefore falls more quickly than v_{RAMP} rises, and the output inverters, as a result, conduct less shoot-through current during the transition. M_{N9e} does not trip until v_{RAMP} is high enough for M_{N9f} to sink M_{N9e}'s 3 nA and M_{N9g}'s 30 nA. When M_{N9f} sinks more than 33 nA, v_{O9a} falls and M_{N9g} opens. As a result, M_{N9e} now pulls v_{O9a} with more current, which expedites v_{O9a}'s fall.

Inductor Energy-Drain Sensor: CP_{LD} in Figs. 3 and 10 senses when L_H depletes by monitoring the current that v_{PZ} establishes through C_S. So as L_H drains into C_{PZ} at the end of i_{PZ}'s positive half cycle, v_{PZ} falls and C_S responds by pulling current from the input of P-type mirror M_{P10a}–M_{P10c} in Fig. 10. M_{P10b} therefore generates voltage v_S across R_S that keeps CP_{LD}'s output v_{LD} low. When L_H depletes all the energy into C_{PZ}, v_{PZ} stops falling, C_S's current drops to nearly zero, and with no current to drive v_S, v_S falls to zero. Since M_{P10c}'s current establishes an offset v_{OS10} across C_{OS} for CP_{LD} that overwhelms CP_{LD}'s inherent offset and rises with v_{PZ}'s transition rate, v_S's fall to zero trips CP_{LD}. This raises v_{LD} and alerts the system that L_H no longer stores energy. Producing an offset v_{OS10} that is higher when v_{PZ} transitions more quickly overdrives CP_{LD}, which accelerates CP_{LD}'s response.

Since CP_{LD}'s inputs hover about ground and response time is only important in one direction, CP_{LD}, CP_{PK+}, and CP_{PK-} share the circuit architecture in Fig. 8. But because CP_{LD}'s speed requirements differ from those of CP_{PK+} and CP_{PK-}, width–length ratios and bias currents are different. In this case, the system enables CP_{LD} when M_{NPZ} closes and the latch in Fig. 10 disables CP_{LD} (after CP_{LD} trips to raise v_{LD}). For a faster response, I_{BLEED}'s 1.5 nA keeps the input mirror M_{P10a} from shutting completely. Note that C_S is so much lower than C_{PZ} that C_S hardly affects v_{PZ}.

Charge Control: The circuit in Fig. 11 implements the charge-control comparator CP_{CHG} in Fig. 3. Here, gate-coupled differential pair M_{P11a}–M_{P11b} senses the voltage across M_{PBAT} in Fig. 3, and mirror M_{N11a}–M_{N11b} ensures that M_{P11a}'s and M_{P11b}'s drain currents equal when M_{PBAT}'s voltage v_{SDP} or $v_{SW} - v_{BAT}$ is zero. This way, when v_{SW} surpasses $v_{BAT,}$ M_{P11a}'s current exceeds M_{N11a}'s to raise v_{O11a}, lower v_{CHG}, and close M_{PBAT}, which begins draining L_H into v_{BAT} through M_{PBAT}'s channel. At this point, M_{P11e} raises v_{OS11} to establish an offset current i_{OS} that M_{P11a} must supply to keep v_{O11a} high. So as L_H's i_L drops, v_{SW} and v_{SDP} fall. When M_{P11a}'s current falls below M_{N11a} and M_{N11i}'s combined current, v_{O11a} then drops and v_{CHG} rises to open M_{PBAT} and reset both v_{OS11} and i_{OS} to zero.

Since L_H's i_L raises v_{SW} quickly when L_H first starts to drain, M_{P11a} can supply considerable current into v_{O11a}, so the circuit can close M_{PBAT} quickly. The purpose of i_{OS} is to help the other transition, to begin transitioning v_{O11a} low when v_{SW} is slightly above v_{BAT}. Starting early gives the circuit time to open M_{PBAT} before v_{SW} falls below v_{BAT}, which would otherwise drain energy from v_{BAT} into L_H. But since M_{P11e} raises v_{OS11} only after v_{O11a} transitions high, i_{OS} does not affect the rising trip point of the circuit. If M_{PBAT} opens early, L_H's i_L raises v_{SW} to the point that M_{PBAT}'s body diode forward-biases and finishes draining L_H into v_{BAT}. The purpose of the diode-connected stack M_{N11d}–M_{N11e} is to clamp v_{O11a}. This way, v_{O11a} requires less transition time to

open M_{N11c} and open M_{PBAT}. After M_{PBAT} opens, the system disables CP_{CHG} to save energy and keep remnant energy in L_H from inadvertently tripping CP_{CHG}.

C. Bias-Current Generators

The nano-amp PTAT current generator in Fig. 12 biases CP_{PK}, the tunable-delay block, and the inductor energy-drain sensor. Here, mirror M_{N12a}–M_{N12f} ensures M_{P12a}–M_{P12b} currents match at I_{BIAS} and M_{P12f}'s current is at $2I_{BIAS}$. This way, M_{P12a} and M_{P12b} impress the gate–source-voltage difference that their width–length ratios establish across M_{P12e} to bias M_{P12e} in triode [21], whose resistance is about 18 MΩ. To avoid a zero-current state, M_{N12i}–M_{N12j} mirrors I_{BIAS} to a stack of diode-connected PFETs that raises v_{START} when I_{BIAS} is zero, in which case the circuit steers startup currents i_{ST1} and i_{ST2} into the PTAT bias core. As a result, I_{BIAS} is 1.2 – 3.6 nA when measured across 2.5 – 12.5-V supplies at room temperature.

The micro-amp PTAT current generator in Fig. 13 is inside both CP_{LD} and CP_{CHG}. As with the nano-amp version, M_{N13a}–M_{N13b} ensures that M_{P13a}–M_{P13b} currents match at I_B, and M_{P13a}–M_{P13b} impresses a gate–source-voltage difference across R_{PTAT} to set I_B to roughly 2 μA at room temperature. When disabled, M_{P13f} is open and M_{N13c} pulls v_{ST} low to charge C_{ST}. So when enabled, M_{P13f} closes and v_{ST}, M_{P13d}, M_{P13e}, and R_{ST} define a current i_{ST} that flows into the PTAT bias core to start the circuit [22]. M_{P13c} mirrors I_B and pulls v_{ST} to the supply when I_B is not zero to open M_{P13e} and shut i_{ST}. This way, I_B settles within 1 μs under all measured conditions.

IV. Measured Performance

Fig. 14 shows the fabricated 1.8 × 1.3 mm^2 0.35-μm CMOS die and the prototyped 4.2 × 3.3 × 0.16 cm^3 board used to test the system. Power transistors M_{NPZ} and M_{PBAT} are against the upper edge and corners of the die to keep metal lengths in the power path short and the substrate noise that the transistors generate away from noise-sensitive blocks. To further reduce crosstalk, the power transistors and the analog blocks connect to the negative supply V_{SS} via separate bond pads, bond wires, and pins. Although they all share the same substrate, "star" connecting them

this way reduces the impact of noise in one on the other. The HSMS-2800 Schottky diode and the 36-nF SMD capacitor that establishes V_{SS} are on the bottom side of the board. A V22b transducer from Mide Technology that integrates $25.4 \times 3.8 \times 0.25$ mm^3 of piezoelectric material inside a 2.7-cm cantilever attaches to the board, which a plastic bolt fixes to a 4810 mini-shaker shaker from Brüel & Kjær. A slide switch enables and disables the system and an LK-G87 displacement sensor from Keyence Corporation monitored the movements of the transducer.

A. Charging Performance

As Fig. 15a shows, the prototype charges 475 nF from the vibrations that would otherwise produce open-circuit piezoelectric voltages $v_{PZ(OC)}$ between 0.57 and 2.0 V from acceleration rates at the base of the cantilever between 0.06 and 0.21 m/s^2. Since the harvester invests battery energy when v_{PZ} peaks to $v_{PZ(PK)+}$ and charges v_{BAT} when v_{PZ} bottoms at $v_{PZ(PK)–}$, v_{BAT} steps down at the end of the positive half cycle and up at the end of the period. With the investment time τ_I fixed at 1.9 µs, harvested output power rises with stronger vibrations to raise v_{BAT}. When vibrations are weak at 0.06 m/s^2, however, the system only generates enough energy to cover the investment and losses. This is why v_{BAT} in Fig. 15a generally rises as long as accelerations are above 0.06 m/s^2.

Although v_{BAT} still rises in Fig. 15b when τ_I is 0.34 µs, the investment time is so short that v_{BAT} hardly invests energy. Under this condition, the system only re-invests what C_{PZ} collects across i_{PZ}'s positive half cycle to raise v_{BAT} in Fig. 15b to 3.61 V at 60 ms (and with more time, to higher voltages). With τ_I at 1.42 and 1.82 µs, however, v_{BAT} invests and collects more energy to rise to 3.71 and 3.72 V. Raising τ_I to 2.53 µs reverses the improvement because power losses at this point outpace gains from investment.

B. Power Performance

As Fig. 16a shows, the system draws up to 79 µW of input power P_{IN} from the transducer when driven with up to 0.25 m/s^2 and investing 91 nJ of battery energy and delivers as much as 52 µW

of output power P_O to v_{BAT}. When the system only re-invests harvested power, when $E_{I(BAT)}$ is close to nil at 0.8 nJ and vibrations are still at 0.25 m/s^2, P_{IN} is 67 μW and P_O is 46 μW. P_{IN} climbs with higher $E_{I(BAT)}$ because the electrostatic force with which the transducer extracts power from motion rises with $E_{I(BAT)}$. P_O, however, does not rise to the same degree because losses in the system also climb with $E_{I(BAT)}$. Vibrations are so weak when $v_{PZ(OC)}$ is 0.61 V, in fact, that P_O in Fig. 16b falls with additional battery investments. With stronger vibrations, v_{BAT} recovers investments when $v_{PZ(OC)}$ is 1.02 V and collects more energy than it invests when $v_{PZ(OC)}$ is 2.62 V.

C. Power-Conversion Efficiency

The reason power losses rise with battery investments $E_{I(BAT)}$ is that switches consume more Ohmic power P_{COND} when they deliver more output power P_O, as Fig. 17a shows when raising vibration strength. As a result, power-conversion efficiency η_{IC} or P_O/P_{IN} across the IC in Fig. 17b falls with higher investments. η_{IC}, however, rises with P_O to 66% – 69% because increases in P_O outpace those of P_{COND}. η_{IC} drops quickly when P_O falls below roughly 5 μW because, while P_{COND} scales with P_O, quiescent and gate-drive power P_Q and P_{GD} do not. In other words, P_Q and P_{GD} are constant and dominate when P_{COND} drops, in this case, below roughly 3 μW.

Efficiency does not actually peak because conduction and gate-drive losses P_{COND} and P_{GD} in M_{NPZ} and M_{PBAT} never balance across P_O. Increasing their widths, which lowers resistance and P_{COND} and raises gate capacitance and P_{GD}, should yield higher efficiency. The drawback to raising P_{GD} is that vibrations must be strong enough to produce more power than P_{GD}. In other words, the threshold above which accelerations must rise to output a positive power is higher with more P_{GD}. As is, CP_{PK}, the tunable-delay block, and the nano-amp generator, which operate continuously, consume 0.3 – 0.5 μW, and duty-cycled blocks CP_{LD} and CP_{CHG} dissipate 45 – 116 nW, so the system outputs power when accelerations exceed 0.06 m/s^2. Although the transducer

model used to simulate the system was imperfect, measured power losses follow those obtained from simulations and predicted by calculations presented in [15].

V. Context and Limitations

Piezoelectric transducers generate the most power when they vibrate at their resonant frequency. Unfortunately, motion is not always consistent or periodic. Many applications, in fact, vibrate in response to shocks, or repeated impact. This means that vibration strength peaks at the onset of an event and falls with time afterwards. Because the prototype senses v_{PZ} and synchronizes the system to v_{PZ} across i_{PZ}'s half cycles, the system automatically adjusts to variable conditions. This is why tapping the bolt head of the board in Fig. 14b three times charged 475 nF in Fig. 18a to about 3.9 V. But since this system cannot adjust the battery investment automatically from cycle to cycle, and it cannot afford to lose the power necessary to transfer battery energy when vibrations are weak, the system only re-invests harvested energy in Fig. 18. As a result, v_{BAT} never falls in Fig. 18b, because the battery never invests energy. In this case, when only re-investing the harvested energy, M_{PBAT} in Figs. 2 and 3 can operate like an asynchronous diode, which simplifies the controller and reduces power losses in the controller.

Since energy in the piezoelectric capacitance C_{PZ} rises linearly with C_{PZ} and quadratically with C_{PZ}'s open-circuit voltage $V_{PZ(OC)}$, and higher vibrating frequencies f_{VIB} deliver this energy more often, output power P_O naturally climbs with C_{PZ}, $V_{PZ(OC)}^2$, and f_{VIB}. This, and because $C_{PZ}V_{PZ(OC)}^2f_{VIB}$ is the maximum power that a lossless full-wave diode-bridge rectifier can output [11]–[13], is why the figure of merit (FoM) in Table I is higher when P_O is high and C_{PZ}, $V_{PZ(OC)}$, and f_{VIB} are low. In this light, the energy-investing prototype presented here outputs 4 to 4.5 times more power than its non-investing switched-inductor predecessor in [15].

Under similar conditions, this technology delivers 3.6 times more power at 52 µW in Fig. 16a when battery-investment energy $E_{I(BAT)}$ is 91 nJ than a full-wave bridge rectifier with zero-volt diodes at its maximum power point can at 14.5 µW from the same source. Even when only re-

investing harvested energy, when $E_{I(BAT)}$ is close to nil at 0.8 nJ, the system still outputs 3.2 times more power. This means that investing battery energy in addition to the re-investment of the harvested energy outputs 13% more power than when only re-investing harvested energy. Similarly, the recycling full-wave bridge rectifier in [13] delivers more power than its non-recycling counterparts because a switched inductor re-invests harvested energy into the transducer. Still, the switched-inductor presented here delivers 20% more power than [13] because it can draw additional investment energy from the battery. Plus, while the system here adjusts to aperiodic vibrations, the rectifier in [13] with the recycling inductor cannot.

Investing energy in this system amounts to pre-charging the capacitance across the transducer. But because junctions and gate oxides break down at about 15 V, the system cannot invest more than this level. Plus, since the components that deliver the investment dissipate power, returns on investment must exceed losses for output power to rise. Satisfying this prerequisite is more difficult when vibrations are weak. This is why P_O in Fig. 16b falls with higher investments when vibrations are weak at 0.07 m/s^2. In other words, investing battery energy raises output power when vibrations are periodic and moderate to strong, and when power-conversion efficiency across the system is high. In the case of the prototyped system, investing battery energy no longer helps when accelerations fall below 0.06 m/s^2.

Ultimately, investing battery energy raises the electrostatic damping force in the piezoelectric transducer, so the system draws more power from motion. This additional force works against vibrations to reduce the displacement distance of the transducer's tip by roughly 1.3% from 634 to 626 μm, as Fig. 19 shows. Thankfully, the damping force is never high enough to reach the threshold beyond which drawn power fails to climb. In fact, the coupling factor of miniaturized transducers is so low that reaching this critical damping point is highly unlikely. The situation can change, however, when transducers are larger and better, that is to say, when coupling factors are higher.

VI. Conclusions

The prototyped 0.35-µm CMOS harvester presented here harnesses 79 µW from a 2.7-cm piezoelectric cantilever to deliver 52 µW to a battery. This is 3.6 times more power than a full-wave bridge rectifier with zero-volt diodes at its maximum power point can at 14.5 µW from the same 0.25-m/s^2 vibrations. For this improvement, the system invests harvested energy collected across the positive half cycle and another 91 nJ from the battery into the piezoelectric transducer. Although returns on investments diminish when vibrations weaken because the system dissipates power when transferring the investment, investing energy still raises output power for accelerations higher than 0.06 m/s^2. In other words, investing energy raises the mechanical-to-electrical energy-conversion efficiency of the transducer. This holds true as long as the system does not over-damp vibrations, which is unlikely in miniaturized transducers because coupling factors are low. Although the harvester can also harness energy from shocks, the system cannot adjust the battery investment "on the fly", so re-investing harvested energy is better in these cases. Still, many applications like motors produce periodic or semi-periodic vibrations. Factories, hospitals, and a host of other applications can therefore enjoy more benefits, because drawing more power from motion allows wireless microsensors to incorporate more intelligence.

Acknowledgement

The authors thank Bryan Legates and Linear Technology for their support and sponsorship.

REFERENCES

[1] R.J.M. Vullers, R. van Schaijk, H.J. Visser, J. Penders, and C. Van Hoof, "Energy harvesting for autonomous wireless sensor networks," *IEEE Solid-State Circuits Magazine*, vol. 2, issue 2, pp. 29–38, 2010.

[2] S.P. Beeby, M.J. Tudor, and N.M. White, "Energy harvesting vibration sources for Microsystems applications," *Meas. Sci. Technol.*, vol. 17, pp. R175–R195, 2006.

[3] P.D. Mitcheson, E.M. Yeatman, G.K. Rao, A.S. Holmes, and T.C. Green, "Energy harvesting from human and machine motion for wireless electronic devices," *Proceedings of the IEEE*, vol. 96, no. 9, pp. 1457-1486, Sept. 2008.

[4] S. Priya and D.J. Inman, *Energy Harvesting Technologies*, New York, NY: Springer Science+Business Media, LLC 2009.

[5] T.T. Le, J. Han, A. von Jouanne, K. Mayaram, and T.S. Fiez, "Piezoelectric micro-power generation interface circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1411–1420, June 2006.

[6] Y.-H. Lam, W.-H. Ki, and C.-Y. Tsui, "Integrated low-loss CMOS active rectifier for wirelessly powered devices," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 53, no. 12, pp. 1378–1382, Dec. 2006.

[7] S. Guo and H. Lee, "An efficiency-enhanced CMOS rectifier with unbalanced-biased comparators for transcutaneous-powered high-current implants," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1796–1804, June 2009.

[8] J.L. Wardlaw, A.İ. Karşılayan, "Self-powered rectifier for energy harvesting applications," *IEEE J. Emerging and Selected Topics in Circuits Syst.*, vol. 1, no. 3, pp. 308–320, Sept. 2011.

[9] M. Marzencki, Y. Ammar, and S. Basrour, "Integrated power harvesting system including a MEMS generator and a power management circuit," in *Proc. IEEE Int. Solid-State Sensors, Actuators, and Microsystems Conf.*, pp. 887–890, June 2007.

[10] E.E. Aktakka, R.L. Peterson, and K. Najafi, "A CMOS compatible piezoelectric vibration energy scavenger based on the integration of bulk PZT films on silicon," in *Proc. IEEE Int. Electron Devices Meetings,* Dec. 2010.

[11] C. Lu, C.-Y. Tsui, and W.-H. Ki, "Vibration energy scavenging system with maximum power Tracking for Micropower Applications," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.*, vol. 19, no. 11, pp. 2109–2119, Nov. 2011.

[12] A. Tabesh and L.G. Fréchette, "A low-power stand-alone adaptive circuit for harvesting energy from a piezoelectric micropower generator," *IEEE Trans. Industrial Electronics*, vol. 57, no. 3, pp. 840–849, March 2010.

[13] Y.K. Ramadass and A.P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[14] D. Guyomar, A. Badel, E. Lefeuvre, and C. Richard, "Toward energy harvesting using active material and conversion improvement by nonlinear processing," *IEEE Trans. Ultrasonics, Ferroelectronics, and Frequency Control*, vol. 52, no. 4, pp. 584–595, Apr. 2005.

[15] D. Kwon and G.A. Rincón-Mora, "A 2-µm BiCMOS Rectifier-Free AC–DC Piezoelectric Energy Harvester-Charger IC," *IEEE Trans. Biomedical Circuits Syst.*, vol. 4, no. 6, pp. 400–409, Dec. 2010.

[16] T. Hehn, F. Hagedorn, D. Maurath, D. Marinkovic, I. Kuehne, A. Frey, and Y. Manoli, "A Fully Autonomous Integrated Interface Circuit for Piezoelectric Harvesters," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, Sept. 2012.

[17] M. Lallart and D. Guyomar, "Piezoelectric conversion and energy harvesting enhancement by initial energy injection," *Appl. Phys. Lett.*, vol. 97, pp. 014104-1–014104-3, 2010.

[18] J. Dicken, P.D. Mitcheson, I. Stoianov, and E.M. Yeatman, "Increased power output from piezoelectric energy harvesters by pre-biasing," *Proc. PowerMEMS*, pp. 75–78, Dec. 2009.

[19] D. Kwon and G.A. Rincón-Mora, "Energy-investment schemes for increasing output power in piezoelectric harvesters," in in *Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, pp. 1084–1087, Aug. 2012.

[20] D. Kwon and G.A. Rincón-Mora, "A Single-inductor 0.35-µm CMOS energy-investing piezoelectric harvester," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 78–79, Feb. 2013.

[21] H.J. Oguey and D. Aebischer, "CMOS current reference without resistance," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1132–1135, July 1997.

[22] Q.A. Khan, S.K. Wadhwa, and K. Misri, "Low power startup circuits for voltage and current reference with zero steady state current," in *Proc. Int. Symp. Low Power Electron. Design (ISLPED)*, pp. 184–188, 2003.

[23] S. Kim and G.A. Rincón-Mora, "Achieving high efficiency under micro-watt loads with switching buck dc-dc converters," *Journal of Low Power Electronics (JOLPE)*, vol. 5, no. 2, pp. 229–240, Aug. 2009.

FIGURE CAPTIONS

Fig. 1. (a) Piezoelectric harvester and (b) transducer model.

Fig. 2. Prototyped energy-investing switched-inductor power stage and corresponding waveforms measured.

Fig. 3. Prototyped energy-investing piezoelectric harvester.

Fig. 4. M_{NPZ}'s driver DRV_N (a) network and corresponding waveforms measured and (b) schematic, where transistor dimensions are μm/μm and unspecified body terminals connect to their corresponding supplies.

Fig. 5. M_{PBAT}'s driver DRV_P.

Fig. 6. Ringing suppressor.

Fig. 7. Control logic for (a) M_{PBAT}'s DRV_P and (b) M_{NPZ}'s DRV_N and (c) their corresponding waveforms.

Fig. 8. Peak detector.

Fig. 9. Tunable delays.

Fig. 10. Inductor energy-drain sensor and corresponding waveforms measured.

Fig. 11. Charge-control comparator CP_{CHG}.

Fig. 12. Nano-amp PTAT bias-current generator.

Fig. 13. Micro-amp PTAT bias-current generator in CP_{LD} and CP_{CHG}.

Fig. 14. 0.35-μm CMOS die fabricated, evaluation board prototyped, and corresponding experimental setup.

Fig. 15. Measured charge profile of a 475-nF capacitor across (a) vibration strength and (b) battery investment.

Fig. 16. Measured input and output power P_{IN} and P_O across (a) vibration strength and (b) battery investment.

Fig. 17. (a) Measured power losses across output power and (b) corresponding power-conversion efficiencies across battery investment.

Fig. 18. Measured charge profile of a 475-nF capacitor when tapped with a finger (a) three times and (b) one time across a finer time scale.

Fig. 19. Variation of cantilever's tip displacement across battery investment and resulting input power drawn.

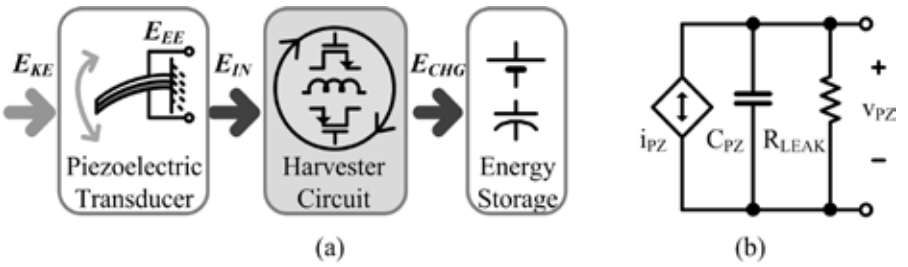

Fig. 1. (a) Piezoelectric harvester and (b) transducer model.

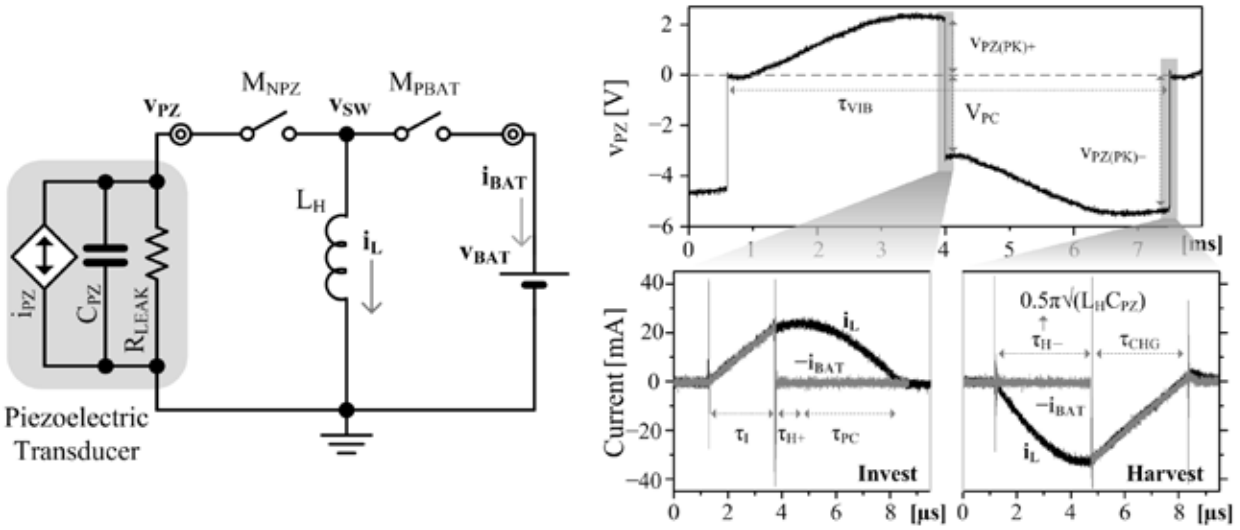

Fig. 2. Prototyped energy-investing switched-inductor power stage and corresponding waveforms measured.

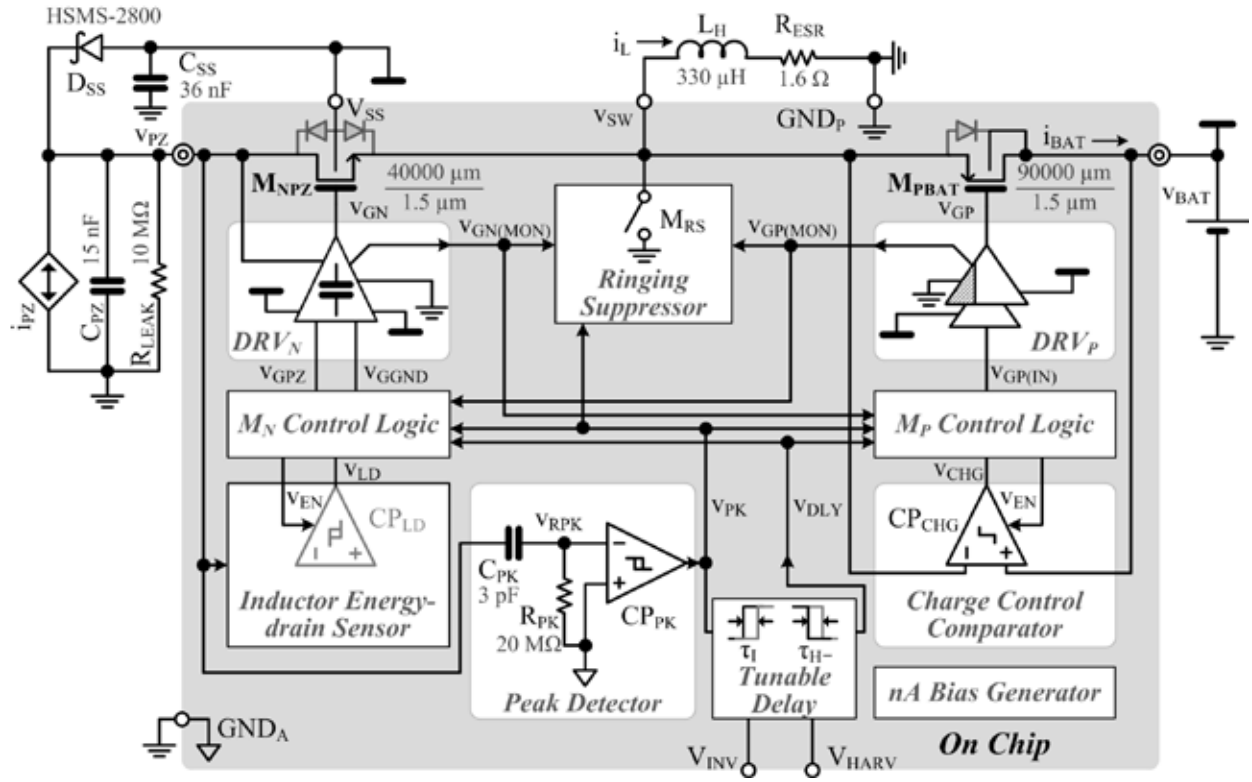

Fig. 3. Prototyped energy-investing piezoelectric harvester.

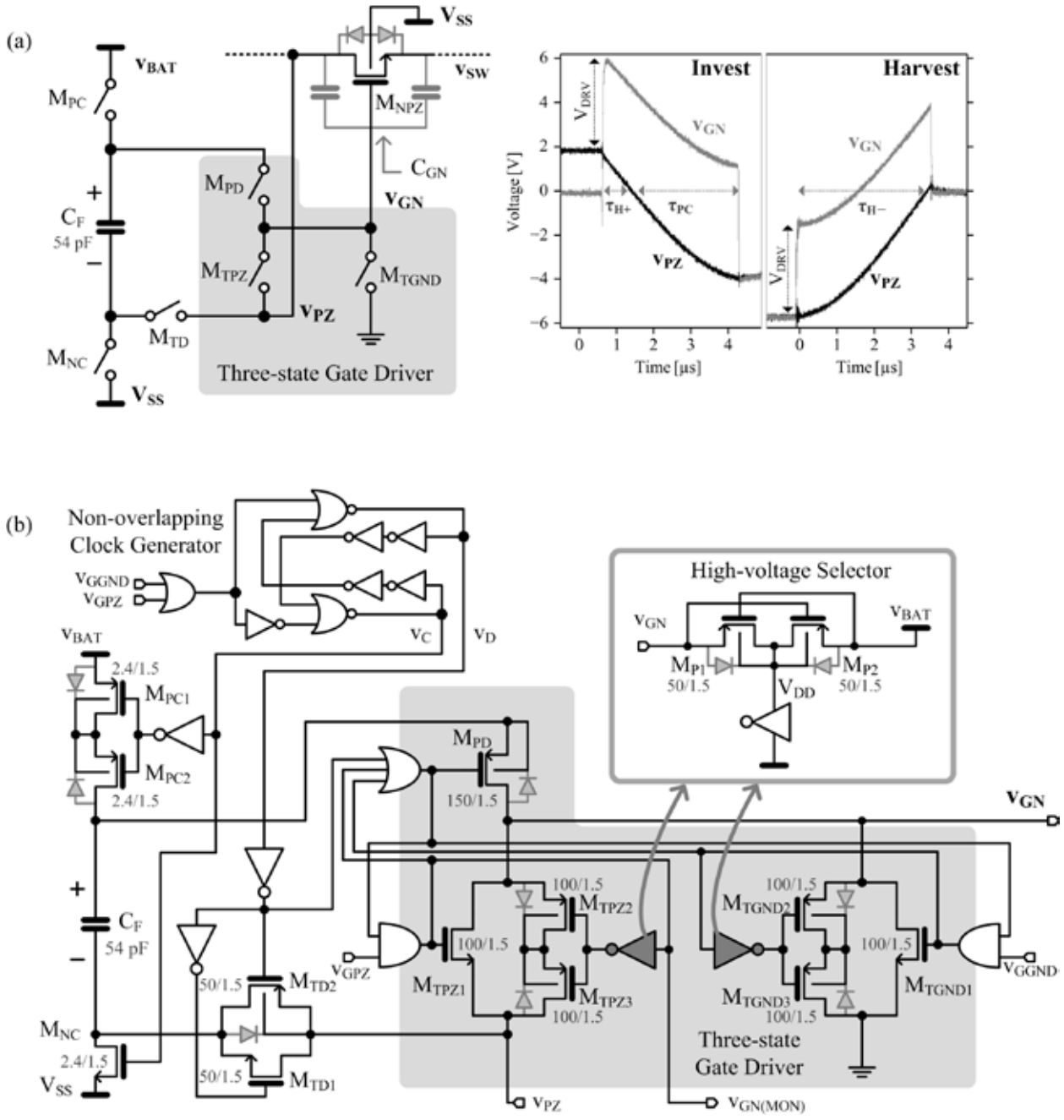

Fig. 4. M_{NPZ}'s driver DRV_N (a) network and corresponding waveforms measured and (b) schematic, where transistor dimensions are µm/µm and unspecified body terminals connect to their corresponding supplies.

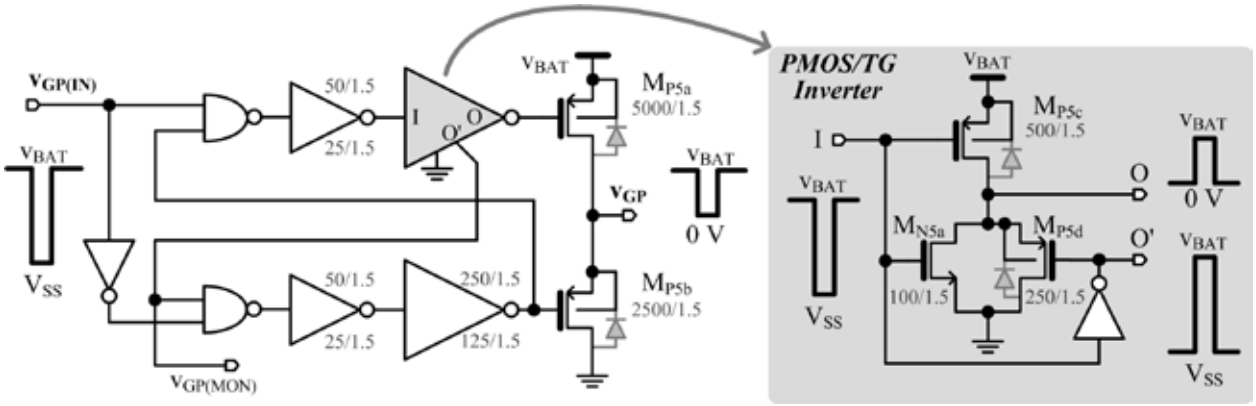

Fig. 5. M_{PBAT}'s driver DRV_P.

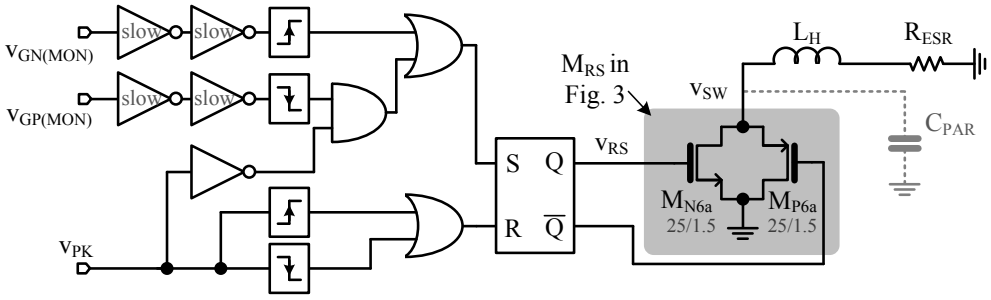

Fig. 6. Ringing suppressor.

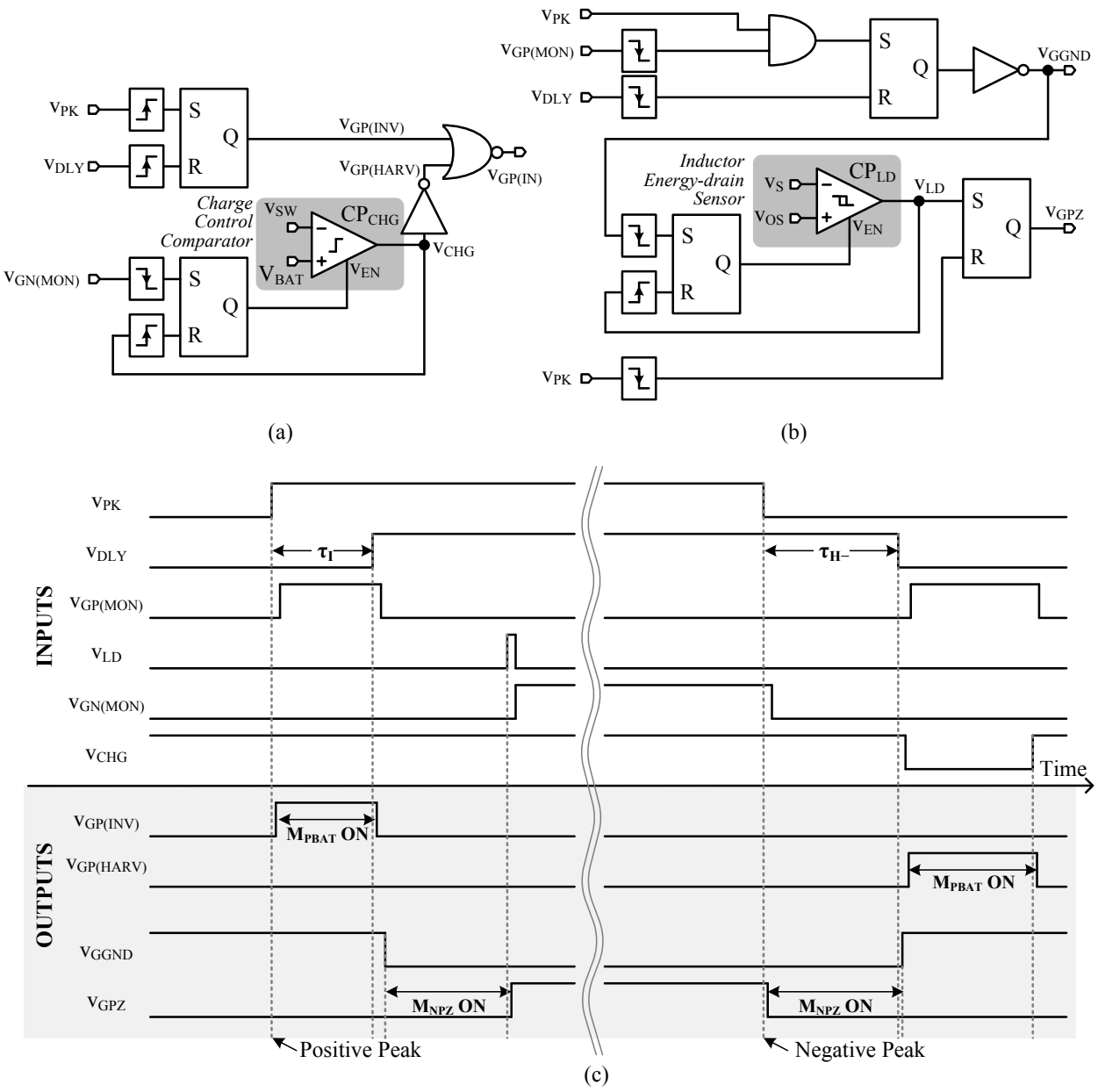

Fig. 7. Control logic for (a) M_{PBAT}'s DRV_P and (b) M_{NPZ}'s DRV_N and (c) their corresponding waveforms.

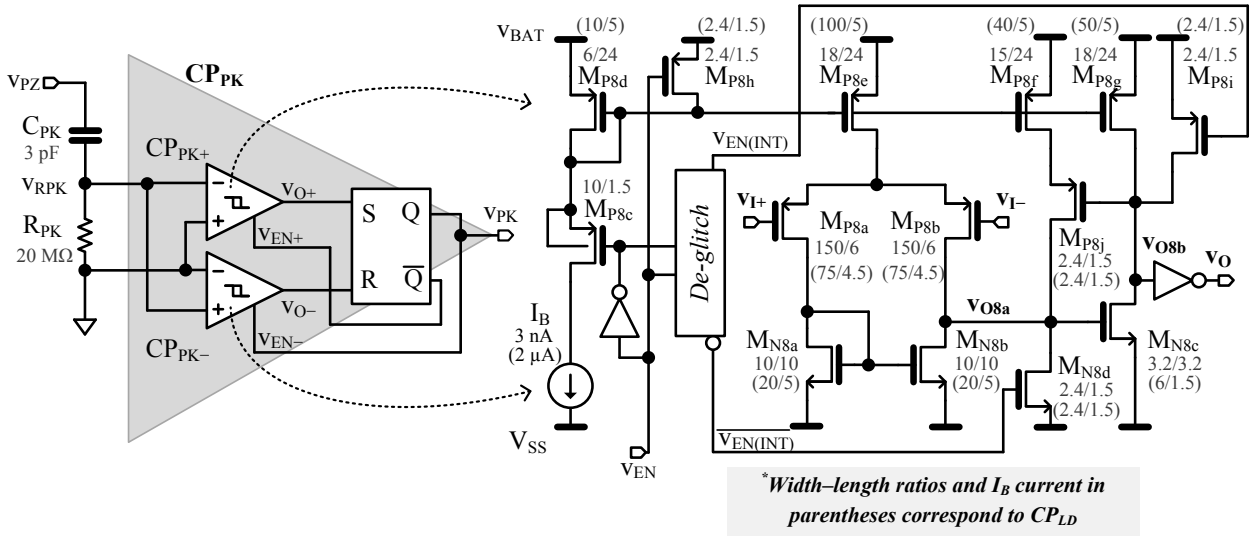

Fig. 8. Peak detector.

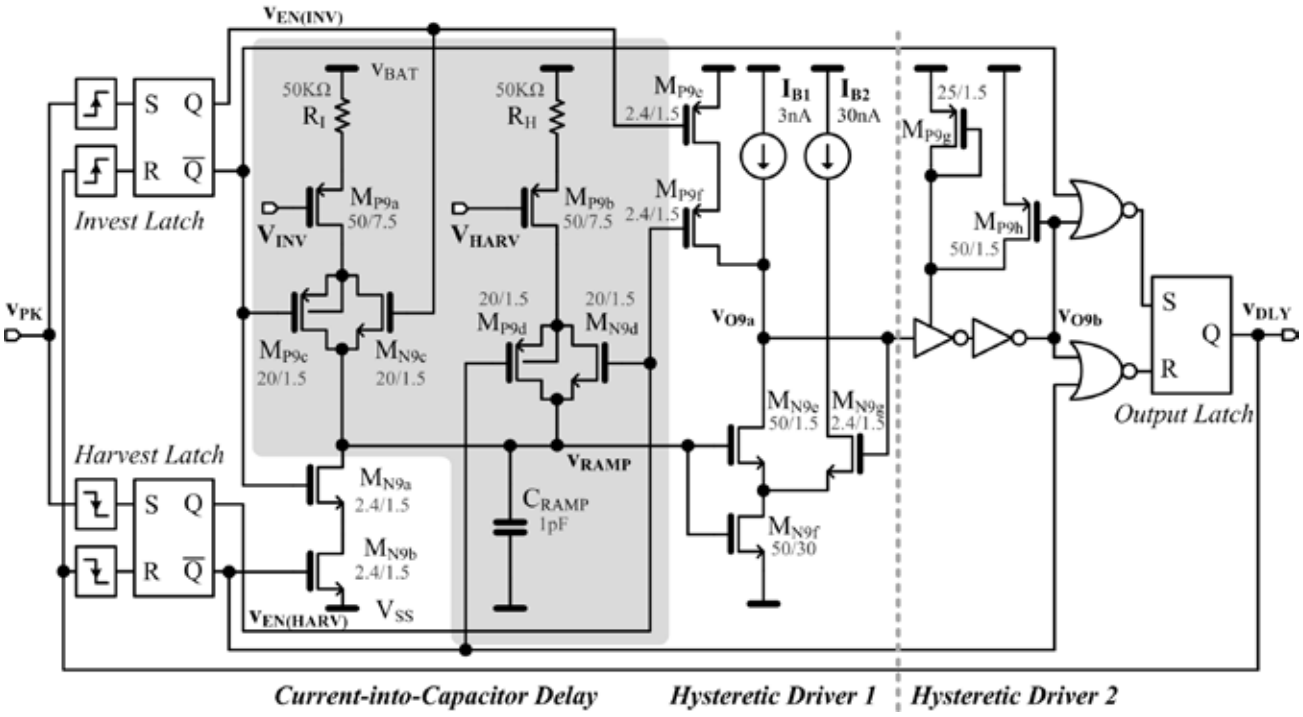

Fig. 9. Tunable delays.

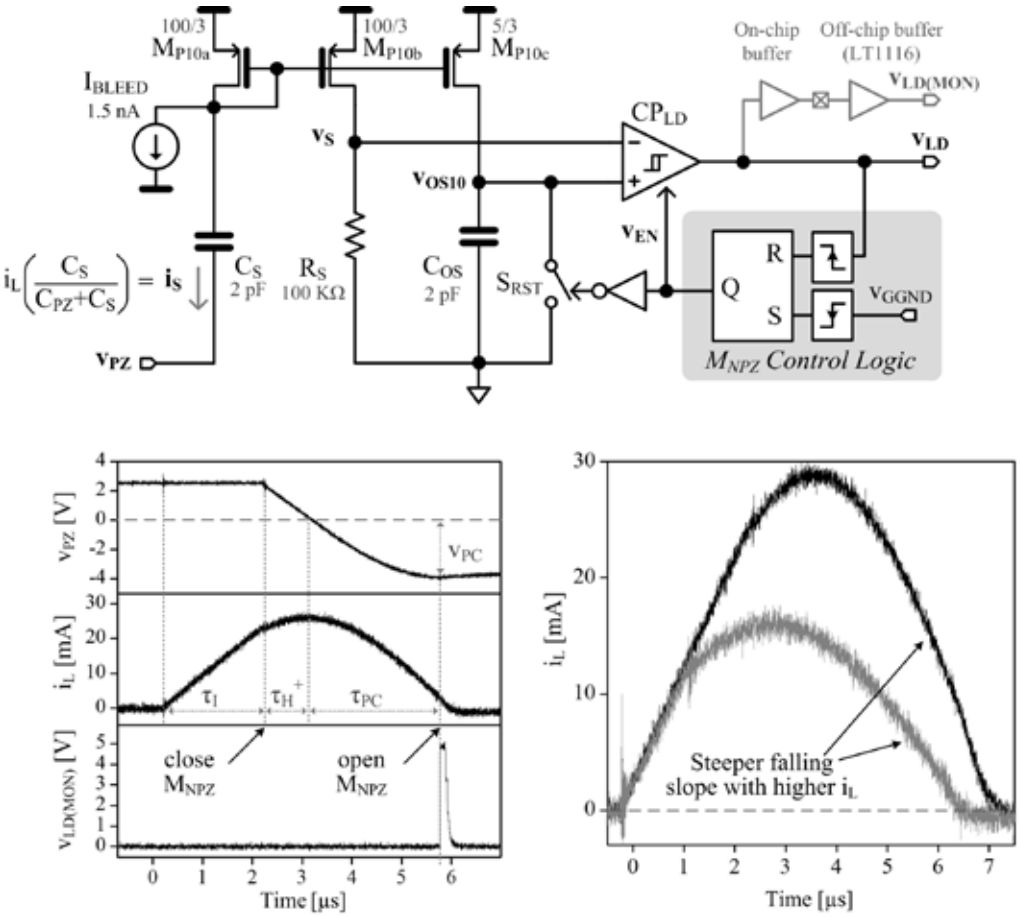

Fig. 10. Inductor energy-drain sensor and corresponding waveforms measured.

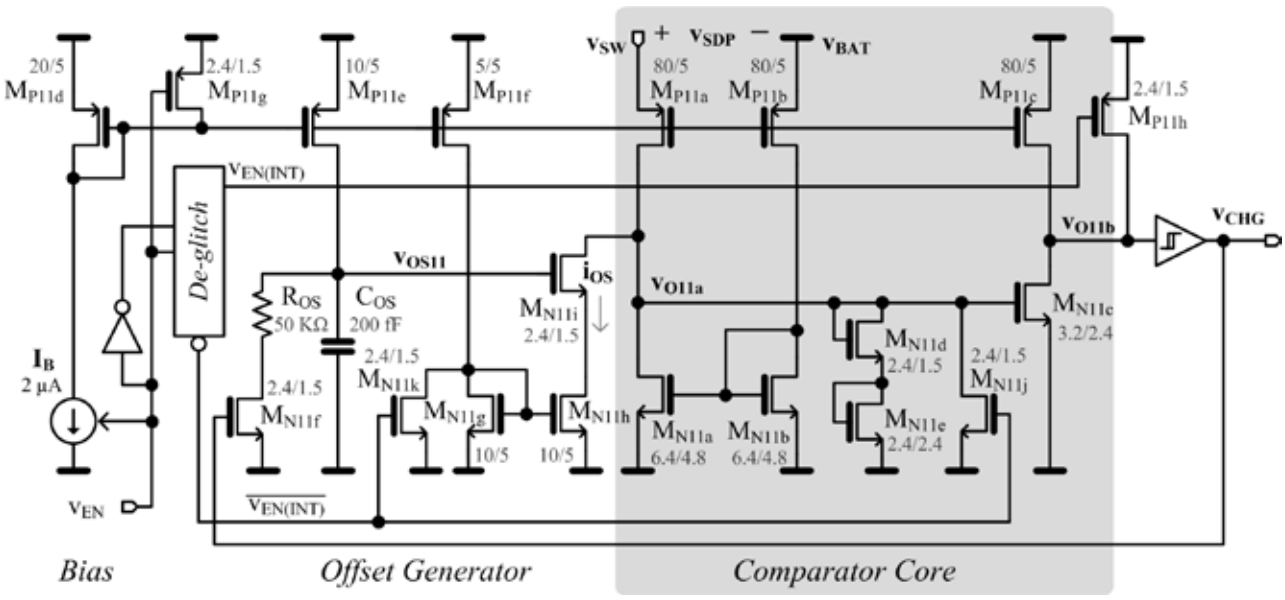

Fig. 11. Charge-control comparator CP_{CHG}.

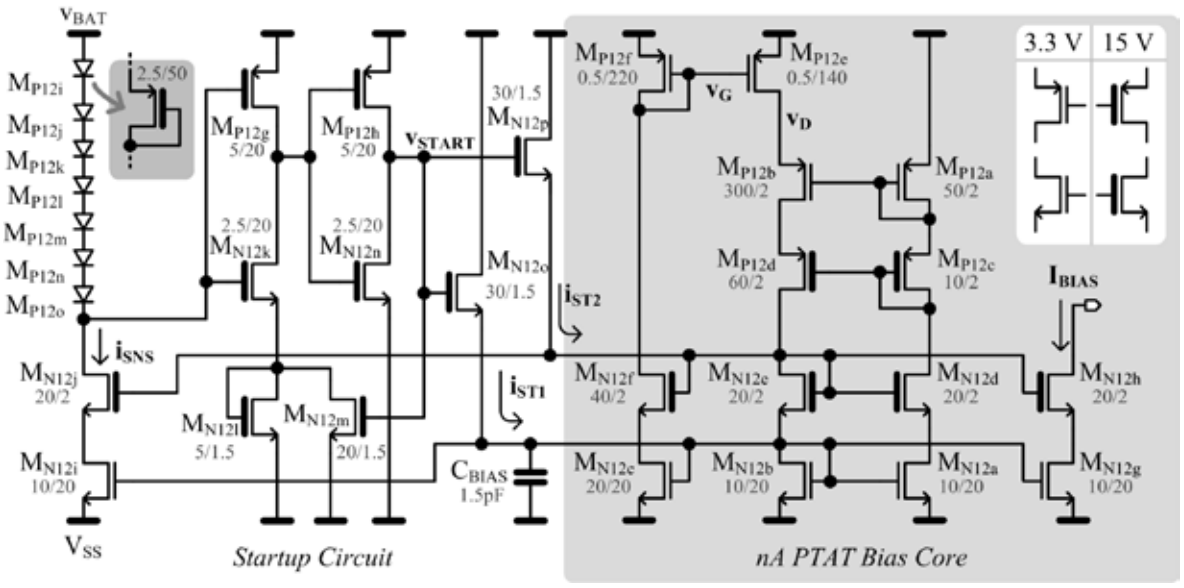

Fig. 12. Nano-amp PTAT bias-current generator.

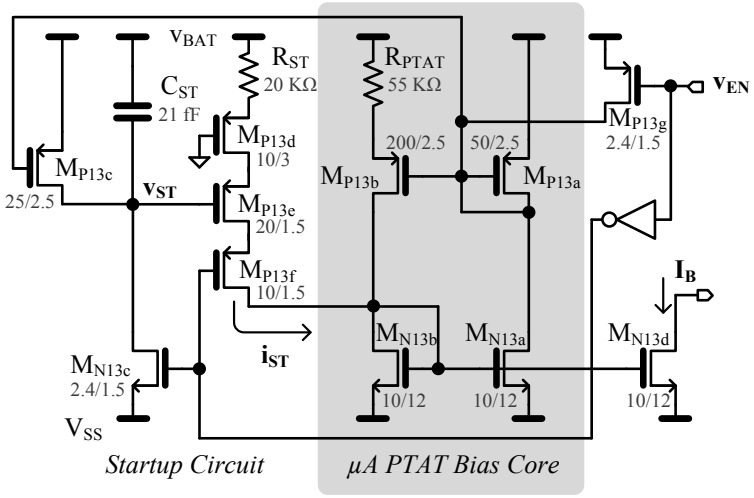

Fig. 13. Micro-amp PTAT bias-current generator in CP_{LD} and CP_{CHG}.

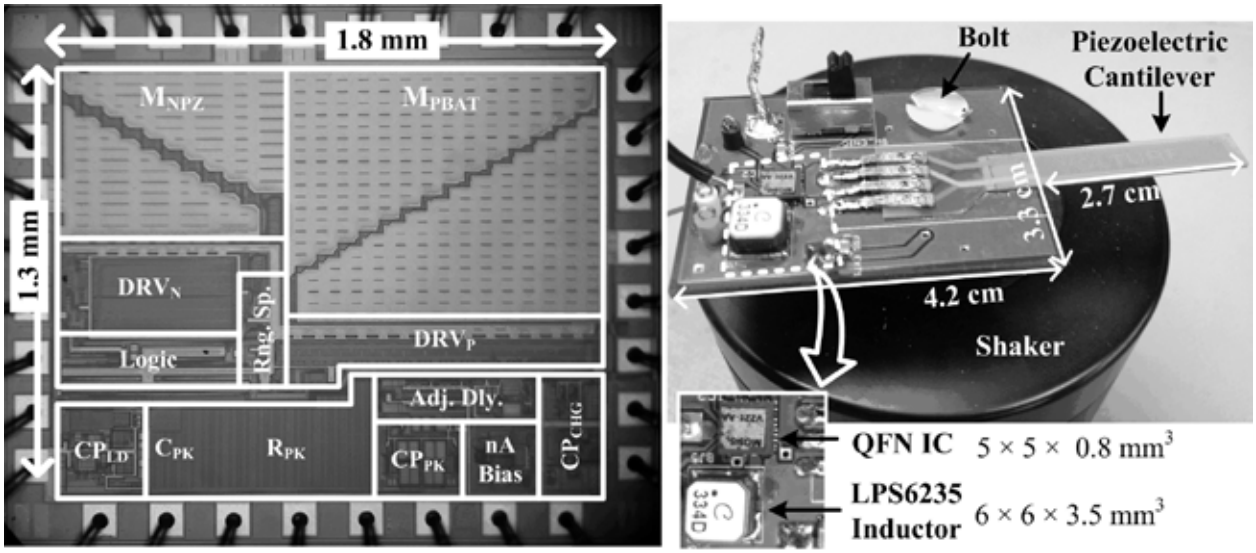

Fig. 14. 0.35-µm CMOS die fabricated, evaluation board prototyped, and corresponding experimental setup.

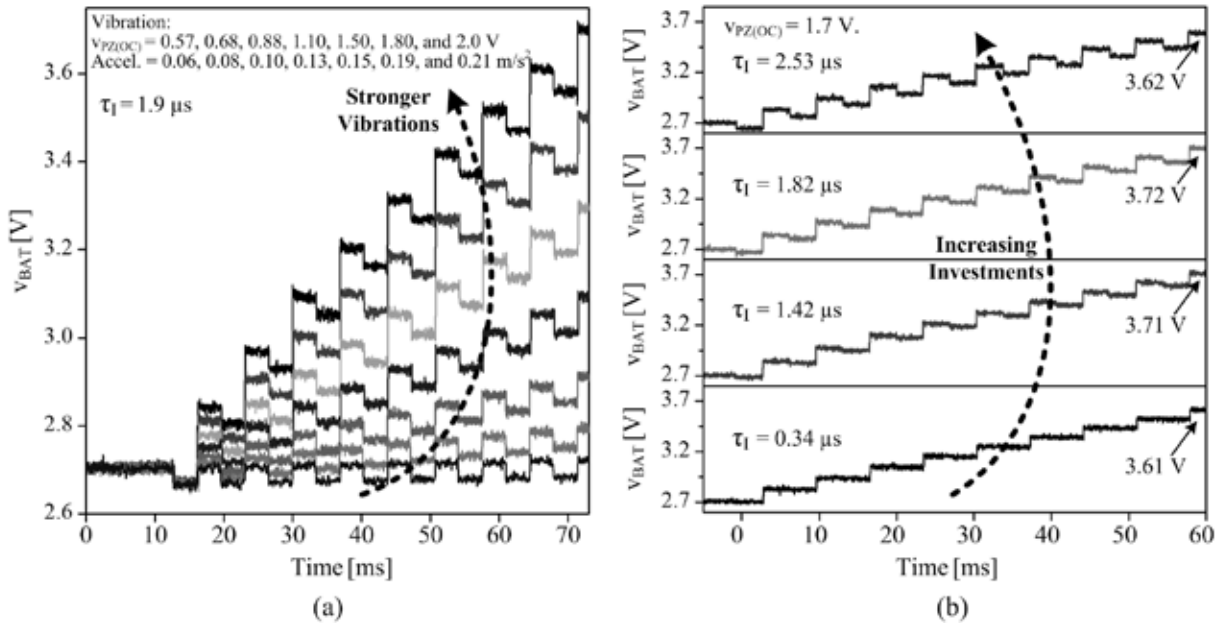

Fig. 15. Measured charge profile of a 475-nF capacitor across (a) vibration strength and (b) battery investment.

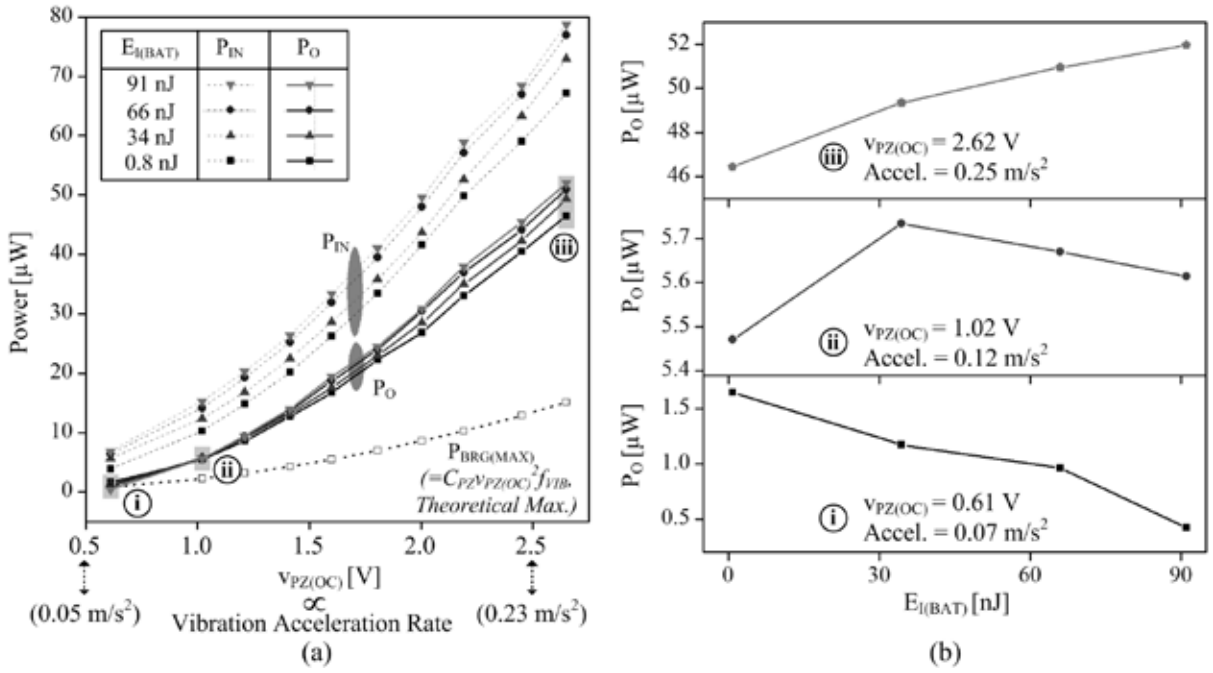

Fig. 16. Measured input and output power P_{IN} and P_O across (a) vibration strength and (b) battery investment.

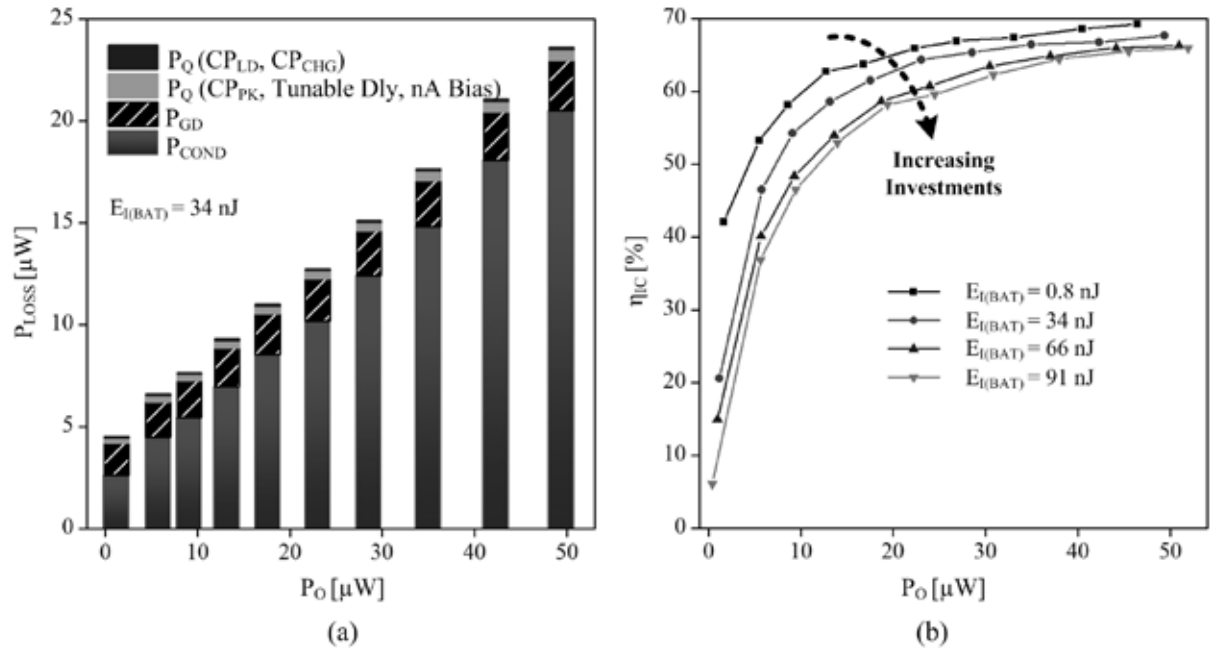

Fig. 17. (a) Measured power losses across output power when raising vibration strength and (b) corresponding power-conversion efficiencies across battery investment.

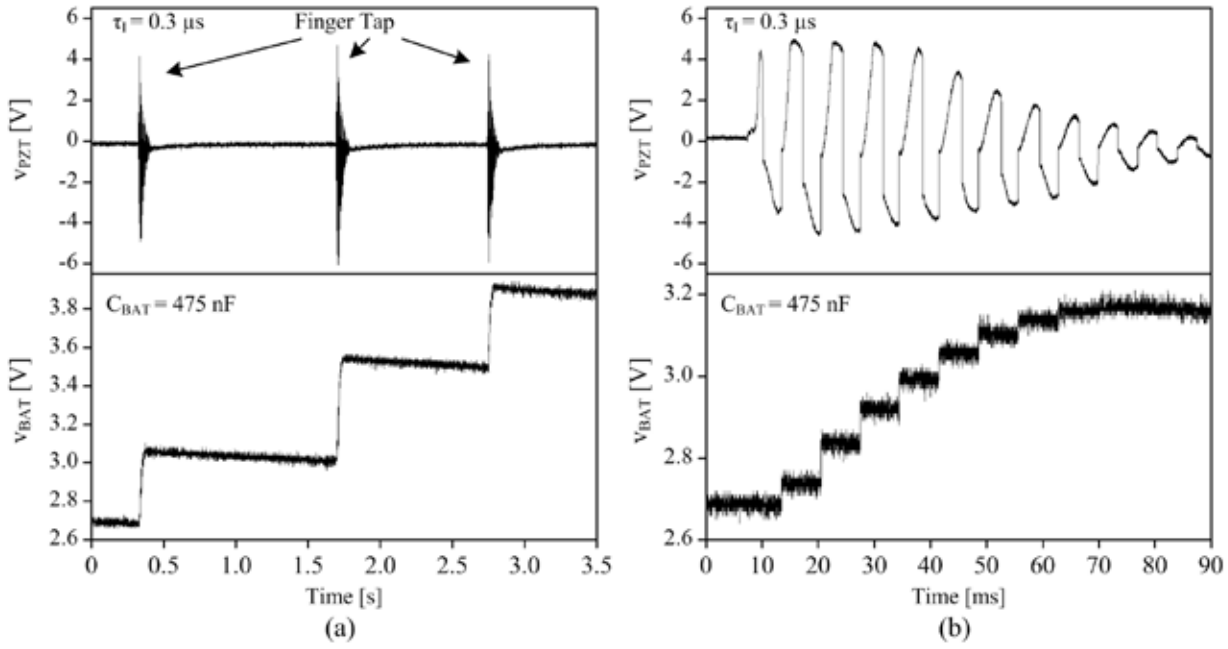

Fig. 18. Measured charge profile of a 475-nF capacitor when tapped with a finger (a) three times and (b) one time across a finer time scale.

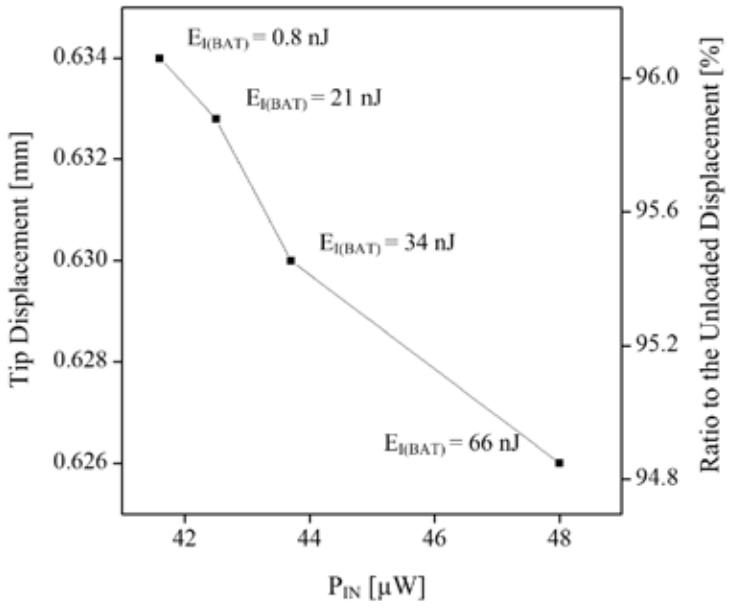

Fig. 19. Variation of cantilever's tip displacement across battery investment and resulting input power drawn.

TABLE I. COMPARISON OF MEASURED HARVESTING PERFORMANCE RESULTS

	Output Power P_O	C_{PZ}	$v_{PZ(OC)}$	f_{VIB}	Figure of Merit: $P_O/C_{PZ}V_{PZ(OC)}^2f_{VIB}$
Full-Wave Diode-Bridge Rectifier [13]	< 5 µW	12 nF	2.4 V	225 Hz	< 0.3
Ground-Switched Rectifier [13]	< 14 µW	12 nF	2.4 V	225 Hz	< 0.9
Recycling-Inductor Rectifier [13]	< 20 µW (L = 22 µH) < 47 µW (L = 820 µH)	12 nF	2.4 V	225 Hz	< 1.3 (L = 22 µH) < 3.0 (L = 820 µH)
Bridge-Free Harvester [15]	30 µW (L = 160 µH)	275 nF	1.2 V	100 Hz	0.8
Buffered Bridge-Free Harvester [16]	477 µW (L = 10 mH)	19.5 nF	12.6 V	176 Hz	0.88
Energy-Investing Harvester [This work]	46 µW (L = 330 µH, $E_{I(BAT)}$ = 0.8 nJ) 52 µW (L = 330 µH, $E_{I(BAT)}$ = 91 nJ)	15 nF	2.6 V	143 Hz	3.2 3.6