Reduce transistor mismatch errors without costly trimming and noisy chopping schemes

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The demand for precision is relentless, from 0.1% voltage references and 0.5µV offset operational amplifiers to 190MS/second 14-bit analog-to-digital (A/D converter) converters, yet fundamental error sources like transistor mismatch errors over process and temperature and RMS switching noise effects continue to plague performance. Shrinking supply voltages, budget-constrained test times, and rising bandwidth requirements only exacerbate the problem. State-of-the-art analog circuit solutions therefore succumb to trimming or switching networks to mitigate these process-induced errors. Unfortunately, neither of these techniques is especially attractive to the designer because trimming is costly and switching is noisy, which is why alternate circuit solutions are desired.

Trimming

Trimming is a post-fabrication circuit adjustment aimed at correcting the process-induced offsets of various components. The temperature-drift dependence of this adjustment should track that of the offset. Typically, one or more strategically placed resistors are tuned to offset the mismatch errors of two or more devices.

The resistance is varied by:
(1) fabricating a number of binarily weighted resistors and open- and/or short-circuiting them with on-chip fuses or
(2) reshaping and therefore resizing a resistor with a laser [1].

The accuracy of the former is limited by the reach and resolution of the trim resistors, that is to say, the initial mismatch accuracy performance that sets the full-scale trim-range resistance and the silicon area and test-time boundaries that limit the total number of bits that can be afforded. Laser trimming, on the other hand, is more accurate and area efficient and therefore often used in high performance data converter applications, but its inherent cost in test time and equipment is many times prohibitive.

The reason why trimming in general is so attractive is that many process-induced errors have an almost linear temperature dependence, like several of the mismatch and offset errors in a bandgap reference [2] and a bipolar differential pair, and consequently trimming at one temperature, for instance, room temperature is sufficient to cancel the temperature drift of the offset [1]. Its cost in manufacturing time, however, can account for 25% of the total cost of a power management IC [3], and this is only to correct first-order (linear) errors. The temperature dependence of higher order errors present in bandgap circuits and MOS and BiCMOS amplifiers are not compensated, only their absolute offsets at the trimming temperature (for example, room temperature) are reduced. Compounded to this are package stress-induced offset errors because most trimming procedures are performed at wafer level to circumvent the increased costs of post-package EEPROM trimming procedures. Package shift offset effects can be reduced by adding post-fabrication low-stress mechanically compliant layers to the IC before encapsulating it with plastic [1], but again, adding these compounds is costly.

Switching solutions

Another technique commonly used to reduce the effects of device mismatch is dynamic-element matching (DEM), a close relative of the better known chopping strategy [4]-[5]. In this technique, devices are matched by periodically interchanging their positions and therefore, in average, duplicating the same offset in all positions. An example of DEM as applied to a current mirror is shown in Fig. 1. If mirror devices MP1-MP2 were perfectly matched, the voltage across the load resistor (V_{REF}) would simply be $I_{REF}R_{REF}$. In practice, however, there is a mismatch between the two mirror devices that generates an offset current and consequently an error in the output voltage. DEM overcomes this offset by periodically interchanging the roles of MP1 and MP2 through a switching network. Since the output then has equal and opposite errors ($\pm\Delta VREF$) about the desired reference over time, the average is free of mismatch offset effects.

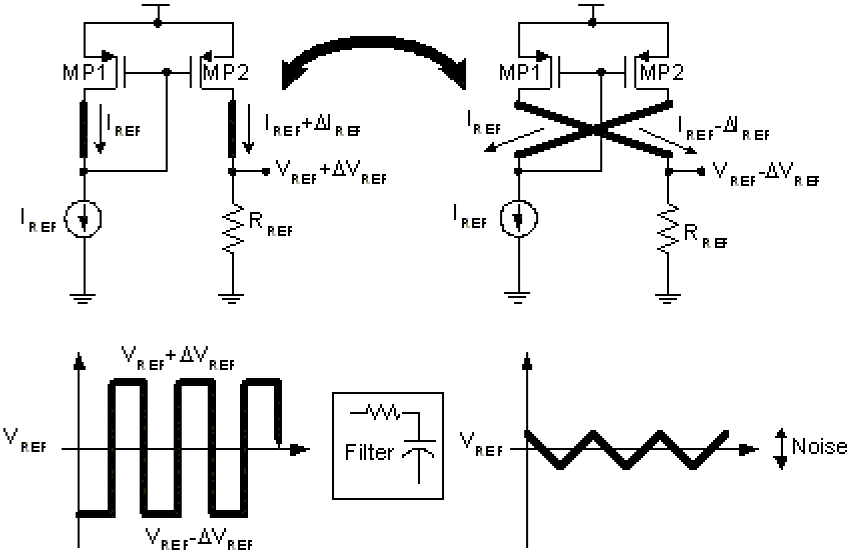

Figure 1. Use of dynamic-element matching to reduce mismatch offset errors

The real-time output of the mirror is a superposition of the ideal DC reference voltage and the opposite and equal values of the offset voltage (Figure 1). This peak-to-peak switching variation ($2\Delta V_{REF}$) is reduced with a low pass filter, as also shown in Figure 1, but not eliminated, which is the drawback of this scheme, especially when large filter capacitors are either unavailable (on-chip applications) or undesired (dynamic references). To minimize clock feed-through and charge-sharing effects, the switching frequency of DEM is normally low (for example, 1-10KHz) and a low roll-off frequency filter is therefore required, that is to say, a large capacitor, which is typically prohibitive in on-chip solutions and small foot-print printed-circuit boards (PCBs). Needless to say, without a large capacitor, the output has a noisy square wave superimposed onto the desired reference, raising the noise floor of the circuit and the entire system it supports.

The Survivor strategy

Barring the use of costly trimming and noisy switching schemes, the circuit must be sufficiently smart to use well-matched devices, which is the basis of the Survivor strategy. The scheme empowers the circuit with the ability to select the best two matching transistors out of an array of possible pairs during start-up and power-on-reset events. A bank of device pairs, each of which is assigned a unique digital code, is fabricated on-chip and, every time the system starts up or is reset, a digital engine connects two pairs from this bank to a comparator through a set of switches, as illustrated in Figure 2. The comparator, which adopts a DEM strategy to achieve low offset, determines which of the two connected pairs has higher mismatch. The digital engine processes this output and discards the pair with the higher offset, that is, the *loser*, and connects another pair from the bank in its place. This new pair is, in turn, compared against the previous *winner*. The winner of the last cycle, that is, the *survivor*, is therefore the pair with the best matching performance.

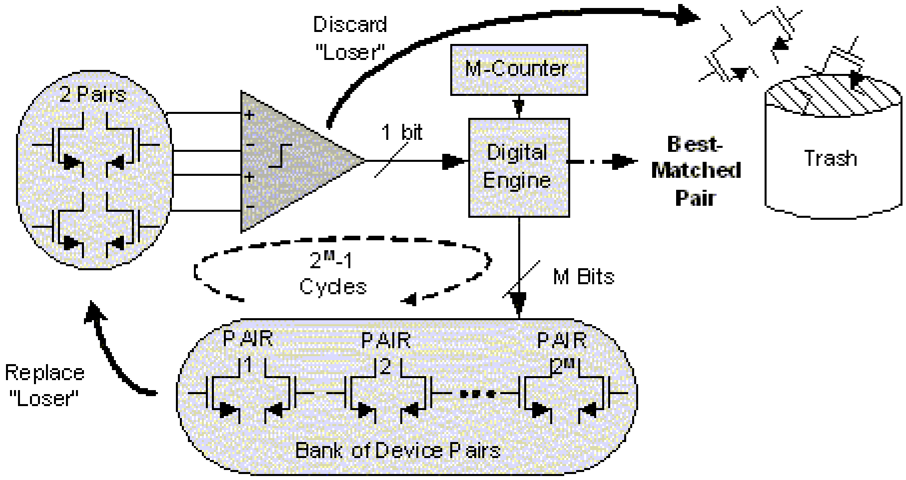

Figure 2. Survivor strategy

Since the system selects the best-matched pair of devices every time it starts up, trimming requirements (for example, linear and higher order temperature compensation) are significantly reduced, if not eliminated. Drift over time, temperature, and/or package-stress effects are all accounted for in each reset cycle, and the fact that DEM is employed in the comparator has no noise impact on the system because it is only operational during start-up and power-on-reset events. The most attractive feature of this scheme is its ability to generate the matching performance of large devices with smaller ones, achieving in the process the accuracy and speed (low parasitic capacitance) demanded by state-of-the-art applications. The main drawback is the silicon real-estate necessary to build the bank of devices, low offset comparator, and driving digital engine, but this cost is many times more acceptable and affordable than test-time, which is what trimming incurs. The statistical advantages of the Survivor strategy are currently under investigation.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Laboratory, at gtap@ece.gatech.edu. More information about our research can be found at www.rincon-mora.com/research.

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