



Energy harvesting: A battle against power losses

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Sep 23, 2006 (11:14 PM)

URL: <http://www.planetanalog.com/showArticle?articleID=193005042>

Is it possible, are indefinite operational life and wireless power grids possible? Maybe not for every application, but how about for micro-scale devices? The fact is in situ energy sources like MEMS vibrational and thermoelectric generators can potentially achieve these goals for small footprint system-in-package (SiP) solutions like bio-implantable devices and wireless sensor transceiver network nodes. The key objective is to scavenge sufficient energy from the environment to sustain the micro-power system indefinitely, or at least extend life to practical levels. The problem, however, is micro-scale harvesters can only generate low-to-moderate power, and the energy-storage and power-delivery processes of the system inherently consume a portion of that, which is why the various functions of a loading application must be power-moded, that is, multiplexed, duty-cycled, and turned off when not needed. Fortunately, low frequency ambient vibrations are relatively abundant, stable, and predictable, and tuned MEMS- and CMOS-compatible electrostatic harvesters, for instance, can generate moderate power levels [1], but only if they prevail over the power losses associated with energy storage and power delivery. The focus of this article is to therefore identify, quantify, and discuss the power-consuming mechanisms present in a harvester circuit.

Harvesting energy

Before attempting to discern the relevant power losses in a harvester, the process and circuit must be understood. For the purposes of this study, a voltage-constrained electrostatic scavenger that harnesses some of the kinetic energy present in vibrations is considered because it is both MEMS and CMOS compatible; in other words, it can all be co-packaged into a single chip. Its operation, as presented in [2], is divided into three distinct phases: pre-charge, harvesting, and recovery. First, when the capacitance of a variable-plate MEMS capacitor is at its peak, energy is invested into the system by pre-charging the capacitor to the battery voltage. The MEMS capacitor is then connected directly to a rechargeable battery (for example, Li-Ion battery), driving charge and energy into the battery when the capacitance drops (that is, the parallel plates separate) in response to ambient vibrations,

$$-I_{\text{Charge}} = \frac{\partial q}{\partial t} = \frac{\partial C}{\partial t} V + C \frac{\partial V}{\partial t} = \frac{\partial C}{\partial t} V \quad (1)$$

When minimum capacitance is reached, harvesting ends and the remaining energy in the capacitor is recovered. The end result, assuming no power is lost in the process, is a net energy-per-cycle gain in the battery of

$$\Delta E_{\text{Gain_Max}} = -\Delta E_{\text{Invested}} + \Delta E_{\text{Harvested}} + \Delta E_{\text{Recovered}} = \frac{1}{2} \Delta C V_{\text{Bat}}^2 \quad (2)$$

To transfer energy back and forth between the battery and the harvesting capacitor, an inductor is used, as shown in Figure 1, because of its low power-consuming properties. The pre-charge phase is therefore decomposed into a sequence of cycles that alternately energize the inductor (Step 1) and exhaust it in charging the MEMS capacitor (Step 2). In the recovery phase, the energy remaining in the capacitor is transferred back into the battery by reversing the Step 1-2 sequence [2]. Harvesting is achieved by short-circuiting the battery to the capacitor when its capacitance decreases, as illustrated with Step 3 in Figure 1.

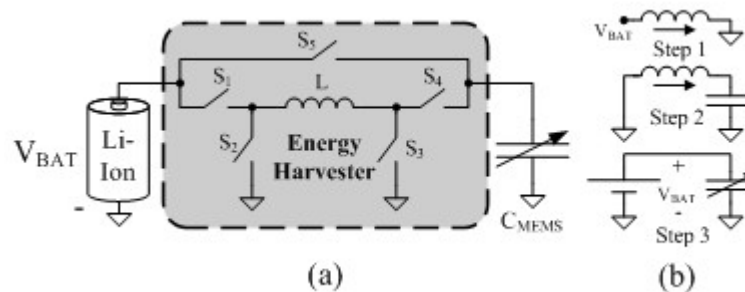


Figure 1. Energy harvester with inductor-based pre-charge and recovery circuit

A more complete and practical realization of the circuit is shown in Figure 2 where ideal switches are replaced with CMOS transistors and their respective body diodes, the battery is replaced with a capacitor-resistor model, and other parasitic capacitors and resistors are included. The 2.7 to 4.2 V Li-Ion battery is, on first order, a fixed-charge energy source with a parasitic load-dependent voltage drop and can therefore be modeled with a large pre-charged capacitor and an equivalent series resistor (ESR). MEMS device C_{MEMS} also has a parasitic ESR in addition to a parasitic capacitor across its terminals. The pre-charge and recovery circuitry features an inductor with its own ESR; CMOS switches MP_1 , MN_2 , and MN_3 ; and CMOS transmission gate MN_4 - MP_4 . The purpose of MN_4 in the transmission gate is to help MP_4 short-circuit the inductor to C_{MEMS} , especially when C_{MEMS} is discharged, which reduces MP_4 's gate-drive low enough to increase MP_4 's resistance beyond acceptable values. Two back-to-back transistors are used in place of S_5 in Figure 1 to prevent body-diode conduction during the pre-charge and recovery phases, which would have otherwise resulted with a single PMOS switching device.

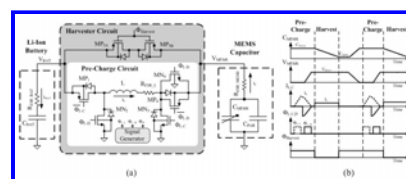


Figure 2. (a) Energy harvester circuit with non-ideal components and (b) control signals

Power losses

Power losses generally come in the form of conduction and switching losses. Parasitic diodes, resistive CMOS switches, and ESRs, for instance, incur I^2R and IV conduction losses. Parasitic capacitors present at the gates and drains of CMOS transistors, on the other hand, require power to charge and discharge, and this is how switching power losses result. Overlaps in the conduction bands of interconnected but oppositely phased switches from supply to ground also introduce additional short-

circuit I^2R conduction losses, but these are reduced by introducing dead bands. For the purposes of the foregoing discussion, power losses will be analyzed in each of the three phases of the circuit: pre-charge, harvesting, and recovery phases.

Pre-charge:

During the pre-charge phase, the cumulative resistance between C_{BAT} and C_{MEMS} , that is, the parasitic ESRs and CMOS channel resistances in the current-flowing path, induce a power loss term that is dependent on how often the current is switched through,

$$P_{Cond} = I_{L,RMS}^2 R \tau_{Cond} f_{Vib} \quad (3)$$

where P_{Cond} is averaged over time, $I_{L,RMS}$ is the root-mean square (RMS) value of the inductor current, R a resistance in the current-flowing path, τ_{Cond} the total conduction time, and f_{Vib} the vibration frequency. Current $I_{L,RMS}$ always flows through R_{ESR_L} , two MOS switches, and one of two other ESRs, and assuming all switch-on resistances (including the parallel combination of MP_4 - MN_4) equal and R_{ESR_BAT} and R are about the same, the total conduction losses are

$$P_{Cond} \approx N \left[I_{L,RMS}^2 (2R_{ds} + R_{ESR_L} + R_{ESR_BC}) \tau_L f_{Vib} \right] \quad (4)$$

where N is the number of inductor storage-delivery cycles within the pre-charge phase, $R_{ESR,BC}$ the ESR of the battery and C_{MEMS} , and τ_L the storage and delivery time within one cycle.

Overlapping the conduction bands of any two interconnecting but oppositely phased switches from supply to ground consumes considerable short-circuit power and a dead time must therefore be inserted in the driving signals. Devices MP_1 and MN_2 and MN_3 and MP_4 - MN_4 are two such sets of devices. When MP_1 and MN_3 turn off, to be specific, current must first flow through MN_1 's body diode, R_{ESR_L} , MP_4 's body diode, and R_{ESR_MEMS} for dead time τ_{Dead} before MN_1 and MN_4 - MP_4 are allowed to conduct, incurring additional conduction power losses,

$$P_{Dead} = N \left[I_{L,Max}^2 (R_{ESR_L} + R_{ESR_MEMS}) + 2I_{L,Max} V_{Diode} \right] \tau_{Dead} f_{Vib} \quad (5)$$

where dead time current $I_{L,Max}$ is the peak inductor current (assumed constant during τ_{Dead}) and V_{Diode} the voltage drop across each body diode.

As each switch turns ON or OFF, the parasitic gate and drain capacitors of the MOS devices must charge and discharge, both events of which require switching power. The average gate-power lost per switching event (turn-ON or -OFF), for instance, for a parasitic gate capacitor ($C_{g,Par}$) is

$$P_{GDrive} = \frac{1}{2} N C_{g,Par} V_{Drive}^2 f_{Vib} \quad (6)$$

where V_{Drive} is the peak voltage change across the capacitor (normally V_{Bat}) [3]. This power is

consumed by the stage that drives $C_{g,Par}$, not the transistor itself. Similarly, as each switching event takes place, parasitic capacitors present at the drain ($C_{d,Par}$) must also charge and discharge. In this latter case, however, the switching transistor dissipates the switching power, as it concurrently conducts drain current with a high drain-source voltage. The resulting average I-V overlap (or drain-charge) power loss per switching event is

$$P_{I-V} = \frac{1}{2} N C_{d,Par} V_{Peak}^2 f_{Vib} \quad (7)$$

where V_{Peak} is the drain-source voltage of the switch before turning ON (equal to V_{Bat} in the case of MP_1 and MN_2). The drain-source voltages of MN_3 , MN_4 , and MP_4 are close to zero (within a diode voltage) before they are turned ON because their respective body diodes discharge their drain-source capacitors during dead time. These latter transistors consequently operate in zero-voltage switching (ZVS) conditions, which incur considerably lower switching losses [4]. In the end, small geometry devices (low $C_{g,Par}$ and $C_{d,Par}$ values) are preferred for lower switching power losses, but only when the gate-drive and drain-charge losses in (6) and (7) overwhelm the gate-drive dependent switch-on resistance conduction losses in (4), all of which is ultimately a strong function of the battery voltage (peak voltage transitions).

1: Harvesting:

Just as in the pre-charge phase, harvesting also incurs conduction and switching losses, but no dead time losses, since only one switch is involved (MP_{5A} - MP_{5B}). To mitigate the adverse effects of clock feed-through and charge injection onto C_{MEMS} when the battery and C_{MEMS} are short-circuited and decrease the reverse-biased leakage currents associated with large source/drain areas from discharging C_{MEMS} , transistors MP_{5A} and MP_{5B} are small geometry devices. As a result, the switching losses in this phase are negligible relative to the conduction losses lost across the composite switch, which is especially acute for small transistors (large switch-on resistance):

$$P_{Harv_Cond} = I_{Harv}^2 (R_{ds5} + R_{ESR_MEMS} + R_{ESR_BAT}) \tau_{Harvest} f_{Vib} \quad (8)$$

where I_{Harv} is the harvesting current, R_{ds5} the cumulative switch-on resistance of MP_{5A} - MP_{5B} , and $\tau_{Max-Min}$ the harvesting time, which is the time it takes C_{MEMS} to reach its minimum capacitance point. The voltage drop across R_{ds5} further increases the voltage across C_{MEMS} , effectively increasing the harvesting current (and energy). The power lost in this resistance is actually supplied by C_{MEMS} , not the battery, in the form of additional mechanical work when separating its parallel plates, which can be offset by adjusting the elasticity of the MEMS capacitor.

There is one more power loss in the harvesting phase, and it results because of mismatches in battery and pre-charged C_{MEMS} voltages just after the pre-charge phase. A voltage difference ($V_{Mismatch}$) between these two devices forces an energy exchange through lossy switch-on resistance R_{ds5} , not the lossless inductor. This power loss is proportional to the vibration frequency and approximately

$$P_{Mismatch} = \frac{1}{2} C_{MEMS_Max} V_{Mismatch}^2 f_{Vib} \quad (9)$$

2: Recovery:

After harvesting ends, the energy left in the capacitor is only about 1-4% of the total energy harvested. The circuit complexity and associated conduction and power losses with recovering this energy tend to negate the absolute benefit of the exercise. For this reason, this left-over energy is considered a negligible loss. As a result, after opening all the switches, C_{MEMS} is allowed to return to its minimum plate-separation state under charge-constrained conditions, thereby decreasing the capacitor voltage to approximately 0 V.

In all, energy harvesting in micro-scale applications is challenging because the process of transferring power is itself lossy. This transfer-induced loss reduces the net energy gain of the system from the maximum theoretical limit depicted in (2) to:


$$\Delta E_{Net} = \frac{1}{2} \Delta C V_{Bat}^2 - \sum P_{Losses} T_{Vib} \quad (10)$$

where T_{Vib} is the period of the vibration and $\sum P_{Losses}$ the aggregate sum of all power losses. Even when a supposedly lossless inductor is used to transfer energy, the fundamental conduction (R_{ds} , ESRs, and diodes), switching ($C_{g,Par}$ and $C_{d,Par}$), and systematic (quiescent power and battery- C_{MEMS} mismatch voltages) losses of the circuit limit the net yield of the system. Optimizing these losses is often contradicting, as is the case with R_{ds} and $C_{d,Par}$ - $C_{g,Par}$, where smaller devices yield lower switching losses and larger devices smaller conduction losses. The battery voltage also has a convoluted role in that it not only sets the gate-drive that determines the various switch-on resistances (that is, conduction losses) but it also establishes the extent to which $C_{g,Par}$ and $C_{d,Par}$ are charged and discharged (that is, switching losses). The objective is to therefore balance these losses and design and build a practical circuit prototype that is able to produce a net energy gain, which is currently under development at the Georgia Tech Analog and Power IC Laboratory.


For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Laboratory, at gtap@ece.gatech.edu. More information about our research can be found at <http://www.rincon-mora.com/research>.

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