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## Inductors and multipliers in practice--Get efficient transfer of energy

**Here's what you need to know about inductors and multipliers to get efficient transfer of energy.**

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Operational life in portable electronics like cellular phones and media players hinges on how efficiently energy is transferred from the battery to the load and no other electronic component can equal the performance of a power inductor in this regard. While linear regulators and charge pumps ultimately expose a conducting [switch](#) to non-zero voltages, inductor-based topologies only do so at close-to-zero voltages, minimizing conduction power losses and therefore producing the most efficient results. Inductors, however, require precious real estate on chip, if integrated, and on the printed-circuit board (PCB), and while lower inductances may be feasible, the larger supply ripple voltages they produce are normally, not acceptable. Consequently, multiplier [circuit](#) techniques that aim at reducing their size requirements are appealing, but only if power efficiencies remain relatively high.

### Applying the inductor multiplier to a switching DC-DC converter

To comprehend the power implications of an inductor multiplier, it is useful to discuss it within the context of a switching step-down converter. In such a circuit, as shown in Figure 1, two out-of-phase switches alternately conduct current to generate a square wave voltage and in the process energize an inductor and release its energy to the load. Together, the inductor and [capacitor](#) filter and average this square wave into an [analog](#) DC voltage, whose value, when compared against a reference voltage in a negative feedback loop, controls and sets the duty cycle of the digital train driving the switches. The current flowing through the inductor is consequently triangular in nature because the voltage impressed across the device is for the most part digital, pulse-width modulated signal  $V_{PWM}$  on one terminal, which is zero or DC [input](#) voltage  $V_{In}$ , and output  $V_{Out}$  on the other, whose ripple voltage variations are negligible when compared to its [DC](#) level and  $V_{PWM}$ 's voltage swing. The load ( $I_{Out}$ ) ultimately sinks the average (DC) portion of inductor current  $I_L$ , in the process forcing the AC ripple current into the [output](#) capacitor, which is why a small [AC](#) ripple [voltage](#) exists at  $V_{Out}$ .

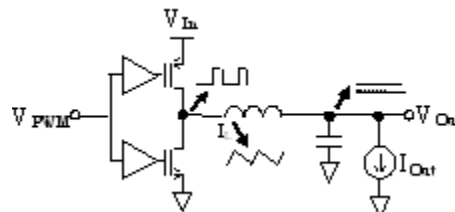


Figure 1. Switching step-down buck DC-DC converter

The effect of applying an inductor multiplier to the buck converter is a smaller capacitor AC ripple current. This is effectively achieved by sinking a portion of the inductor AC ripple current, as shown in Figure 2, and only sourcing a small difference to the capacitor (the inductor DC current flows to the load unchanged). Multiplying circuit  $L_{Multiplier}$  senses and/or predicts the AC ripple current and generates an appropriately sized out-of-phase signal, mostly canceling the ripple current flowing through a small on-chip or in-package inductor, allowing only a small AC ripple voltage to appear at the converter output. The power associated with this out-of-phase current determines the efficiency impact of the multiplier on the converter, which ultimately sets the viability of the same.

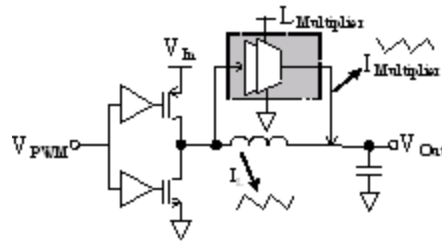


Figure 2. Applying the inductor multiplier to a buck converter:  $L_{Multiplier}$  effectively subtracts AC ripple current from a small inductor

### Impact on power efficiency

The conventional switching buck converter is already plagued with a series of power-consuming factors that fundamentally limit its efficiency performance. The voltages across the power devices, for one, although small, are finite and quantifiable, and those devices carry both the DC and AC portions of the inductor current. Switching those power devices on and off also requires energy, especially because they are inherently large transistors with considerably large input capacitances. While the inductor and capacitor are theoretically lossless, the parasitic equivalent series resistances (ESRs) they introduce are not. The inductor's ESR and capacitor's ESR consume power as they carry DC and AC ripple current, in the inductor case, and only AC ripple current, in the capacitor case. Because of these dependencies, the efficiency of a conventional converter normally peaks at an optimum load, as shown in Figure 3, and decreases with increasing load currents, as DC current losses increase ( $I_{L-DC}^2 R_{Eq}$  or  $I_{Out}^2 R_{Eq}$ ) and with decreasing load currents, as output power decreases ( $I_{Out} V_{Out}$ ) and AC ripple current losses and switching losses remain constant ( $I_{L-AC}^2 R_{Eq}$  or  $\Delta I_{L-RMS}^2 R_{Eq}$ ) [1].

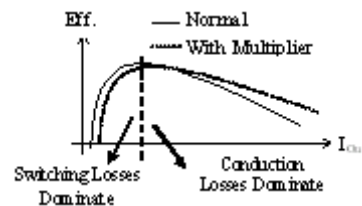


Figure 3. Efficiency performance of a buck converter with and without the inductor multiplier

Since the multiplier only carries AC ripple current, the power it dissipates is not proportional to load current  $I_{Out}$  but only to the peak-to-peak value of the inductor ripple current ( $\Delta I_L$ ), which is set independently of  $I_{Out}$  (that is, the average current sourced by the multiplier is zero). And more specifically, as shown in Figure 4 [2] and Equation 1, the power consumed is linearly dependent on  $V_{in}$  and  $\Delta I_L$  because the device sourcing the positive ripple current is exposed to  $V_{in} - V_{Out}$  and the transistor sinking the negative ripple current to  $V_{Out}$ , while both carrying an average ripple current of  $\Delta I_L/8$ :

$$P_{Multiplier} = \frac{(V_{in} - V_{out}) \Delta I_L}{8} + \frac{V_{out} \Delta I_L}{8} = \frac{V_{in} \Delta I_L}{8} \quad (1)$$

The end result is, like switching and other AC ripple-related losses, the additional power consumed by the multiplier has limited impact on efficiency during heavier loading conditions when load-related losses ( $I_{Out}^2 R_{Eq}$ ) overwhelm all other losses. The multiplier carries an additional benefit, however, in that it uses a smaller on-chip or in-package inductor to achieve the same accuracy performance of a larger device. The smaller inductor has fewer wire turns and therefore exhibits lower ESR and ESR-related losses ( $I_{Out}^2 R_{ESR}$  and  $I_{L-AC}^2 R_{ESR}$ ), the result of which may be higher overall converter efficiency during heavier loading conditions, as illustrated in Figure 3.

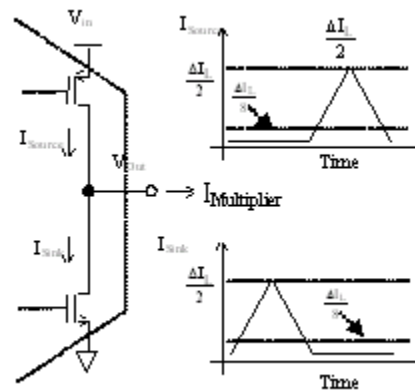


Figure 4. Inductor multiplier's output stage and accompanying current conduction waveforms

### In practice

Inductor multipliers incur additional AC current ripple-related losses whose degrading effects on power efficiency are most profound during light loads, which are prevalent conditions in portable applications. Discrete printed circuit board (PCB) realizations, in fact, which [exploit](#) the benefits of relatively mature inductor technologies (that is, high inductances with low ESR values), may not reap any advantages from the multipliers; unless the multiplying feature is used for speed-up purposes, that is, for better regulating performance and therefore improved accuracy. For instance, the multiplier may be used to achieve low output ripple voltages during steady-state conditions and disabled only during load-dump events so as to respond at the speed characteristic of a lower inductance value, that is, faster. The multiplying feature can also be used to alter the duty cycle of a given input-output voltage combination by multiplying the inductance only during specific times of the switching period. This extra degree of freedom, which may be most useful in avoiding extreme duty-cycle conditions, may not be sufficient to warrant the additional losses incurred by the circuit in discrete PCB solutions, however.

The real benefits of the inductor multiplier surface within the context of total integration, when the performance of on-chip and in-package inductors is relatively poor. The parasitic ESR associated with these micro-scale devices is typically large because thinner wires are used, which translates to lower efficiency across the load-current range. An inductor multiplier may therefore ease the size requirements of the inductor to such a degree that the savings in ESR-related losses can compensate for the additional multiplier losses. The option is especially appealing when considering on-chip inductances of 100 nH or higher are next to impossible to achieve with reasonable quality factors; in other words, fully integrated DC-DC converters with low output ripple voltages are difficult to realize. Total integration is therefore what brings the most value to inductor multipliers, when only low inductance devices are available and/or ESR-related power losses are extreme — a [CMOS](#) prototype of the inductor multiplier is currently under development to test and study these effects.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Laboratory, at [gtap@ece.gatech.edu](mailto:gtap@ece.gatech.edu). More information about our research can be found at <http://www.rincon-mora.com/research>.

### References:

- [1] G.A. Rincón-Mora, Power Management ICs — A Top-Down Design Approach. Lulu, 2005 (ISBN 1-4116-6359-4).
- [2] L.A. Milner and G.A. Rincón-Mora, "A Novel Predictive Inductor Multiplier for [Integrated Circuit](#) DC-DC Converters in Portable Applications," in Proceedings of the 2005 International Symposium on Low Power Electronics and Design, pp. 84-89.

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