



US006628109B2

(12) **United States Patent**  
**Rincon-Mora**

(10) **Patent No.:** **US 6,628,109 B2**  
(45) **Date of Patent:** **\*Sep. 30, 2003**

(54) **INTEGRATED LOW RIPPLE, HIGH FREQUENCY POWER EFFICIENT HYSTERETIC CONTROLLER FOR DC-DC CONVERTERS**

5,063,490 A	*	11/1991	Maehara et al.	363/37
5,363,020 A	*	11/1994	Chen et al.	315/209 R
5,770,940 A	*	6/1998	Goder	323/282
5,923,542 A	*	7/1999	Sasaki et al.	363/16
5,982,106 A	*	11/1999	Bobel	315/209 R
6,369,555 B2	*	4/2002	Rincon-Mora	323/282

(75) **Inventor:** **Gabriel A. Rincon-Mora, Allen, TX (US)**

\* cited by examiner

(73) **Assignee:** **Texas Instruments Incorporated, Dallas, TX (US)**

(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

*Primary Examiner*—Adolf D. Berhane

(74) *Attorney, Agent, or Firm*—J. Dennis Moore; W. James Brady, III; Frederick J. Telecky, Jr.

(21) **Appl. No.:** **09/883,780**

(22) **Filed:** **Jun. 18, 2001**

(65) **Prior Publication Data**

US 2001/0054883 A1 Dec. 27, 2001

**Related U.S. Application Data**

(60) Provisional application No. 60/214,102, filed on Jun. 26, 2000.

(51) **Int. Cl.<sup>7</sup>** ..... **G05F 1/40**

(52) **U.S. Cl.** ..... **323/282**

(58) **Field of Search** ..... 323/280, 282, 323/284, 351

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,929,882 A \* 5/1990 Szepesi ..... 323/222

(57) **ABSTRACT**

The present invention relates to a method of improving power efficiency in a converter circuit at low load currents. The method comprises the steps of monitoring a load current of the converter circuit and adjusting a natural frequency of the converter circuit based on the load current. Such an adjustment of the natural frequency results in a reduction in switching losses at low load currents, thereby improving the power efficiency associated therewith. The present invention also relates to a circuit for improving a power efficiency in a dc—dc converter. The circuit comprises a converter circuit and a comparator circuit coupled to an input of the converter circuit. The dc—dc converter also comprises a feedback circuit coupled between an input and an output of the comparator circuit; the feedback circuit is operable to alter a trip frequency of the comparator circuit as a function of a load current at an output of the converter circuit, thereby decreasing switching losses at low load currents and improving the power efficiency associated therewith.

**30 Claims, 6 Drawing Sheets**



























