Errata for *Analog IC Design with Low-Dropout Regulators*

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Chapter 2

Page 69: "…the MOSFET enjoys the benefit of true symmetric performance…"

Chapter 3

Equation 3.4: $G_{M.LF}\big|_{v_{out}=0} = \frac{i_{out}}{v_{in}} \approx \frac{v_{gs}g_m}{v_{gs}+v_R} = \frac{v_{gs}g_m}{v_{gs}+R\left(v_{gs}g_m\right)} = \frac{g_m}{1+Rg_m} \le g_m$

Equation 3.5: $G_{M.LF}\big|_{v_{out}=0} = \frac{i_{out}}{v_{in}} \approx \frac{v_{gs}g_m - v_R g_{mb}}{v_{gs}+v_R} = \frac{g_m}{1+\left(g_m+g_{mb}\right)R} \le g_m$

Equation 3.6: $G_{M.LF}\big|_{v_{out}=0} = \frac{i_{out}}{v_{in}} \approx \frac{v_\pi g_m}{v_\pi + v_R} = \frac{v_\pi g_m}{v_\pi + R\left[v_\pi g_m\left(1+\frac{1}{\beta}\right)\right]} \approx \frac{g_m}{1+Rg_m} \le g_m$

Equation on page 89: $\left(R \parallel \frac{1}{sC}\right) = \frac{R}{1+sRC} = \frac{R}{1+\frac{s}{2\pi p}}$

Equation 3.20:

$$G_M \approx \frac{g_m}{1+g_m\left(R \,\|\, \frac{1}{sC_{PAR}}\right)} = \frac{g_m}{1+g_m\left(\frac{R}{1+sRC_{PAR}}\right)} = \frac{g_m\left(1+sRC_{PAR}\right)}{\left(1+g_mR\right)\left[1+\frac{sRC_{PAR}}{\left(1+g_mR\right)}\right]}$$

$$= \frac{G_{M.LF}\left(1+\frac{s}{2\pi z_G}\right)}{\left[1+\frac{s}{2\pi z_G}\left(\frac{G_{M.LF}}{g_m}\right)\right]} \equiv \frac{G_{M.LF}\left(1+\frac{s}{2\pi z_G}\right)}{\left(1+\frac{s}{2\pi p_G}\right)}$$

Figure 3.14:

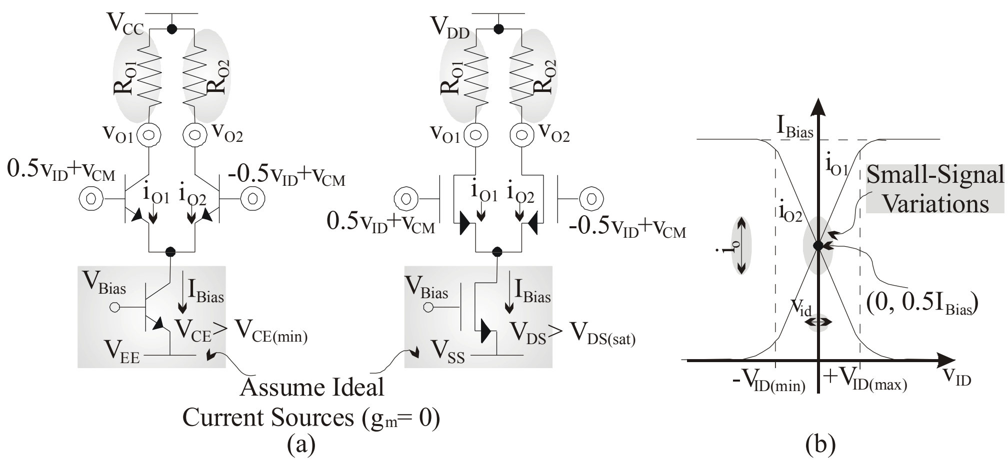
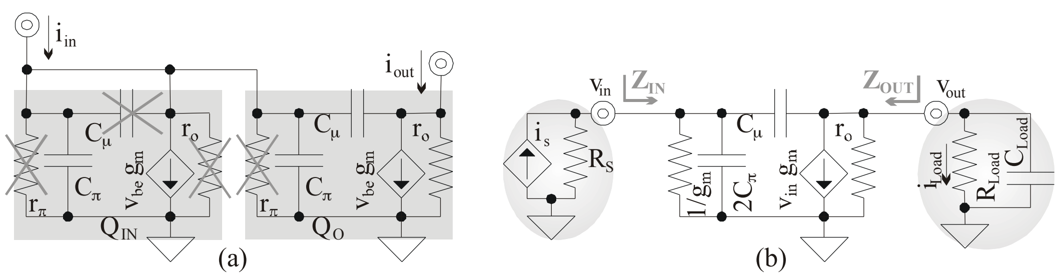


Figure 3.22:



Equation 3.78:

Since Q_{IN}–Q_O mirrors $i_{gm.IN}$,

$$i_{b.CO} = \frac{i_{gm.IN}}{1+\beta} \quad \text{and} \quad R_{IN} = \left(\frac{1}{g_{m.CIN}} + \frac{1}{g_{m.M}}\right) \parallel R_{IN.CO} \approx \frac{2}{g_m} \parallel \left[\frac{2}{g_m}(1+\beta)\right] \approx \frac{2}{g_m}$$

Equation 3.81:

$$A_{I.LF} \equiv \frac{i_{Load}}{i_s} = \left(\frac{v_{in}}{i_s}\right)\left(\frac{v_{b.M}}{v_{in}}\right)\left(\frac{i_{gm.M}}{v_{b.M}}\right)\left(\frac{v_{e.CO}}{i_{gm.M}}\right)\left(\frac{i_{gm.CO}}{v_{e.CO}}\right)\left(\frac{v_{out}}{i_{gm.CO}}\right)\left(\frac{i_{Load}}{v_{out}}\right)$$

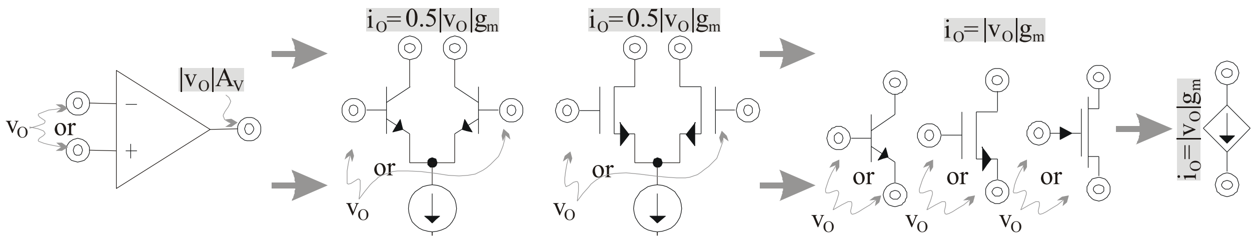
$$= \left(R_S \parallel R_{IN}\right)\left[\frac{\left(\frac{1}{g_{m.M}}\right)}{R_{IN}}\right]\left(-g_{m.M}\right)\left[\frac{r_{o.CO} + R_{Load}}{1 + g_{m.CO} r_{o.CO}} \parallel \left(r_{\pi.CO} + \frac{1}{g_{m.M}} + \frac{1}{g_{m.CIN}}\right)\right]\left(g_{m.CO}\right)\left(R_{OUT} \parallel R_{Load}\right)\left(\frac{1}{R_{Load}}\right)$$

$$\approx \left(R_S \parallel R_{IN}\right)\left(\frac{1}{2}\right)\left(-g_{m.M}\right)\left(\frac{1}{g_{m.CO}}\right)\left(g_{m.CO}\right)\left(\frac{R_{OUT} \parallel R_{Load}}{R_{Load}}\right)$$

$$\approx \left(\frac{2}{g_{m.M}}\right)\left(\frac{1}{2}\right)\left(-g_{m.M}\right)\left(\frac{1}{g_{m.CO}}\right)\left(g_{m.CO}\right)(1) \approx -1$$

Chapter 4

Figure 4.10:

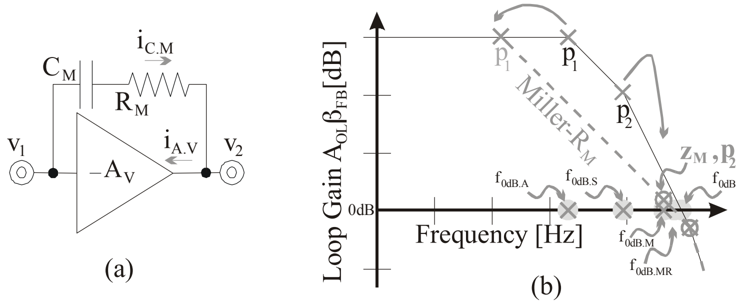


*** Unused terminal at 0, V_{Bias}, or v_I (but not in the feedback path)**

Page 153, 2nd paragraph, line 14: "…to i_O (i.e., approximately g_m) and i_O to v_{FB} (i.e., roughly R), respectively."

Equation 4.15: $A_{G.CL} \equiv \frac{i_O}{v_I} = \frac{A_{G.OL}}{1 + A_{G.OL}\beta_{FB}} \approx \frac{g_m}{1 + g_m R} \approx \frac{1}{R}$

Figure 4.20:



Page 168, 2[nd] paragraph, line 6: "…where the output voltage is zero, which means i_o or $v_{fb}/(r_\pi||R)$ is $v_e g_m(r_\pi||R||r_o)/(r_\pi||R)$ or approximately g_m."

Page 168, 3[rd] paragraph, line 12: "…current gain $A_{I.OL}$ is i_o/i_e, where i_o is M_C's gate voltage v_{gC} (or approximately, $i_e r_{o1} A_V$) into source-degenerated transconductance i_o/v_{gC}:"

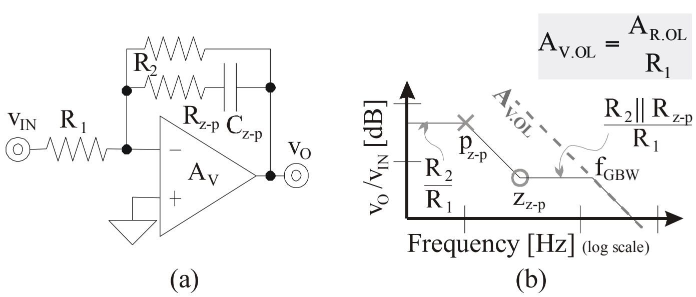
Equation 4.47:

$$A_{I.OL} = \frac{i_o}{i_e} = \frac{-i_e r_{o1}\left(-A_V\right)\left(\dfrac{i_o}{v_{gC}}\right)}{i_e} = r_{o1}\left[g_{mA}\left(r_{dsA} \parallel r_{sd3}\right)\right]\left(\frac{g_{mC}}{1+g_{mC}r_{o1}}\right) \approx g_{mA}\left(r_{dsA} \parallel r_{sd3}\right)$$

Page 169, 1[st] paragraph, line 3: "…or $r_{dsC}A_V$, where A_V is $g_{mA}(r_{dsA}||r_{sd3})$:"

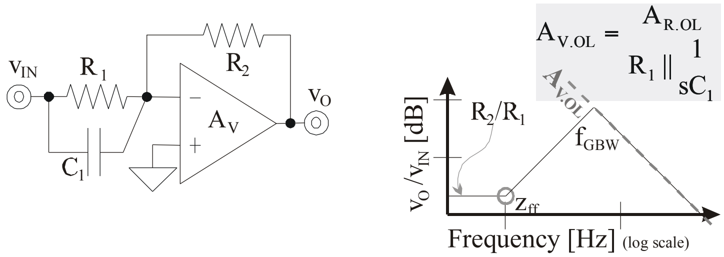
Page 185, Active LHP Zeros, line 5: "…equivalent pole-zero pair $p_{z\text{-}p}$-$z_{z\text{-}p}$ results because…"

Figure 4.24:



Page 186, paragraph 2, line 6: "…(i.e., $1/2\pi R_1 C_1$) until the gain reaches the amplifier's maximum possible gain $A_{V.OL}$, beyond which point the close-loop gain drops with $A_{V.OL}$, as shown in Fig. 4.25b."

Figure 4.25:



(a) (b)

Chapter 5:

Equation 5.13:

$$\frac{f_{0dB(max).PMOS}}{f_{0dB(min).PMOS}} = \left[GBW_{(max)}\left(\frac{p_{B(max)}}{z_{ESR(min)}}\right)\right]\left(\frac{1}{GBW_{(min)}}\right) \approx \left(\sqrt{\frac{I_{L(max)}}{I_{L(min)}}}\right)\left(\frac{C_{O(max)}}{C_{B(min)}'}\right)$$

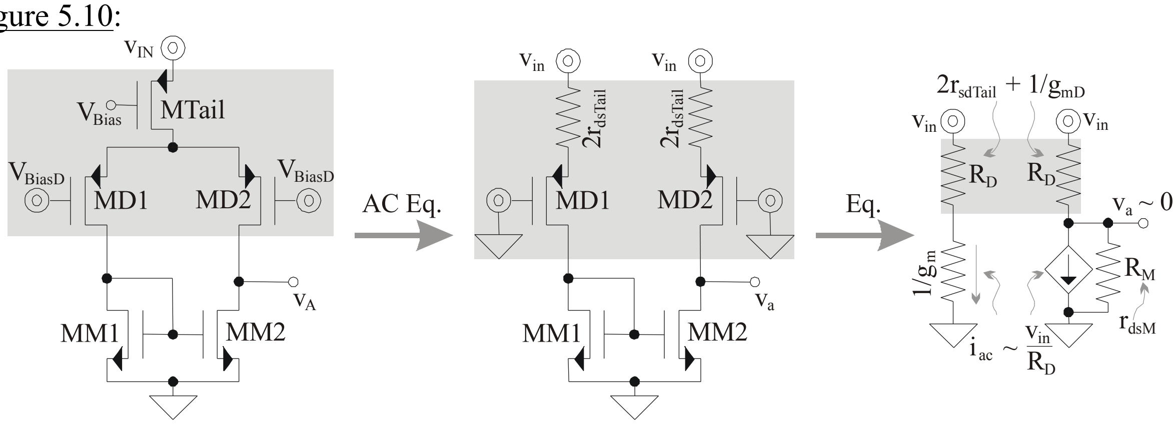
Equation 5.14:

$$\frac{f_{0dB(max).PNP}}{f_{0dB(min).PNP}} = \left[GBW_{(max)}\left(\frac{p_{B(max)}}{z_{ESR(min)}}\right)\right]\left(\frac{1}{GBW_{(min)}}\right) \approx \left(\frac{I_{L(max)}}{I_{L(min)}}\right)\left(\frac{C_{O(max)}}{C_{B(min)}'}\right)$$

Equation 5.18:

$$\frac{f_{0dB.Int(max)}}{f_{0dB.Int(min)}} = \left[\frac{1}{GBW_{Int}}\left(\frac{GBW_{Int}}{p_{O(min)}}\right)\right]\left[GBW_{Int}\left(\frac{p_{B(max)}}{z_{ESR(min)}}\right)\right] \leq 10\left(\frac{C_{O(max)}}{C_{B(min)} + C_{P(min)} + C_{L(min)}}\right)$$

Figure 5.10:



Chapter 6:

Equation 6.8:

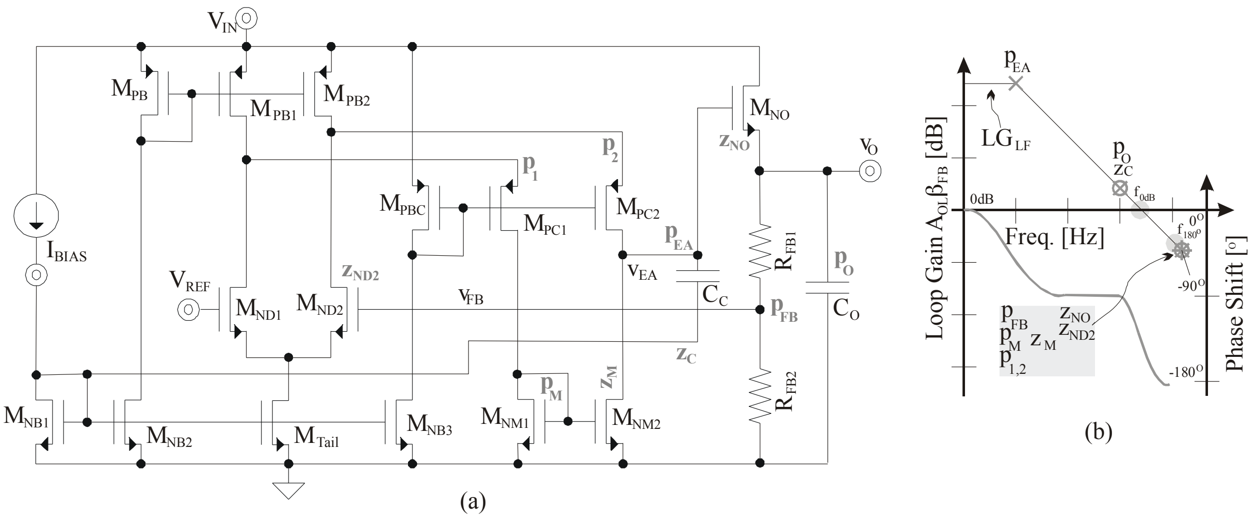
$$LG_{+FB} \approx G_{+FB}Z_{O.BUF} \approx \frac{\dfrac{G_{+FB}R_{O.BUF}}{LG_{REG}+1}}{\left(\dfrac{R_{O.BUF}C_{SW}s}{LG_{REG}+1}+1\right)} \approx \frac{\dfrac{G_{+FB}}{g_{m.BUF}(LG_{REG}+1)}}{\left[\dfrac{C_{SW}s}{g_{m.BUF}(LG_{REG}+1)}+1\right]} < 1$$

Equation 6.9:

$$LG_{REG} \approx A_{EA}A_{PO}\beta_{FB} = \frac{A_{EA}A_{PO}R_{FB1}}{R_{FB1}+R_{FB2}} > LG_{+FB}\Big|_{LG_{REG}<1} \approx \frac{\dfrac{G_{+FB}}{g_{m.BUF}}}{\left(\dfrac{C_{SW}s}{g_{m.BUF}}+1\right)}$$

Chapter 7:

Figure 7.2:



Appendix A

Derivation: Time Linear Regulators Require to Respond to a Sudden Load-current Step

A regulator, in essence, is a differential amplifier used in a non-inverting feedback configuration. As such, an equivalent gain block with a reference voltage as its non-inverting input can model its closed-loop response. Figure A.1 illustrates the circuit and its model. The output of the regulator is loaded with a capacitor having a finite ESR value and a current sink characterized by transient load-current steps. Capacitor C_O, at first charged to V_{OUT}, initially provides the current demanded by the transient load because the regulator requires some time to react. Voltage v_{OUT} therefore instantaneously drops a voltage equal to the product of the load current and the ESR of C_O. Consequently, voltage v_X instantaneously drops an attenuated version of the same. This voltage change will be considered, for this derivation, the transient stimulus against which the circuit must react to maintain a regulated output voltage. For analysis, the stimulus is referred back to V_{REF} by simply inverting the polarity of the instantaneous voltage change. This procedure allows the circuit to be modeled, as shown in the figure, by a block having the closed-loop transfer function displayed from V_{REF} to v_{OUT} with a transient voltage step as its stimulus. In this manner, the response time (system delay) to a load-current change may be approximated.

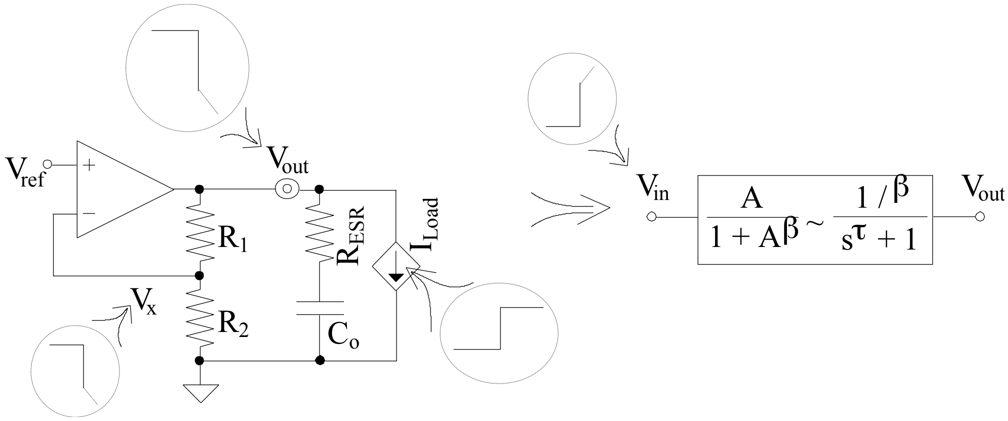


Figure A.1. Block-model development of a typical linear regulator for estimating the time delay through the system.

For simplicity, the circuit is further assumed to exhibit a single-pole response. This assumption is reasonable if any secondary pole is sufficiently displaced from the system's dominant pole. As a result, the output is expressed as a function of input v_{IN} and time constant τ:

$$v_{OUT} = v_{IN}\left(\frac{A}{1+A\beta}\right) \approx \frac{v_{IN}}{\beta}\left(\frac{1}{s\tau+1}\right), \tag{A.1}$$

where τ is $1/\omega_{BW}$, ω_{BW} the bandwidth in radians, A the forward open-loop gain of the regulator and β the feedback gain factor or R_2 / (R_1 + R_2). Figure A.2 shows the time-dependent waveforms of the load current, the consequential input referred voltage, and the output. The input referred signal is further simplified to a single step response (v_{IN}'). This approximation is done since only the delay associated with the instantaneous voltage change is pursued: approximate delay through the system for a single event. The peak-peak voltage of the step response, 1 / s in the s domain, is assumed to be 1 V; thus, v_{OUT} is

$$v_{OUT} = \frac{1}{s\beta}\left(\frac{1}{s\tau+1}\right) = \frac{1}{\beta}\left[\frac{1}{s} - \left(\frac{\tau}{s\tau+1}\right)\right] = \frac{1}{\beta}\left[\frac{1}{s} - \left(\frac{1}{s+\frac{1}{\tau}}\right)\right], \tag{A.2}$$

in the s domain, or equivalently,

$$v_{OUT} = \frac{1}{\beta}\left[1 - \exp\left(\frac{-t}{\tau}\right)\right] \tag{A.3}$$

in the time domain, where t refers to time. Consequently, time delay t_{delay} is the time span defined by the onset of the input transition to the time the output reaches 90% of its final value (i.e., 0.9 / β),

$$v_{OUT}\Big|_0^{\frac{0.9}{\beta}\text{ V}} = \frac{1}{\beta}\left[1 - \exp\left(\frac{-t}{\tau}\right)\right]\Bigg|_0^{t_{90\%}} \tag{A.4}$$

or

$$t_{delay} = t_{90\%} = \tau \ln 10 \approx 2.3\tau = \frac{2.3}{\omega_{BW}}. \tag{A.5}$$

Consequently, the approximate time delay through the regulator is 2.3 / ω_{BW}, or equivalently, 0.37 / f_{BW}.

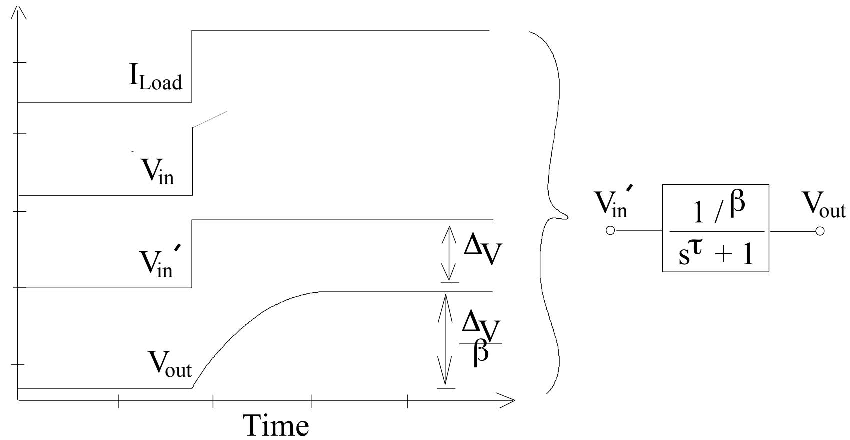


Figure A.2. Time-domain description of the system under a stepped load-current change.